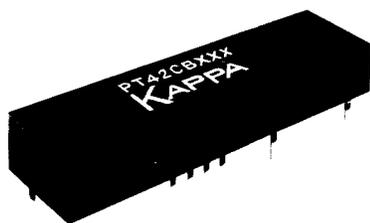


SERIES PT42 TTL SCHOTTKY (32-PIN)

# 4-BIT PROGRAMMABLE DELAY LINE



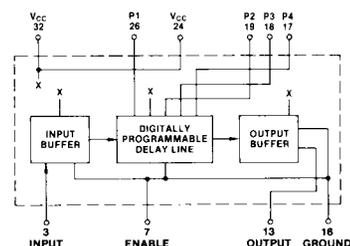
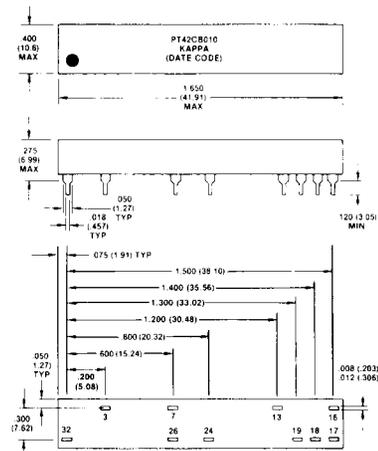
RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
V <sub>CC</sub> Supply Voltage	4.75	5.00	5.25	V
V <sub>IH</sub> High-Level Input Voltage	2.0			V
V <sub>IL</sub> Low-Level Input Voltage			0.8	V
I <sub>IK</sub> Input Clamp Current			-18	mA
I <sub>OH</sub> High-Level Output Current			-1.0	mA
I <sub>OL</sub> Low-Level Output Current			20	mA
T <sub>A</sub> Operating Free-Air Temperature	0	+25	+70	°C

FEATURES

- Inherent Delay: 15 ns ± 1 ns
- Input signal requirements: TTL logic
- Output fan-out: TTL Schottky load
- Total Delay Tolerance: ±5% or ±1 ns, WIG

MARKINGS AND DIMENSIONS, in (mm)



DC ELECTRICAL CHARACTERISTICS

TEST CONDITIONS

Parameter	Condition	MIN	TYP	MAX	UNIT
V <sub>OH</sub> High-Level Output Voltage	V <sub>CC</sub> = min, V <sub>IL</sub> = max, I <sub>OH</sub> = max	2.7	3.4		V
V <sub>OL</sub> Low-Level Output Voltage	V <sub>CC</sub> = min, V <sub>IH</sub> = min, I <sub>OL</sub> = max			0.5	V
V <sub>IK</sub> Input Clamp Voltage	V <sub>CC</sub> = min, I <sub>I</sub> = I <sub>IK</sub>			-1.2	V
I <sub>IH</sub> High-Level Input Current	V <sub>CC</sub> = max, V <sub>IN</sub> = 2.7V			50	μA
	V <sub>CC</sub> = max, V <sub>IN</sub> = 5.25V			1.0	mA
I <sub>IL</sub> Low-Level Input Current	V <sub>CC</sub> = max, V <sub>IN</sub> = 0.5V			-2	mA
I <sub>OS</sub> Short Circuit Output Current	V <sub>CC</sub> = max, V <sub>OUT</sub> = 0, one output at a time	-40		-100	mA
I <sub>CCH</sub> High-Level Supply Current	V <sub>CC</sub> = max, V <sub>IN</sub> = OPEN			90	mA
I <sub>CCL</sub> Low-Level Supply Current	V <sub>CC</sub> = max, V <sub>IN</sub> = 0			115	mA
N <sub>H</sub> Fanout High-Level Output	V <sub>CC</sub> = max, V <sub>OH</sub> = 2.7V			20	TTL load
N <sub>L</sub> Fanout Low-Level Output	V <sub>CC</sub> = max, V <sub>OL</sub> = 0.5V			10	TTL load

INPUT PULSE TEST CONDITIONS

Parameter	MIN	TYP	MAX	UNIT
E <sub>IN</sub> Pulse Voltage	3.1	3.2	3.3	V
T <sub>RI</sub> Pulse Rise-Time			2.0	ns
T <sub>W</sub> Pulse Width, of Total Delay	50	100		%
d Duty Cycle		40	50	%

FUNCTION TABLE

Enable	Address (Bit No.)				Delay Out
	4	3	2	1	
L	L	L	L	L	T <sub>0</sub>
L	L	L	L	H	T <sub>1</sub>
L	L	L	H	L	T <sub>2</sub>
L	L	L	H	H	T <sub>3</sub>
L	L	H	L	L	T <sub>4</sub>
L	L	H	L	H	T <sub>5</sub>
L	L	H	H	L	T <sub>6</sub>
L	L	H	H	H	T <sub>7</sub>
L	H	L	L	L	T <sub>8</sub>
L	H	L	L	H	T <sub>9</sub>
L	H	L	H	L	T <sub>10</sub>
L	H	L	H	H	T <sub>11</sub>
L	H	H	L	L	T <sub>12</sub>
L	H	H	L	H	T <sub>13</sub>
L	H	H	H	L	T <sub>14</sub>
L	H	H	H	H	T <sub>15</sub>
H	X	X	X	X	L

L = Logic 0  
 H = Logic 1  
 X = Don't care  
 T<sub>0</sub> = Reference or inherent delay of circuit.  
 T<sub>1</sub> to T<sub>15</sub> = Multiplier of incremental delay.

Part <sup>(2)</sup> Number	Incremental Delay Per Step <sup>(3)</sup>	Total Delay <sup>(1)</sup> Change
PT42CB010	1 ns	15 ns
PT42CB020	2 ns	30 ns
PT42CB030	3 ns	45 ns
PT42CB040	4 ns	60 ns
PT42CB050	5 ns	75 ns
PT42CB060	6 ns	90 ns
PT42CB080	8 ns	120 ns
PT42CB100	10 ns	150 ns
PT42CB120	12 ns	180 ns
PT42CB150	15 ns	225 ns
PT42CB200	20 ns	300 ns
PT42CB250	25 ns	375 ns
PT42CB300	30 ns	450 ns
PT42CB350	35 ns	525 ns
PT42CB400	40 ns	600 ns
PT42CB450	45 ns	675 ns
PT42CB500	50 ns	750 ns
PT42CB600	60 ns	900 ns
PT42CB800	80 ns	1,200 ns
PT42CB101	100 ns	1,500 ns

1. This delay value does not include the T<sub>0</sub> delay.  
 2. Other delays also available upon request.  
 3. V<sub>CC</sub> = T<sub>YP</sub>, E<sub>IN</sub> = T<sub>YP</sub>, T<sub>RI</sub> = Max, T<sub>W</sub> = T<sub>YP</sub>, d = T<sub>YP</sub>, T<sub>A</sub> = T<sub>YP</sub>



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