DESCRIPTION

The PT4305 is a PLL-tuned FSK receiver for short-range wireless data applications in the 315 MHz and 434 MHz frequency bands. The PT4305 offers a high level of integration and only requires few external components.

The PT4305's receive section includes a low-noise amplifier, image-reject mixer, IF band-pass filter, limiting amplifier, and frequency-shift keying (FSK) demodulator and also includes automatic gain control (AGC). A switched-capacitor data filter further filters the signal after the demodulator before a slicing comparator restores the data to full-swing CMOS logic levels.

The local oscillator sub-system consists of a phase-locked loop (PLL) based on a crystal oscillator reference. The receiver channel frequency is determined by the choice of the crystal frequency.

A built-in voltage regulator provides improved power supply rejection (PSR) and extends the supply voltage range from 2.4 V to 5.5 V.

The PT4305 is available in a 16-pin SSOP package and its operation is specified over the temperature range from –40 to +85 °C.

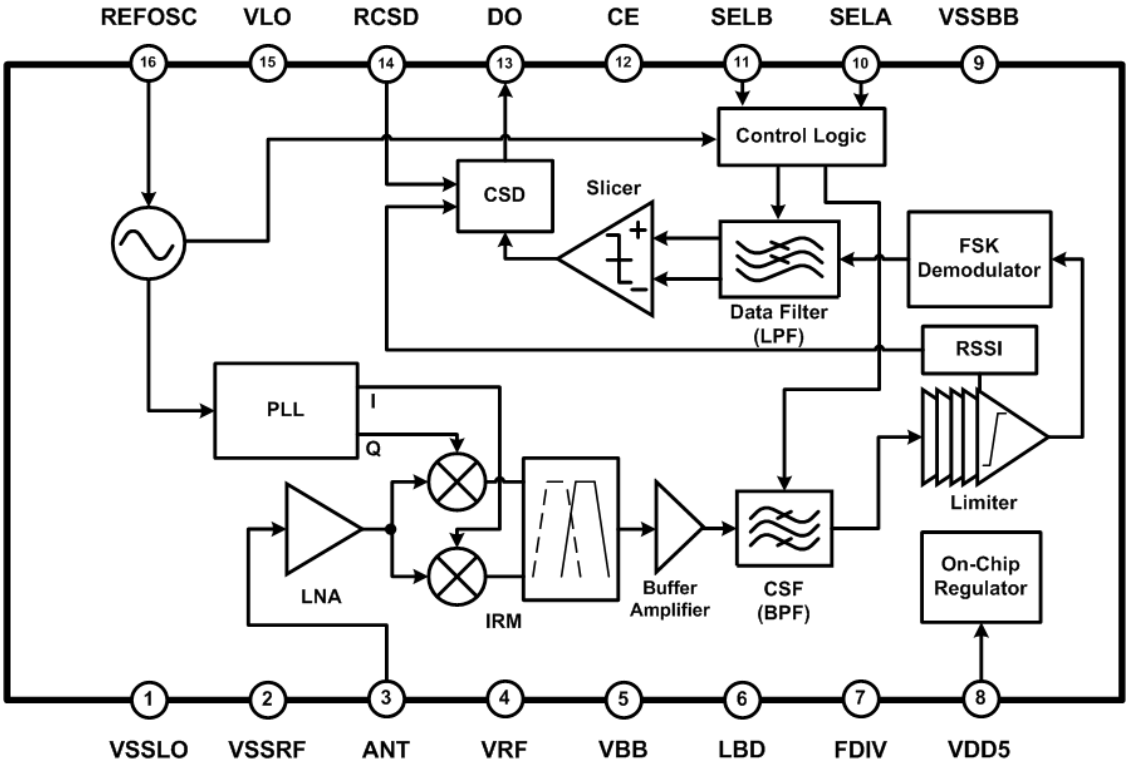
FEATURES

- Supply voltage range: 2.4 V to 5.5 V
- Low current consumption: 5.2 mA (typical) at 433.92 MHz
- Supported data rate range: 1 Kb/s to 10 Kb/s
- Few external components
- Image-reject mixer
- On-chip auto-tuned channel-select band-pass filter
- Received signal strength indicator (RSSI)
- Leader-code detection
- 16-pin SSOP package

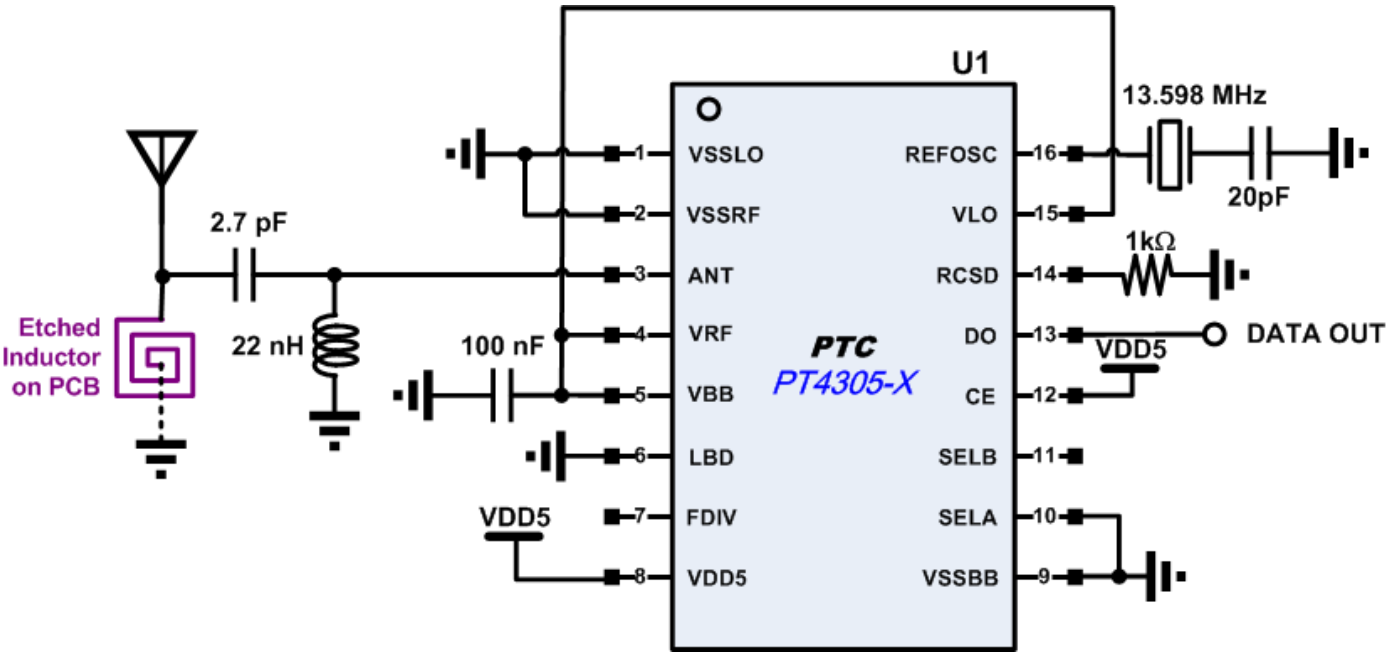
APPLICATIONS

- Remote keyless entry (RKE) systems
- Remote control
- Home security and alarm
- Wireless toy control
- Personal/patient data logging
- Remote automatic meter reading

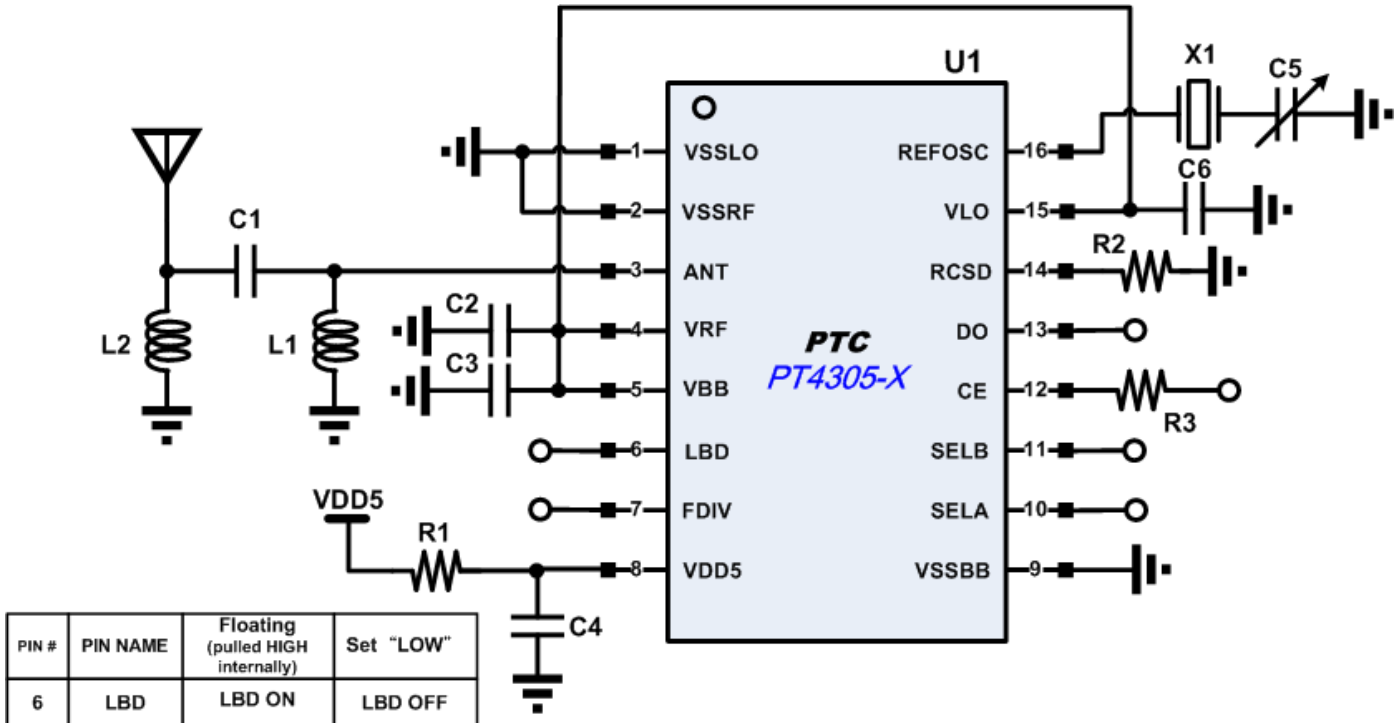
BLOCK DIAGRAM



433.92 MHz APPLICATION EXAMPLE



APPLICATION CIRCUIT



PIN #	PIN NAME	Floating (pulled HIGH internally)	Set "LOW"
6	LBD	LBD ON	LBD OFF
7	FDIV	For 433.92 MHz	For 315 MHz

BILL OF MATERIALS

Part	Value		Unit	Description
	315 MHz	433.92 MHz		
L1	47 n	22 n	H	Antenna input matching, coil inductor
L2	82 n	56 n	H	Antenna ESD protection, coil inductor (optional)
C1	1.8 p	2.7 p	F	Antenna input matching
C2/C3/C4/C6	100 n	100 n	F	Power supply de-coupling capacitor
C5	20 p	20 p	F	Dependent upon crystal oscillator vendor; for frequency fine-tuning
R1	10	10	Ω	Power supply de-coupling resistor (optional)
R2	1 K	1 K	Ω	Carrier sense threshold adjustment resistor (optional)
R3	10 K	10 K	Ω	MCU interface resistor (optional)
X1	9.882	13.598	MHz	Crystal with C_{Load} = 10 pF, for reference oscillator
U1	PT4305 IC	PT4305 IC	U1	Receiver chip

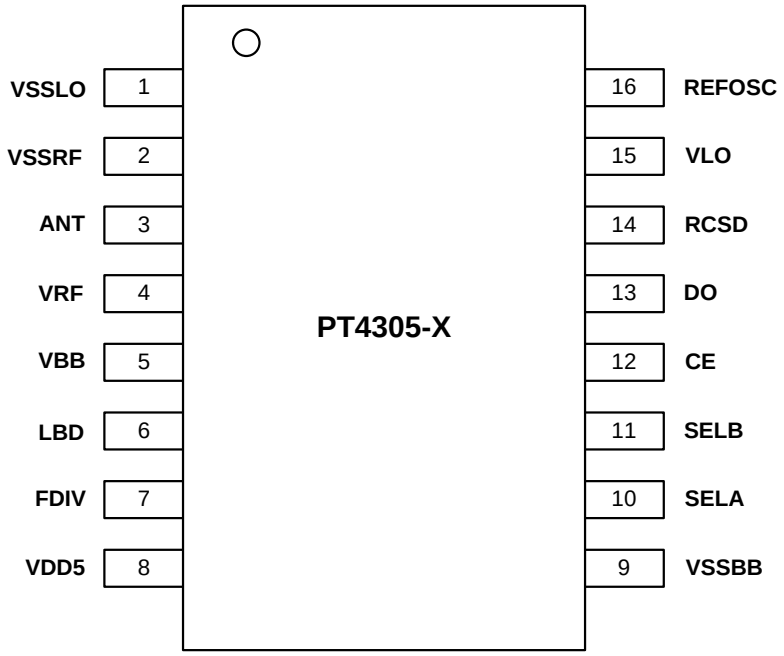
Notes:

1. L1 and C1 are the components for input matching network. They may need to be adjusted for different PCB layout and antenna requirements.
2. The *optional* components may be used depending upon specific application requirements.
3. C5 = 20pF is recommended value, the user can be adjusted to get the accurate oscillating frequency.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT4305-X	16 Pins, SSOP, 150 mil	PT4305-X

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
VSSLO	G	Ground for LO sub-system	1
VSSRF	G	Ground for RF front-end	2
ANT	I	RF input connection to antenna via a matching network	3
VRF	P	Supply voltage for RF front-end	4
VBB	P	Supply voltage for baseband chain	5
LBD	I	Leader code detection select, pulled HIGH internally. Tie to LOW to disable leader code detection feature.	6
FDIV	I	RF frequency band select, pulled HIGH internally.	7
VDD5	P	5 V regulator input	8
VSSBB	G	Ground for baseband chain	9
SELA	I	Data filter bandwidth select (pin A), pulled HIGH internally.	10
SELB	I	Data filter bandwidth select (pin B), pulled HIGH internally.	11
CE	I	Chip enable (pull HIGH to enable)	12
DO	O	Data output	13
RCSD	I/O	Carrier sense threshold adjustment resistor pin	14
VLO	P	Supply voltage for LO sub-system	15
REFOSC	I	Reference oscillator input	16

FUNCTIONAL DESCRIPTION

POWER SUPPLY

The PT4305 provides an internal voltage regulator to supply all receiver blocks. Hence, all the supply voltage pins, except VDD5, are to be connected together. Bypass capacitors should be placed as close as possible to the supply voltage pins. The VDD5 pin (pin 8) should be connected to the external supply voltage and should incorporate series-R, shunt-C filtering. The PT4305 chip can operate in the supply voltage range from 2.4 V to 5.5 V.

RF FRONT-END

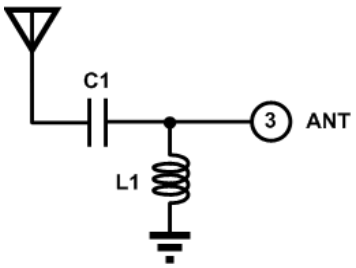
The RF front-end of the receiver employs a super-heterodyne configuration that down-converts the input radio frequency (RF) signal to an intermediate frequency (IF) signal. According to the block diagram, the RF front-end consists of an LNA and an image rejection down-conversion mixer, and the in-phase (I) and quadrature (Q) local oscillator (LO) signals for the mixer are generated from the PLL frequency synthesizer.

A special feature of the PT4305 is its integrated doubly-balanced image-rejection mixer (IRM), which eliminates the need for a costly front-end SAW filter for many applications. The advantages of not using a SAW filter include simplified antenna matching, less board space, and lower BOM cost. The mixer cell consists of a pair of doubly-balanced mixers that perform an I-Q down-conversion of the RF input to the IF band with high-side injection (i.e. $f_{RF} = f_{LO} - f_{IF}$). The image-rejection circuitry then combines these signals to achieve an image-rejection ratio typically over 30 dB. High-side injection is mandatory (e.g. low-side injection may not be selected) due to the nature of the on-chip image rejection implementation. The IF output of the IRM is connected to a buffer amplifier to drive the succeeding IF-band, channel-select filter (CSF).

The RF front-end provides the good low-noise performance (NF < 5 dB), high voltage conversion gain (> 45 dB), and excellent reverse isolation.

The ANT pin can be matched to 50 Ohm with an L-type circuit shown in the figure below. Inductor and capacitor values may be different from those in the provided BOM table depending on PCB material, PCB thickness, ground configuration, and the length of traces used in the layout.

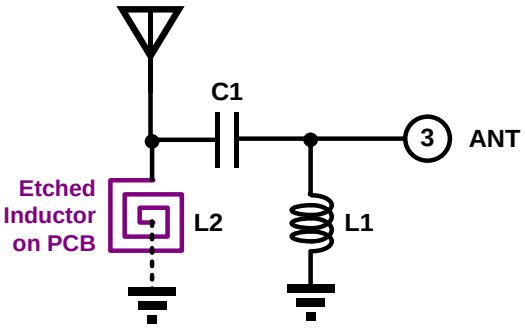
An example of the input-matching network is shown in the following figure and the input impedances of the PT4305 for 315/433.92 MHz frequency bands are listed in the right-hand side table. Please note that the component values given in the BOM for the application circuit shown on Page 3 are nominal values only.



RF Frequency f_{RF}	ANT Input Impedance (Pin 3)
315 MHz	3.58 − j173.21 Ω
433.92 MHz	4.15 − j243.24 Ω

ANTENNA PIN ESD PROTECTION

The PT4305 IC provides the ESD protection level (Human Body Mode) better than 4 KV at the ANT pin. However, higher ESD protection level may still be required at the system level for some applications. Achieving an enhanced ESD protection level will rely on external components. Changing L1 from SMD type to coil type may enhance ESD protection level by up to 1 KV, and adding a shunt coil inductor L2 (may either use an etched inductor on PCB) in front of C1 may help to further improve ESD protection.



RF Frequency f_{RF}	Suggested value for L2
315 MHz	82 nH
433.92 MHz	56 nH

REFERENCE OSCILLATOR

All timing and tuning operations on the PT4305 are derived from the internal one-pin Colpitts reference oscillator. Timing and tuning functions are provided by the REFOSC pin thru one of two methods:

1. Connect a crystal to the REFOSC pin
2. Drive the REFOSC pin with an external timing signal

When a crystal is used, the minimum oscillation voltage swing is 300 mV_{PP}. If using an externally applied signal, the signal source should be AC-coupled and its input swing should be limited to the operating range from 0.6 V_{PP} to 2.0 V_{PP}.

As with any super-heterodyne receiver, the mixing product between the internal LO (local oscillator) frequency, f_{LO}, and the incoming transmit frequency, f_{TX}, must ideally equal the IF center frequency, f_{IF}.
The following equations may be used to compute the appropriate f_{LO} for a given f_{TX}:

$f_{LO} = f_{TX} \times (352 / 351)$ for 433.92 MHz band and $f_{LO} = f_{TX} \times (256 / 255)$ for 315 MHz band.

Hence, $f_{IF} = f_{TX} \div 351$ for 433.92 MHz band and $f_{IF} = f_{TX} \div 255$ for 315 MHz band.

Using the above equations, frequencies f_{TX} and f_{LO} are computed in MHz. High-side LO injection results in an image frequency above the frequency of interest. For a given value of f_{LO}, the equation below may be used to compute the reference oscillator frequency, f_{REFOSC}:

$f_{REFOSC} = f_{LO} \div 32$.

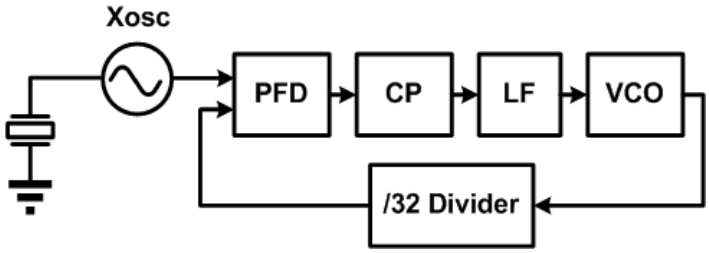
The following table specifies f_{REFOSC} for two common transmit frequencies for the PT4305 chip (high-side LO mixing).

Transmit Frequency f_{TX}	Reference Oscillator Frequency f_{REFOSC}
315 MHz	9.882 MHz
433.92 MHz	13.598 MHz

PHASE-LOCKED LOOP (PLL)

The PT4305 utilizes an integer-N PLL to generate the receiver LO. The PLL consists of a voltage-controlled oscillator (VCO), reference crystal oscillator, asynchronous ÷ 32 fixed-modulus divider, charge pump, loop filter and phase-frequency detector (PFD). All components are integrated on-chip. The PFD compares two signals and produces an error signal that is proportional to the difference between the input signal phases. The error signal passes through a loop filter that provides a loop bandwidth of approximately 200 KHz, and is used to control the VCO. The VCO output frequency is fed back through the fixed-modulus frequency divider to one input of the PFD. The other input to the PFD comes directly from the reference crystal oscillator. Thus, the VCO output frequency, which is used as the LO frequency, is phase-locked to the reference frequency and $f_{REFOSC} = (f_{TX} + f_{IF}) \div 32 = f_{LO} \div 32$.

The block diagram below illustrates the basic elements of the PLL.



CHANNEL-SELECT FILTER

The PT4305 embeds a channel-select filter (CSF) with a bandwidth of approximately 380 KHz. The CSF is implemented as a sixth-order active filter for the low-IF architecture. An automatic frequency tuning circuit is also included on-chip and its absolute reference clock is derived from the reference crystal oscillator. The automatic frequency tuning circuit centers the pass-band of the CSF at the IF frequency (f_{IF}).

FSK DEMODULATOR

The PT4305 utilizes a balanced digital logic quadricorrelator to demodulate the frequency-shift keyed (FSK) signal. The recommended frequency deviation (f_{DEV}) of FSK modulation is from ±50 KHz to ±75 KHz. Please note that the receive LO frequency must be tuned to reside within the $\pm f_{DEV}$ window of the transmit carrier frequency. If the frequency of the transmitter shifts too much from a specified value (315MHz or 433.92MHz), the frequency deviation (f_{DEV}) should be increased to obtain a wider operation window.

LIMITER/RSSI

The RSSI is implemented as a successive detection logarithmic amplifier which follows the internal CSF. The logarithmic amplifier achieves ±3 dB logarithmic linearity and the RSSI output level achieves a dynamic range of approximately 60 dB when the automatic gain control (AGC) circuitry is disabled, and of over 85 dB when the AGC circuitry is enabled. The RSSI slope is approximately 10.5 mV/dB.

DATA FILTER

The data filter (post-demodulator filter) is utilized to remove additional unwanted signals after the FSK demodulator. The data filter is implemented as a 2nd-order low-pass Sallen-Key filter. The data filter bandwidth (BW_{DF}) must be selected according to the application requirement and should be set according to the equation

BW_{DF} = 0.65 / shortest pulse-width

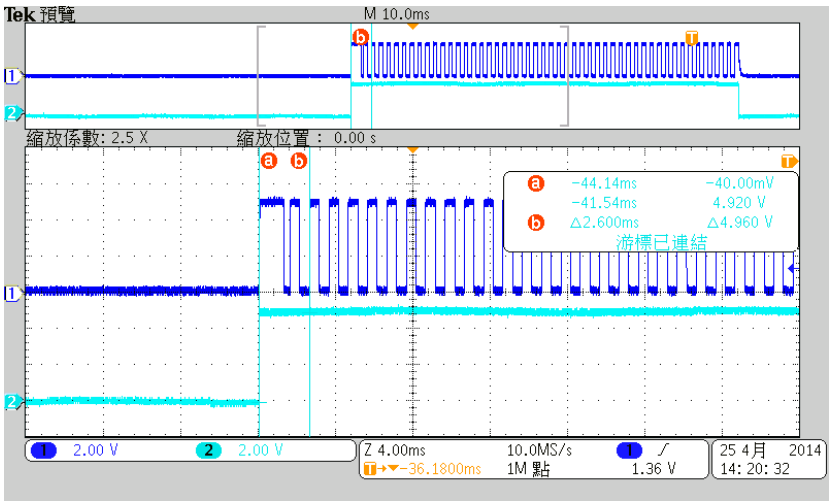
The input pins of SELA and SELB control the data filter bandwidth in four binary steps as shown in the table below. Please note that the values indicated in this table are nominal values. The filter bandwidth scales linearly with frequency so the exact value will depend on the operating frequency.

SELA	SELB	Data Filter Bandwidth BW_{DF}	
		f_{RF} = 315 MHz	f_{RF} = 433.92 MHz
1	1	900 Hz	1250 Hz
1	0	1800 Hz	2500 Hz
0	1	3600 Hz	5000 Hz
0	0	7200 Hz	10000 Hz

POWER-DOWN CONTROL

The chip enable (CE) pin controls the power on/off behavior of the PT4305. Connecting CE to logic HIGH sets the PT4305 to its normal operation mode; connecting CE to logic LOW sets the PT4305 to standby mode. The chip current consumption will be lower than 1 μA in standby mode. Once enabled, the PT4305 relies on an internal fast start-up circuit to achieve a start-up time which is less than 3 ms to recover received data at 3-dB above the minimum received RF input level.

The following figure exhibits the system start-up time in the conditions of Temp = 27ºC, f_{RF} = 433.92 MHz, P_{RF} = –105 dBm, f_{DEV} = ±50 KHz and D_{RATE} = 2 Kb/s. The CE pin is triggered every 100 mS.



ANTENNA DESIGN

For a $\lambda/4$ dipole antenna and operating frequency, f (in MHz), the required antenna length, L (in cm), may be calculated by using the formula

$$L = \frac{7132}{f}$$

For example, if the frequency is 315 MHz, then the length of a $\lambda/4$ antenna is 22.6 cm. If the calculated antenna length is too long for the application, then it may be reduced to $\lambda/8$, $\lambda/16$, etc. Without degrading the input return loss. However, the RF input matching circuit may need to be re-optimized. Note that in general, the shorter the antenna, the worse the receiver sensitivity and the shorter the detection distance. Usually, when designing a $\lambda/4$ dipole antenna, it is better to use a single conductive wire (diameter about 0.8 mm to 1.6 mm) rather than a multiple core wire.

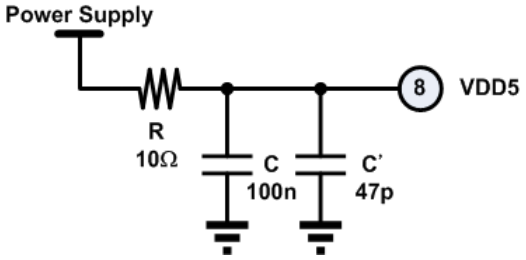
If the antenna is printed on the PCB, ensure there is neither any component nor ground plane underneath the antenna on the backside of PCB. For an FR4 PCB (ε_r = 4.7) and a strip-width of 30 mil, the length of the antenna, L (in cm), is calculated by

$$L = \frac{c}{4 \times f \times \sqrt{\varepsilon_r}}$$ where "c" is the speed of light (3 x10^{10} cm/s).

PCB LAYOUT CONSIDERATION

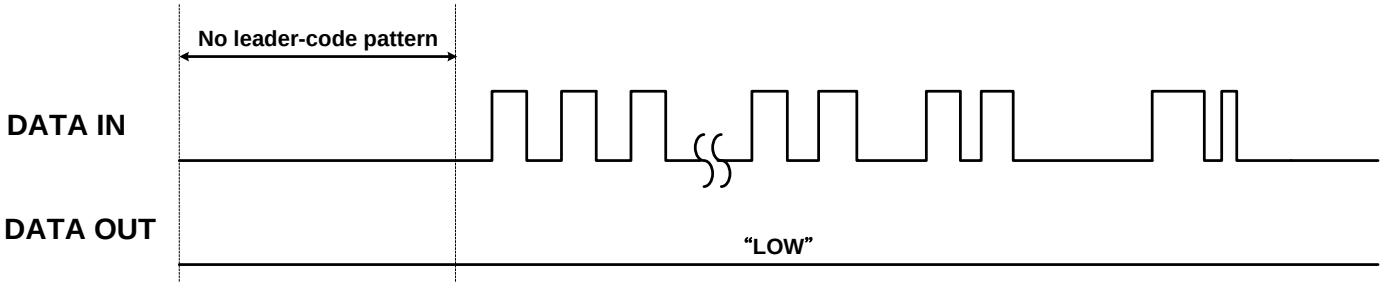
Proper PCB layout is extremely critical in achieving good RF performance. At the very least, using a two-layer PCB is strongly recommended, so that one layer may incorporate a continuous ground plane. A large number of via holes should connect the ground plane areas between the top and bottom layers. Note that if the PCB design incorporates a printed loop antenna, there should be no ground plane beneath the antenna.

Careful consideration must also be paid to the supply power and ground at the board level. The larger ground area plane should be placed as close as possible to all the VSS pins. To reduce supply bus noise coupling, the power supply trace should be incorporate series-R, shunt-C filtering as shown below.



LEADER CODE DETECTOR (OPTIONAL)

The PT4305 supports a leader code function to detect the actual data (this function is enabled when the LBD pin is set to HIGH). If the data frame doesn't have a leader code pattern in front of the data code, the output of the chip will always be kept LOW. At the same time, the chip continuously detects the leader code pattern.



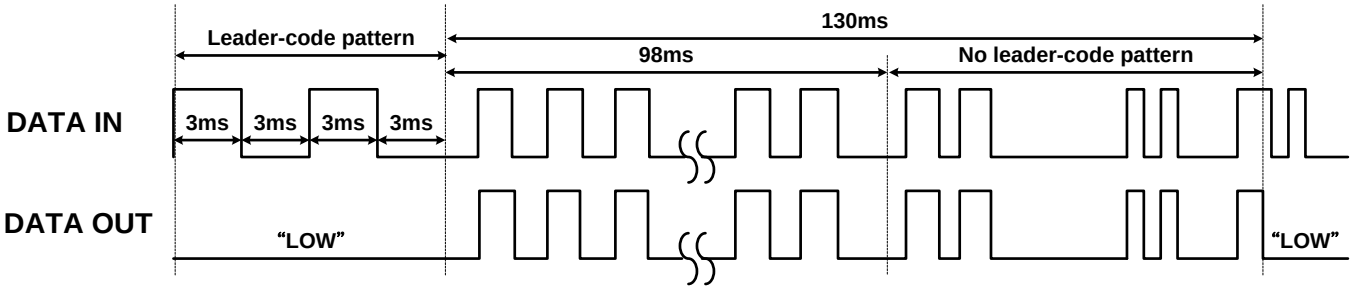
If the data frame has a leader code pattern in front of the data, the chip will remove the leader code automatically and only output the data.

In the PT4305, the leader code pattern consists of a 4-bit code of HIGH-LOW-HIGH-LOW and each bit must be maintained for 3 ms with ±5 % variation. (The acceptable duration time of each bit in the leader code pattern is between 2.85 ms and 3.15 ms)

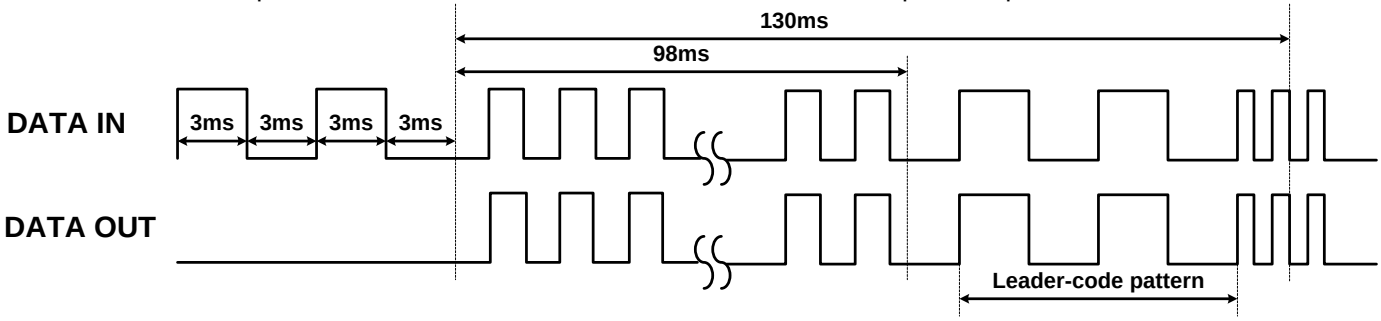
When the PT4305 detects the leader code pattern, it starts to output the data for 98 ms. During this time (0 to 98 ms), the leader-code detector does not check for the leader code pattern and just outputs the data bits.

After 98 ms of data output, the leader-code detector will again re-check for the leader code pattern.

If no leader code pattern is detected between 98 ms and 130 ms, the output of the chip will be kept LOW after 130 ms.



If another leader code pattern is detected between 98 ms and 130 ms, the chip will output the data as described above.

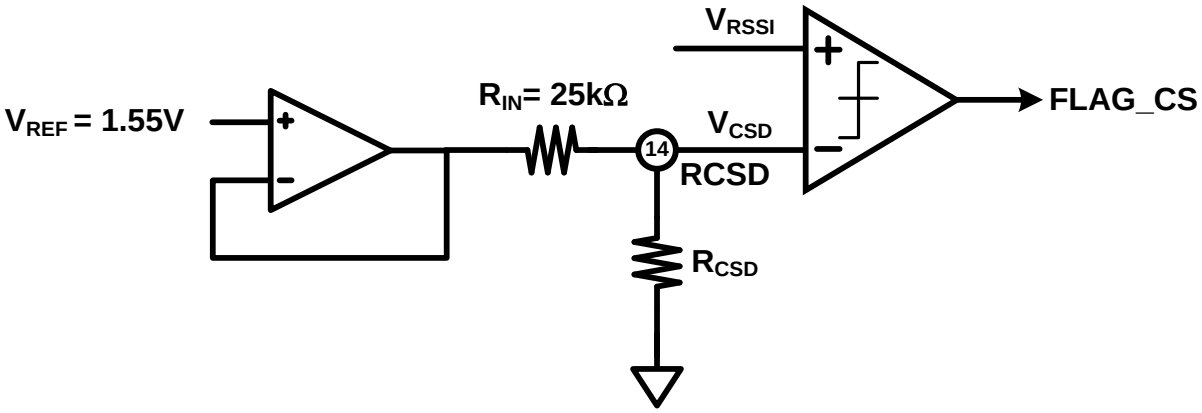


CARRIER SENSE DETECT FUNCTION (OPTIONAL)

PT4305 provides a carrier sense detect (CSD) function that may be used for receiving information (i.e. to detect a "live" carrier). The CSD function is always enabled when the chip enable is pulled HIGH[NOTE].

When the RSSI voltage corresponding to an input signal is lower than a specified threshold (V_{CSD}), the internal signal FLAG_CS = LOW. In this case, the DO output will always be kept LOW by the CSD circuitry.

When the RSSI voltage corresponding to an input signal is larger than the V_{CSD} threshold, the internal signal FLAG_CS = HIGH. In this case, the DO output will start to output data.



The threshold of the CSD function may be adjusted by an external resistor, R_{CSD}. The threshold value varies from 0 to 1.55 V according to the value of R_{CSD}.

$$V_{CSD} = \mathbf{V}_{REF} \times \frac{R_{CSD}}{R_{CSD} + R_{IN}}$$

The on-chip reference voltage, V_{REF}, is generated by a reference current flow through a series of polysilicon. However, due to process, noise, and temperature variations, the on-chip reference voltage will be changed slightly.

The threshold voltage, V_{CSD}, should be set slightly above the minimum RSSI voltage to inhibit random fluctuations when there is no input RF signal. However, setting the threshold voltage too high may lower the sensitivity of the PT4305.

To disable the CSD function, the threshold voltage may be set lower than the minimum RSSI voltage. In this case, the FLAG_CS signal is always LOW.

In the PT4305, a 1 KΩ resistor is connected from pin 14 (RCSD) to ground to disable the CSD function.

NOTE: The carrier-sense detect function will be disabled automatically when the lead-code detector is enabled (when the LBD pin kept floating).

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage Range	V_{DD5}	–0.3	6	V
Analog I/O Voltage	—	–0.3	3	V
Digital I/O Voltage	—	–0.3	6	V
Operating Temperature Range	T_A	–40	+85	°C
Storage Temperature Range	T_{STG}	–40	+125	°C

PACKAGE THERMAL CHARACTERISTIC

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
From Chip Conjunction Dissipation to External Environment	Rja	T_A = 27 °C	—	37.15	—	°C/W
From Chip Conjunction Dissipation to Package Surface	Rjc		—	1	1.8	

ELECTRICAL CHARACTERISTICS

Nominal conditions: V_{DD5} = 5.0 V, V_{SS} = 0 V, CE = HIGH, T_A = +27°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General Characteristics						
Supply Voltage	V_{DD5}	Supply voltage applied to VDD5 pin only	2.4	5	5.5	V
Current Consumption	I_{DD5}	f_{RF} = 315 MHz	4.5	5	5.5	mA
		f_{RF} = 433.92 MHz	4.7	5.2	5.7	
Standby Current	I_{STBY}	CE = LOW	—	—	1	A
Operating Frequency	f_{RF}	FDIV = LOW	—	315	—	MHz
		FDIV = Floating	—	433.92	—	
Maximum Receiver Input Level	$P_{RF,MAX}$		–20	–15	—	dBm
Sensitivity[1]	S_{IN}	FSK[2], Bd_{RATE} = 2 Kb/s, f_{DEV} = ±50 KHz at 315 MHz	—	–107	–104	dBm
		FSK[2], Bd_{RATE} = 2 Kb/s, f_{DEV} = ±50 KHz at 433.92 MHz	—	–106	–103	dBm
Data Rate	DR		—	2	10	Kb/s
Transmit Modulation Deviation	f_{DEV}		±50	±60	±75	KHz
System Start-Up Time	T_{STUP}		2	4	6	ms
RF Front-End						
Image Rejection Ratio	IRR		25	30	—	dB
LO Leakage	L_{LO}	Measured at antenna input	—	—	–70	dBm
IF Section						
IF Center Frequency	f_{IF}	f_{RF} = 315 MHz	—	1.235	—	MHz
		f_{RF} = 433.92 MHz	—	1.236	—	
IF Bandwidth	BW_{IF}		—	380	—	KHz
RSSI Slope	SL_{RSSI}		9	10.5	12	mV/dB
Demodulator						
Post-Demodulator Filter Bandwidth (f_{RF} = 315 MHz)	BW_{DF}	SELA = SELB = floating	—	0.9	—	KHz
		SELA = floating; SELB = LOW	—	1.8	—	
		SELA = LOW; SELB = floating	—	3.6	—	
		SELA = SELB = LOW	—	7.2	—	
Post-Demodulator Filter Bandwidth (f_{RF} = 433.92 MHz)	BW_{DF}	SELA = SELB = floating	—	1.25	—	KHz
		SELA = floating; SELB = LOW	—	2.5	—	
		SELA = LOW; SELB = floating	—	5	—	
		SELA = SELB = LOW	—	10	—	
Phase-Locked Loop						
Reference Frequency	f_{REFOSC}	FDIV = LOW	—	9.882	—	MHz
		FDIV = floating	—	13.598	—	MHz
Reference Signal Voltage Swing[3]	V_{REF}	Peak-to-peak voltage (V_{PP})	0.6	—	2	V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
VCO Frequency Range	f_{VCO}		250	—	500	MHz
Divider Ratio	DIV		—	32	—	—
Digital/Control Interface						
Input-High Voltage	V_{IH}	CE pin	0.8 × V_{DD5}	—	—	V
Input-Low Voltage	V_{IL}	CE, LBD, FDIV, SELA, SELB pins	—	—	0.2 × V_{DD5}	V
Output Current	I_{OUT}	Source current at 0.8 × V_{DD5}	—	480	—	A
		Sink current at 0.2 × V_{DD5}	—	600	—	
Output-High Voltage	V_{OH}	DO pin, I_{OUT} = –1 μA	0.9 × V_{DD5}	—	—	V
Output-Low Voltage	V_{OL}	DO pin, I_{OUT} = +1 μA	—	—	0.1 × V_{DD5}	V
Output Rise/Fall Times	t_R / t_F	DO pin, C_{LOAD} = 15 pF	—	2	—	s

Notes:
1. The sensitivity is defined as the lowest input level to achieve BER = 1e–3 when receiving NRZ data.
2. Baud Rate = 2 Kb/s, FSK modulation deviation = ±50 KHz, 50% duty cycle
3. Depends on the ESR of the crystal

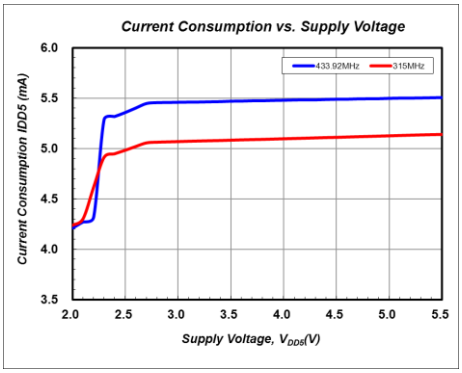


Figure 1. Current Consumption vs. Supply Voltage

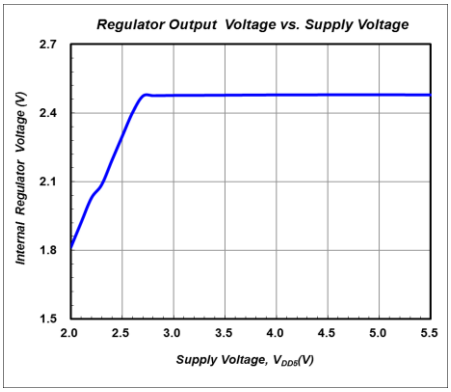


Figure 2. Voltage Regulator Characteristic

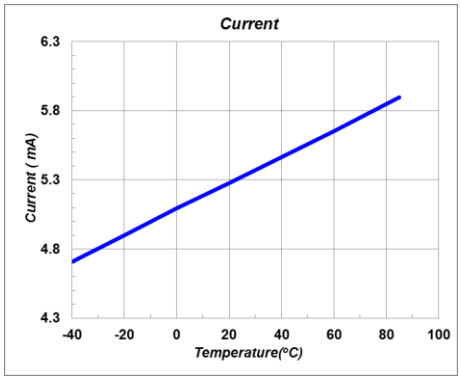


Figure 3. Current Consumption vs. Temperature[NOTE]

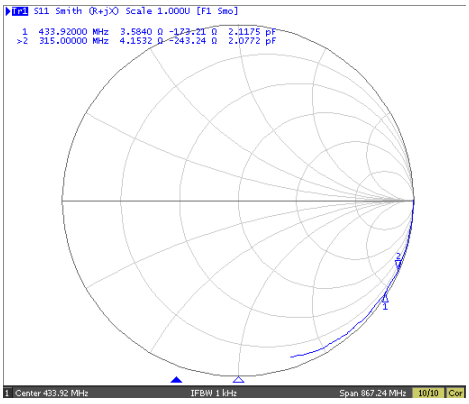


Figure 4. Smith Plot of ANT

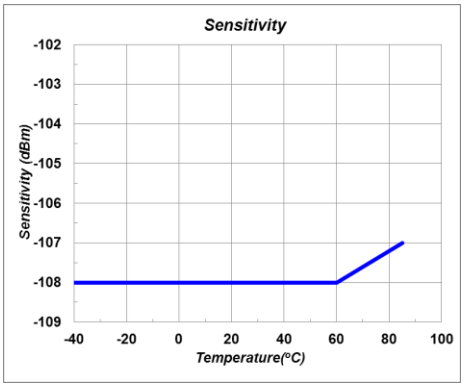
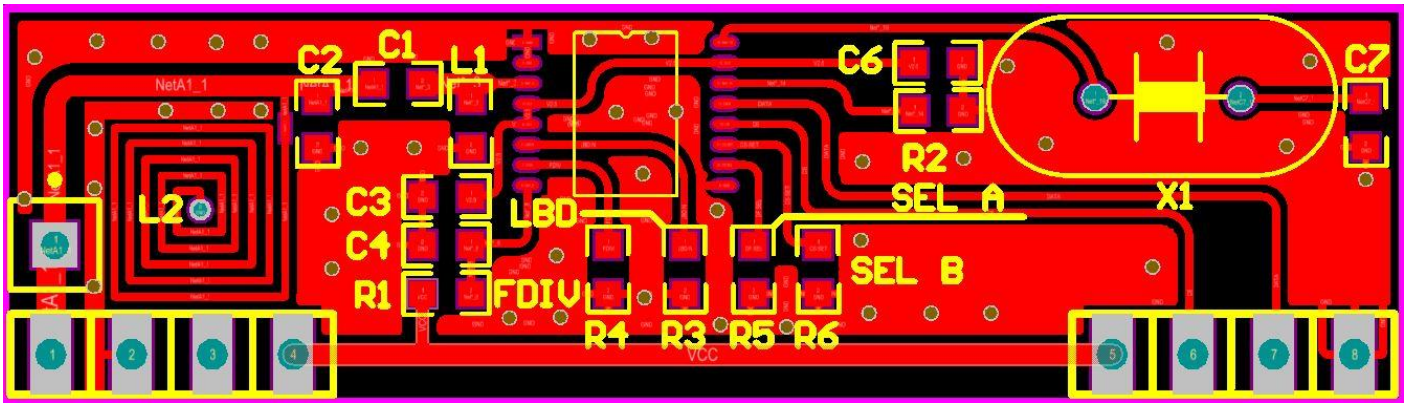


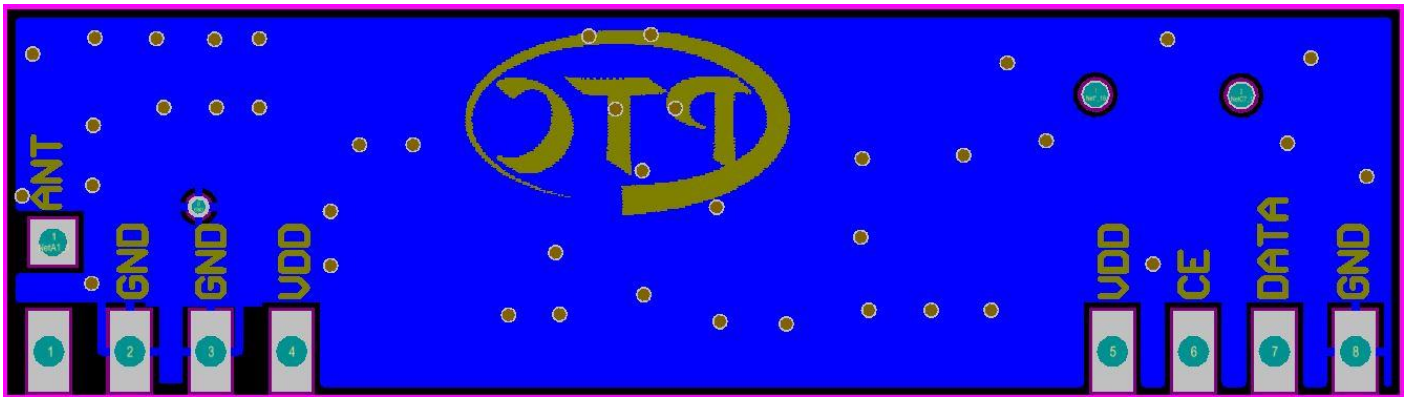
Figure 5. Sensitivity vs. Temperature [NOTE]

NOTE: V_{DD5} = 5 V, f_{RF} = 433.92 MHz, SELA/SELB = floating/LOW, D_{RATE} = 2 Kb/s, f_{DEV} = ±50 KHz; sweep temperature from –40 °C to 85 °C.

EVALUATION BOARD LAYOUT



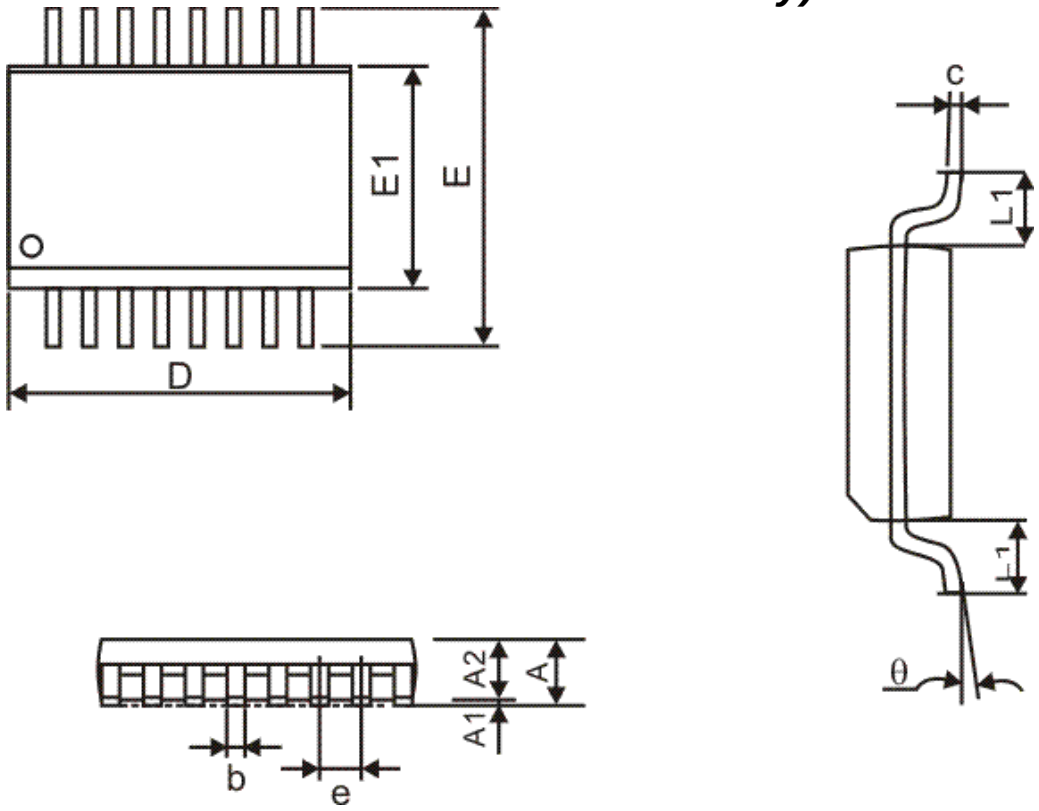
<Top Side>



<Bottom Side>

PACKAGE INFORMATION

16 Pins, SSOP (Shrink Small Outline Package with 3.9 × 4.9 mm Body Size, 0.64 mm Pitch Size and 1.6 mm Thick Body)



Symbol	Min.	Nom.	Max.
A	-	-	1.750
A1	0.100	-	-
A2	1.245	-	-
b	0.203	-	0.305
c	0.102	-	0.254
D	4.90 BSC		
e	0.635 BSC		
E	6.00 BSC		
E1	3.90 BSC		
L1	1.04 REF		
θ	0º	-	8º

Notes:

1. Refer to JEDEC MO-137AB
2. Unit: mm

IMPORTANT NOTICE

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