PT5301

2 Watts Audio Power Amplifier

GENERAL DESCRIPTION

The PT5301 is an audio power amplifier mainly designed for applications in mobile phones and other portable communication device applications. It is capable of delivering 1.25 watts of continuous average power to an 8Ω load and 2 watts of continuous average power to a 4Ω load with less than 1% distortion (THD+N) from a 5V power supply. The PT5301 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.
The PT5301 features a low-power shutdown mode and improved pop & click circuitry that attenuates noise which would otherwise occur during turn on and turn off transactions. The PT5301 is delivered with miniature MSOP-8, DFN-8 and SMD-9 packages (Pd free).

APPLICATION

- Mobil Phones
- PDAs
- Portable electronic devices

FEATURES

- Low Distortion

0.50W @ VDD=5.0V, R_L=8Ω THD+N = 0.03%
0.25W @ VDD=3.0V, R_L=8Ω THD+N = 0.04%
0.15W @ VDD=2.6V, R_L=8Ω THD+N = 0.05%

- Output Power @ 1% THD+N

1.25W @ VDD=5.0V, RL=8Ω
2.0W @ VDD=5.0V, RL=4Ω
0.425W @ VDD=3.0V, R_L=8Ω
0.60W @ VDD=3.0V, R_L=4Ω
0.30W @ VDD=2.6V, R_L=8Ω
0.40W @ VDD=2.6V, R_L=4Ω

- Ultra low shutdown current
- Improved pop & click noise eliminating function
- No need for output coupling or bootstrap capacitors
- 2.2 -5.5V operation supply voltage
- Thermal protection
- External gain configuration capability
- Pd free MSOP-8, DFN-8, and SMD-9 packages
- Unity-gain stable

ORDERING INFORMATION

Pd-Free PACKAGE	TEMPERATURE	ORDER PART NUMBER	TRANSPORT MEDIA	MARKING
MSOP-8	-40°C to 85 °C	PT5301EMSO	Tape and Reel	PT5301 XXXXXC
SMD-9	-40°C to 85 °C	PT5301ESMD	Tape and Reel	P5301 XXXXX
DFN-8	-40°C to 85 °C	PT5301EQFN	Tape and Reel	PT5301 XXXXXC

TYPICAL APPLICATION

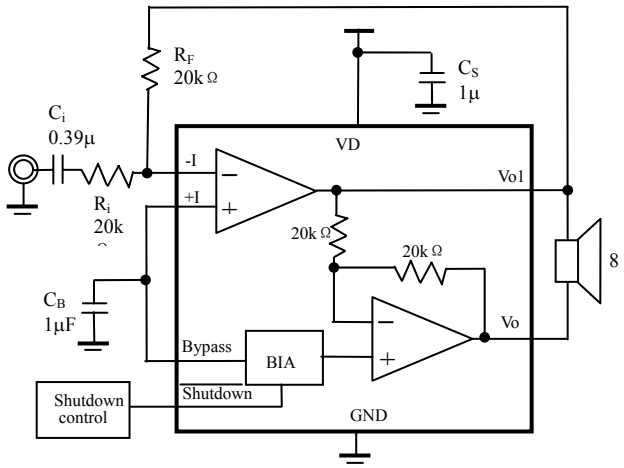
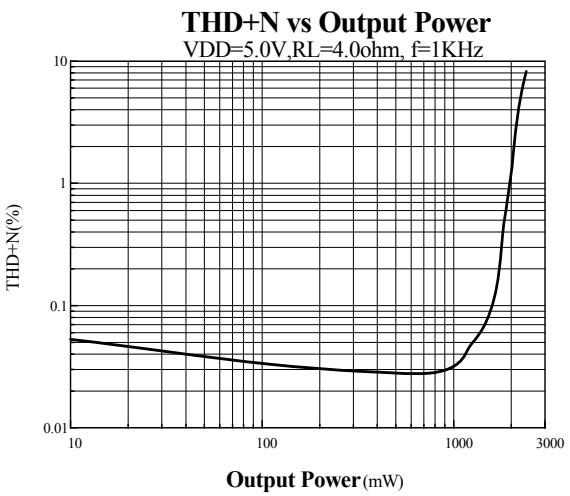
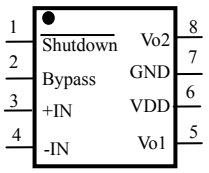


Figure 1. Typical Audio Amplifier Application Circuit.

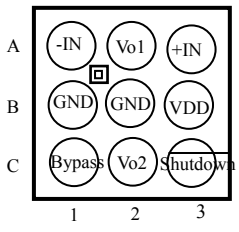
KEY PERFORMANCE CHART



PIN ASSIGNMENT



MSOP8/DFN8 Top View



SMD9 Top View

PIN DESCRIPTIONS

MSOP8/ DFN8	SMD9	NAMES	DESCRIPTION
1	C3	Shutdown	Turn-on or turn-off the chip
2	C1	Bypass	Set the common voltage
3	A3	+IN	The non-inverting input node
4	A1	-IN	The inverting input node
5	A2	Vo1	The 1st node of outputs
6	B3	VDD	Power supply 2.5~5.5V
7	B1, B2	GND	ground
8	C2	Vo2	The 2nd node of outputs

ABSOLUTE MAXIMUM RATINGS (Note 1)

ITEMS	VALUE	UNIT
Supply Voltage	6	V
Input Voltage	-0.3～VDD+0.3	V
Thermal Resistance, MSOP8: θ_{JA}/θ_{JC}	190/56	℃/W
Thermal Resistance, SMD9: θ_{JA} (Note 3)	180	℃/W
Power Dissipation (Notes 5, 6)	Internal limited	
Operating Temperature	-40 to 85	℃
ESD Susceptibility (Note 4)	2500	V
Storage Temperature	-65 to 150	℃
Package Lead Soldering Temperature	260℃, 10s	℃

RECOMMENDED OPERATING RANGE (Note 2)

SYMBOL	PARAMETER	VALUE
T_A	Temperature Range	-40°C≤T_A≤85°C
V_{DD}	Supply Voltage	2.2V≤V_{DD}≤5.5V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.
Note 3: All bumps have the thermal resistance and contribute equally when used to lower thermal resistance. All bumps must connected to achieve specified thermal resistance
Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the PT5301, see power derating curves for additional information.

Note 6: Maximum power dissipation in the device (P_{DMAX}) occurs at an output power level significantly below full output power. P_{DMAX} can be calculated using Equation 1 shown in the Application Information section. It may also be obtained from the power dissipation graphs.

ELECTRICAL CHARACTERISTICS VDD = 5V (Notes 7, 8)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. TA = 25˚C.

SYMBOL	ITEMS	CONDITIONS	TYP	LIMIT	UNITS
I_{dd}	Quiescent Power Supply Current	V_{in}=0V,I_O=0A,No Load	2.9	4.5	mA
		V_{in}=0V,I_O=0A, 8Ω Load	2.9	5	mA
I_{sd}	Shutdown current	$V_{shutdown}$ =0 (Note 9)	0.1	2	uA
V_{sdih}	Shutdown Voltage Input High		1.6		V
V_{sdil}	Shutdown Voltage Input Low		1.4		V
V_{os}	Output Offset Voltage		1.3	50	mV
Po	Output Power (8Ω Load)	f=1k; THD+N=1% (max)	1.25	0.9	W
	Output Power (4Ω Load)	f=1k; THD+N=1% (max)	2		W
T_{wu}	Wake-up time		146		ms
THD	Total Harmonic Distortion + Noise	Po=0.5Wrms; f=1k, 8Ω Load	0.03		%
PSRR	Power Supply Rejection Ratio	Input float, V_{ripple}=200mV sine wave p-p	90 (f=217Hz), 79 (f=1k)		
		Input terminated with 10Ω, V_{ripple}=200mV sine wave p-p	71 (f=217Hz), 69 (f=1k)	57 (min)	dB
Ro	Resistor Output to GND(Note 10)		11.0	9.7	kΩ(min)
				12.5	kΩ(max)

ELECTRICAL CHARACTERISTICS V_{DD} = 3V (Notes 7, 8)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. TA = 25˚C.

SYMBOL	ITEMS	CONDITIONS	TYPICAL	LIMIT	UNITS
I_{dd}	Quiescent Power Supply Current	V_{in}=0V, Io=0A, No Load	2.8	4.3	mA
		V_{in}=0V, Io=0A, 8Ω Load	2.8	5	mA
I_{sd}	Shutdown current	$V_{shutdown}$ =0 (Note 9)	0.1	2	uA
V_{sdih}	Shutdown Voltage Input High		1.1		V
V_{sdil}	Shutdown Voltage Input Low		1.0		V
V_{os}	Output Offset Voltage		1.3	50	mV
Po	Output Power (8Ω Load)	f=1k;THD+N=1%(max)	425		mW
	Output Power (4Ω Load)	f=1k;THD+N=1% (max)	600		mW
T_{wu}	Wake-up time		150		ms
THD	Total Harmonic Distortion +	Po=0.25Wrms;f=1k,8Ω	0.04		%
PSRR	Power Supply Rejection Ratio	Input float, V_{ripple}=200mV sine wave p-p	88 (f=217), 79 (f=1k)		
		Input terminated with 10Ω, V_{ripple}=200mV sine wave p-p	67 (f=217), 68 (f=1k)	55 (min)	dB
Ro	Resistor Output to GND(Note 10)		11.0	9.7	kΩ(min)
				12.5	kΩ(max)

ELECTRICAL CHARACTERISTICS V_{DD} = 2.6V (Notes 7, 8)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. TA = 25˚C.

SYMBOL	ITEMS	CONDITIONS	TYPICAL	LIMIT	UNITS
I_{dd}	Quiescent Power Supply Current	V_{in}=0V, Io=0A, No Load	2.8	4.3	mA
		V_{in}=0V, Io=0A, 8Ω Load	2.8	5	mA
I_{sd}	Shutdown current	$V_{shutdown}$ =0 (Note 9)	0.1	2	uA
V_{sdih}	Shutdown Voltage Input High		1		V
V_{sdil}	Shutdown Voltage Input Low		0.9		V
V_{os}	Output Offset Voltage		1.3	50	mV
Po	Output Power (8Ω Load)	f=1k;THD+N=1%(max)	300		mW
	Output Power (4Ω Load)	f=1k;THD+N=1% (max)	400		mW

ELECTRICAL CHARACTERISTICS V_{DD} = 2.6V (Continued) (Notes 7, 8)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. TA = 25°C.

SYMBOL	ITEMS	CONDITIONS	TYPICAL	LIMIT	UNITS
T_{wu}	Wake-up time		153		ms
THD	Total Harmonic Distortion + Noise	Po=0.15Wrms; f=1k, 8Ω Load	0.05		%
PSRR	Power Supply Rejection Ratio	Input terminated with 10Ω,	66 (f=217), 68 (f=1k)		dB
Ro	Resistor Output to GND (Note 10)		11.0	9.7	kΩ(min)
				12.5	kΩ(max)

Note 7: Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 8: "Typical" means that measured at 25°C and represent the parametric norm. "Limit" indicates that are guaranteed by PowTech's quality control standards. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 9: For micro SMD package, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase ISD by a maximum of 2μA.

Note 10: R_O is measured from the output pin to ground. This value represents the parallel combination of the 15kΩ output resistors and the two 20kΩ resistors.

EXTERNAL COMPONENTS DESCRIPTION

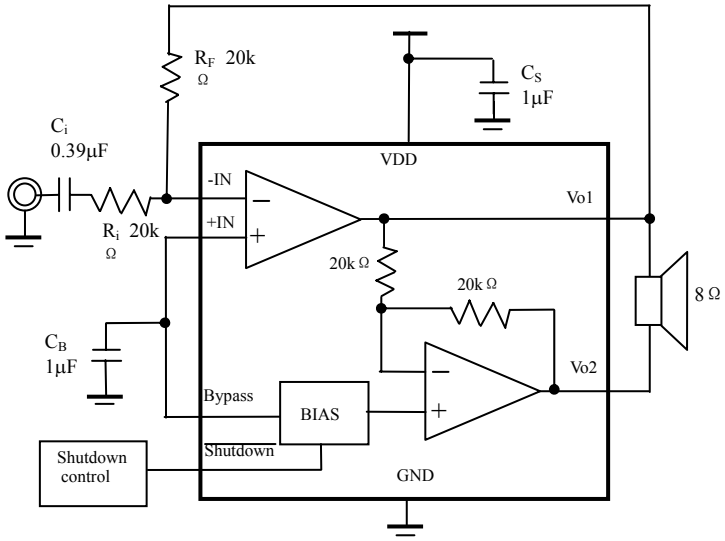
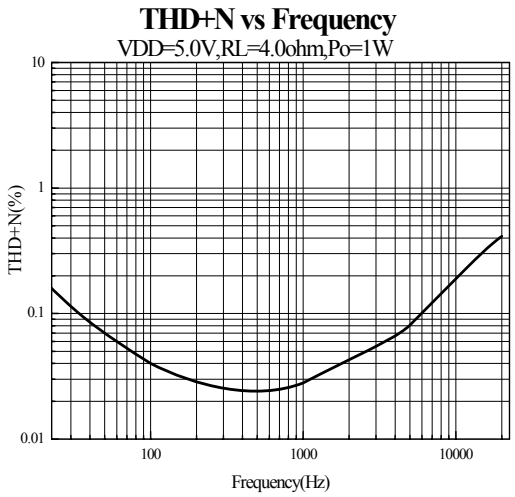
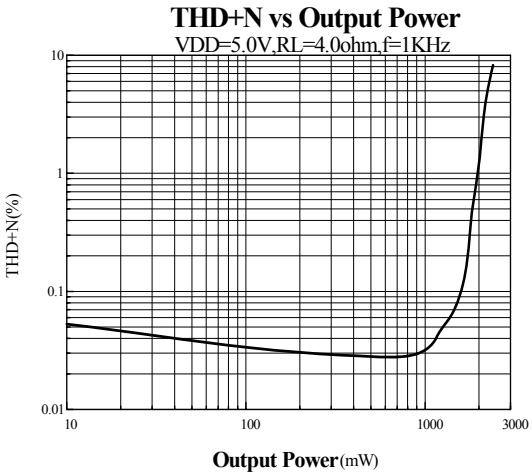


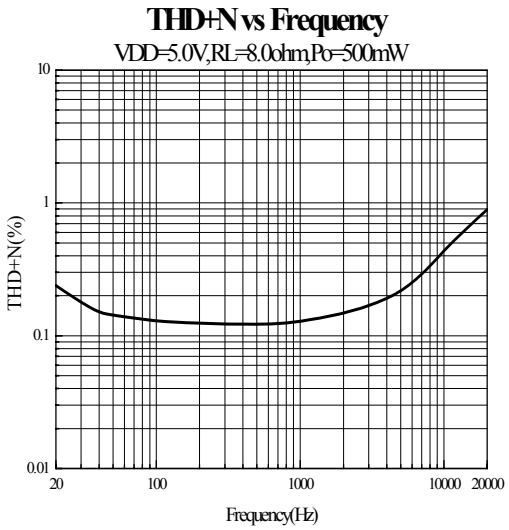
Figure 1. Typical Audio Amplifier Application Circuit.

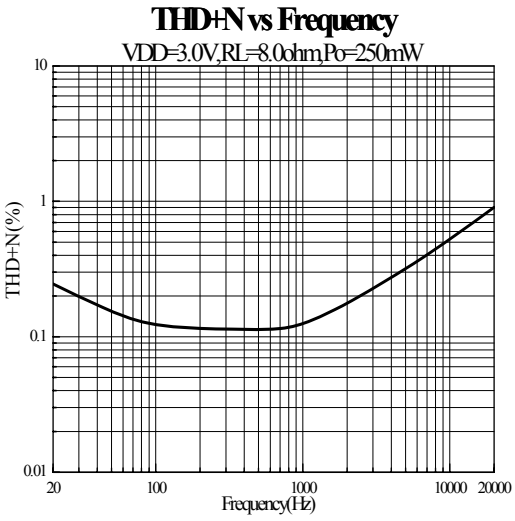
COMPONENTS		FUNCTIONAL DESCRIPTION
1	R_i	Inverting input resistor that sets the closed-loop gain together with R_F. This resistor also performs as a high pass filter with C_i at $f_C = 1/(2\pi R_i C_i)$
2	C_i	Input coupling capacitor which blocks the DC voltage at the input terminals. It also creates a high pass filter with R_i at $f_C = 1/(2\pi R_i C_i)$. For more details of how to determine the value of C_i, look at the section of **Proper Selection of External Components**.
3	R_F	Feedback resistor which sets the closed-loop gain together with R_F.
4	C_S	Supply bypass capacitor which provides supply voltage filtering. For more details of how to determine the value of C_B, refer to the section of **Power Supply Bypassing**.
5	C_B	Bypass pin capacitor which provides half-supply filtering. For more details of how to determine the value of C_B, look at the section of **Proper Selection of External Components**.

TYPICAL FERFORMANCE CHARACTERISTICS



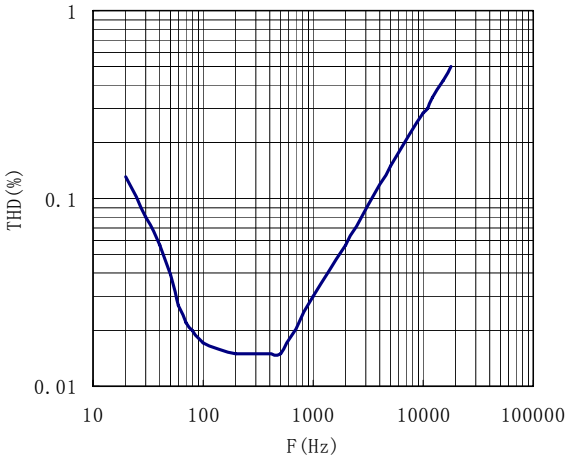




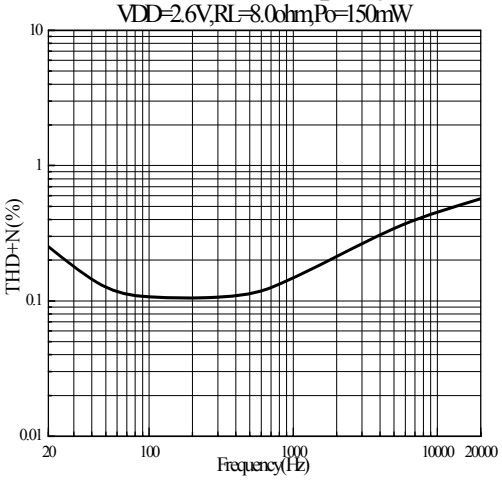


TYPICAL FERFORMANCE CHARACTERISTICS (Continued)

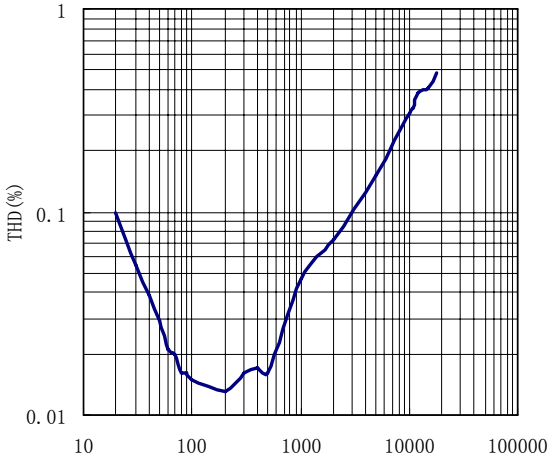
THD+N vs Frequency
VDD=3V, RL=4Ω, and Po=500mW



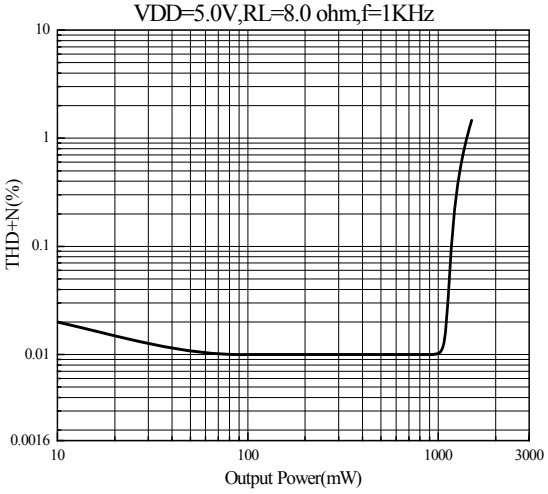
THD+N vs Frequency
VDD=2.6V,RL=8.0ohm,Po=150mW



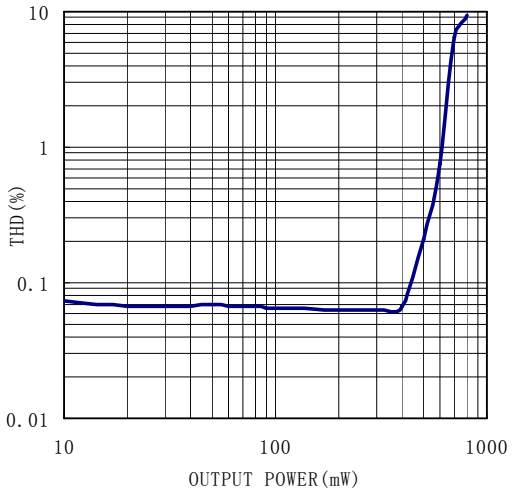
THD+N vs Frequency
VDD=2.6V, RL=4Ω, Po=150mW



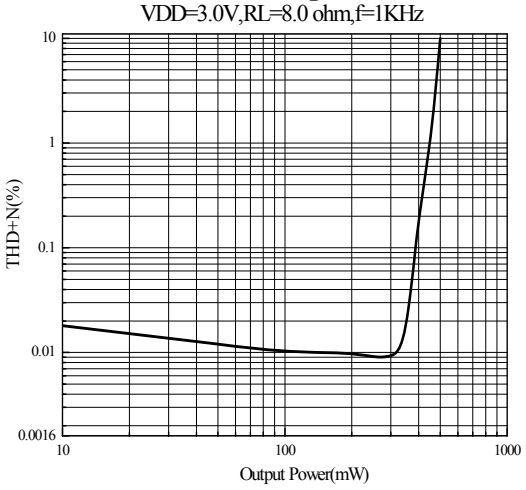
THD+N vs Output Power
VDD=5.0V,RL=8.0 ohm,f=1KHz



THD+N vs Output Power
Vdd=3V,RL=4Ω,and f=1kHz

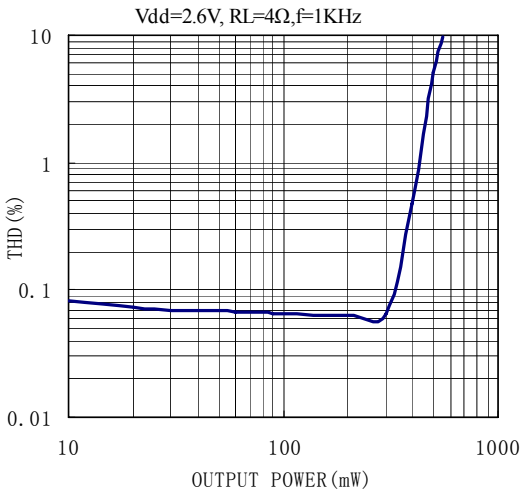


THD+N vs Output Power
VDD=3.0V,RL=8.0 ohm,f=1KHz

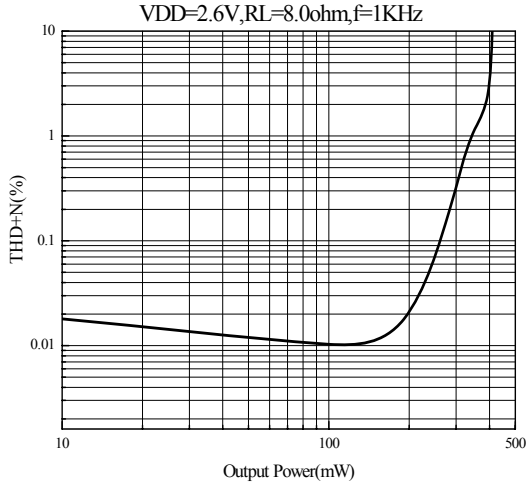


TYPICAL FERFORMANCE CHARACTERISTICS (Continued)

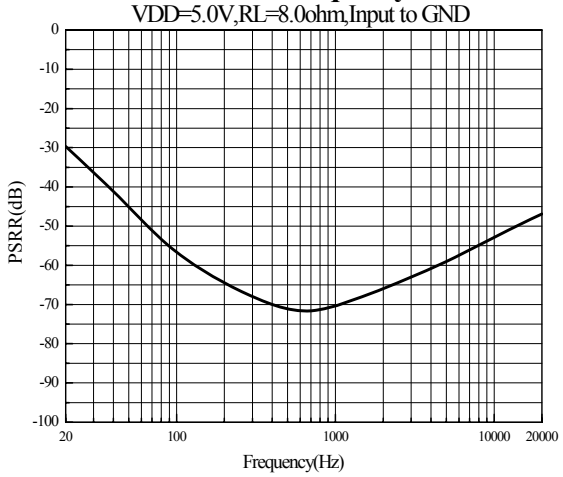
THD+N vs Ouput Power



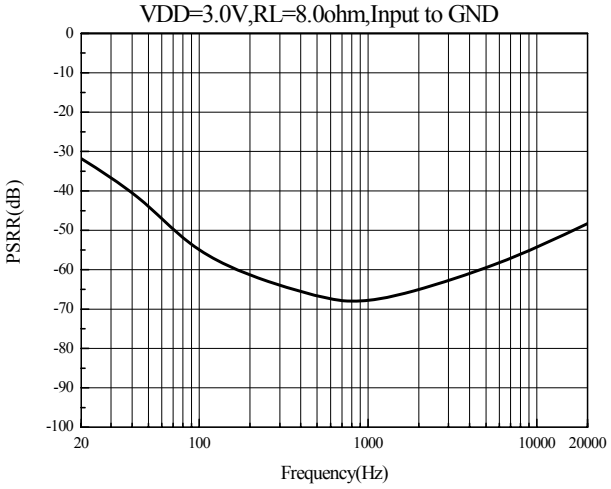
THD+N vs Output Power



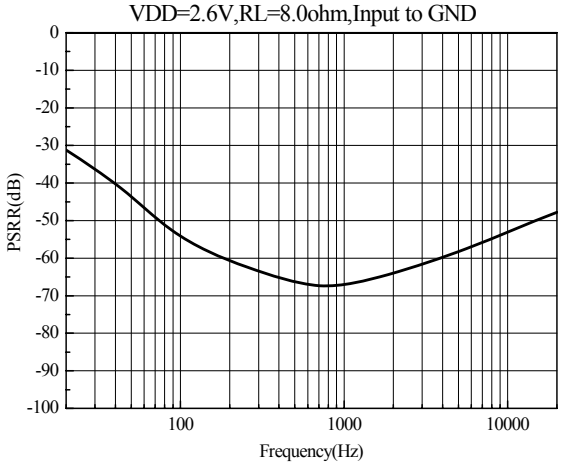
PSRR vs Frequency



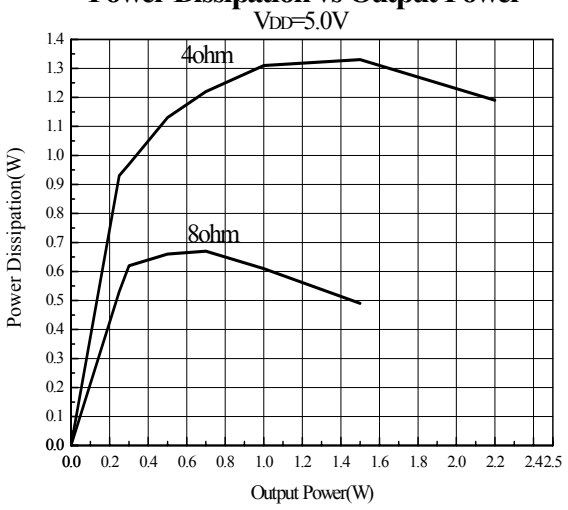
PSRR vs Frequency



PSRR vs Frequency



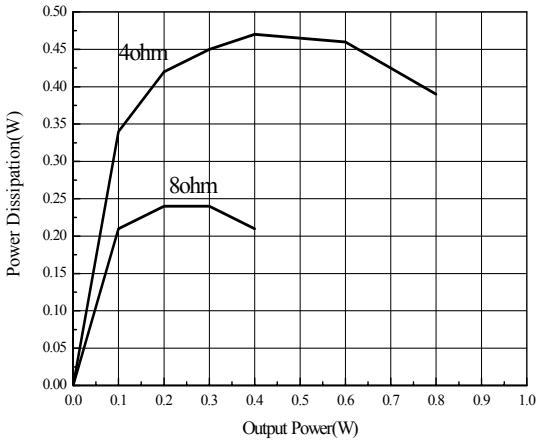
Power Dissipation vs Output Power



TYPICAL FERFORMANCE CHARACTERISTICS (Continued)

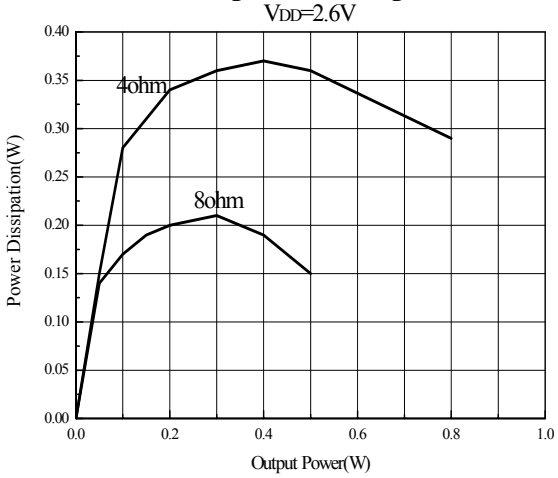
Power Dissipation vs Output Power

VDD=3.0V



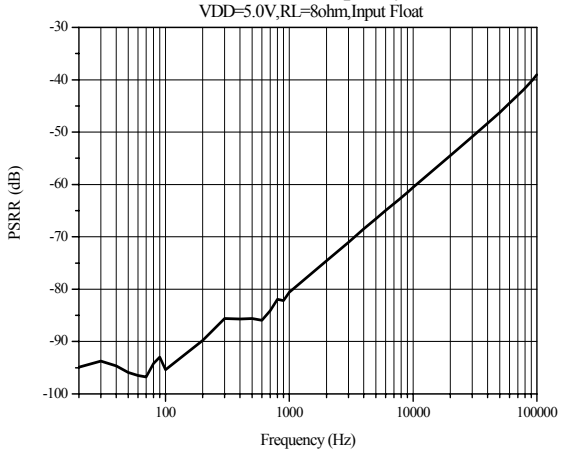
Power Dissipation vs Output Power

VDD=2.6V



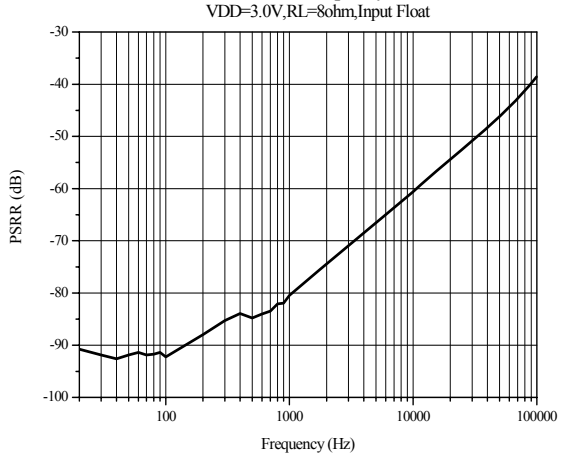
PSRR vs Frequency

VDD=5.0V,RL=8ohm,Input Float



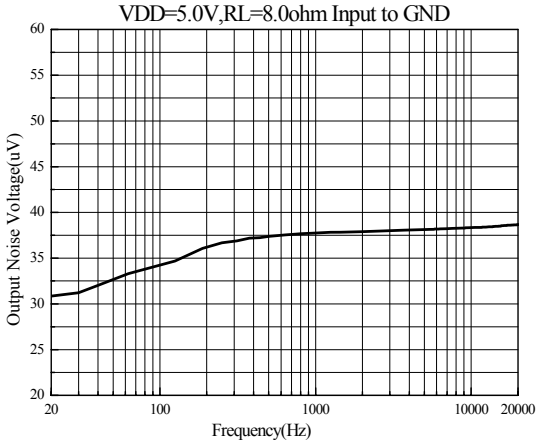
PSRR vs Frequency

VDD=3.0V,RL=8ohm,Input Float



Noise Floor

VDD=5.0V,RL=8.0ohm Input to GND



APPLICATION INFORMATION

Bridge Configuration Explanation

As shown in Figure1, the PT5301 has two internal operational amplifiers. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_F to R_i while the second amplifier's gain is fixed by the two internal 20kΩ resistors. *Figure1* shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180˚. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_F / R_i)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in PT5301, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

Power Dissipation

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the PT5301 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \qquad (1)$$

It is critical that the maximum junction temperature T_{JMAX} of 150˚C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding copper foil, the thermal resistance of the application can be reduced from the free air value of θ_{JA}, resulting in higher P_{DMAX} values without thermal shutdown protection circuitry being activated. Additional copper foil can be added to any of the leads connected to the PT5301. It is especially effective when connected to V_{DD}, GND, and the output pins. If T_{JMAX} still exceeds 150˚C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the **Typical Performance Characteristics** curves for power dissipation information for different output powers and output loading.

Power Supply Bypassing

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10μF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the PT5301. The selection of a bypass capacitor, especially C_B, is dependent upon PSRR requirements, click and pop performance (as explained in the section, **Proper Selection of External Components**), system cost, and size constraints.

Shutdown Function

In order to reduce power consumption while not in use, the PT5301 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry whenever the Shutdown pin is put at logical "low". While the device may be disabled with shutdown voltages in between ground and supply, the idle current may be greater than the typical value of 0.1μA. Therefore, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or

microprocessor output is used to control the shutdown circuitry, which provides a quick, smooth transition to shutdown. Another solution is to use a single-throw switch in conjunction with an external pull-up resistor (or pull-down, depending on shutdown high or low application). This scheme guarantees that the shutdown pin will not float, thus preventing unwanted state changes.

Proper Selection of External Components

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the PT5301 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The PT5301 is unity-gain stable which gives the designer maximum system flexibility. The PT5301 should be used in low gain configurations to minimize THD+N+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure1*. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 VDD). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the PT5301 turns on. The slower the PT5301's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), should produce a virtually pop & click free shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0µF is recommended in all but the most cost sensitive designs.

Audio Power Amplifier Design

A 1W/8Ω Audio Amplifier

Given:

Power Output	1Wrms
Load Impedance	8Ω
Input Level	1Vrms
Input Impedance	20kΩ
Bandwidth	100Hz–20kHz ± 0.25dB

5V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the PT5301 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 2.

$$A_{VD} = \sqrt{(P_O P_L)}/(V_{IN}) = V_{orms}/V_{inrms}$$
$$R_F / R_i = A_{VD}/2 \qquad (2)$$

From Equation 2, the minimum A_{VD} is 2.83; use A_{VD} =3. Since the desired input impedance was 20kΩ, and with an A_{VD} impedance of 2, a ratio of 1.5:1 of R_F to R_i results in an allocation of R_i = 20kΩ and R_F = 30kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of −3dB frequency points. Five times away from a −3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified.

f_L = 100Hz/5 = 20Hz

f_H = 20kHz×5= 100kHz

As mentioned in the **External Components** section, R_i in conjunction with C_i create a high-pass filter.

$C_i \geq 1/(2\pi \times 20k\Omega \times 20Hz) = 0.397\mu F$; use $0.39\mu F$

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With an A_{VD} = 3 and f_H = 100kHz, the resulting GBWP = 300kHz which is much smaller than the PT5301 GBWP of 2.0MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the PT5301 can still be used without running into bandwidth limitations.

The PT5301 is unity gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypass in the typical application. However, if a closed-loop gain is much greater than the normal setting value (i.e. gain = 10), a feedback capacitor (C_4) may be required as shown in Figure 2. to limit the bandwidth of the amplifier. The feedback capacitor creates a low pass filter that eliminates the possible high frequency oscillations. Be aware that an possible inadequate combination of R3 and C4 will cause roll-off before 20kHz. A typical combination is R_3 = 20kΩ and C_4 = 25pf. Users could refer this combination when design a high gain audio amplifier.

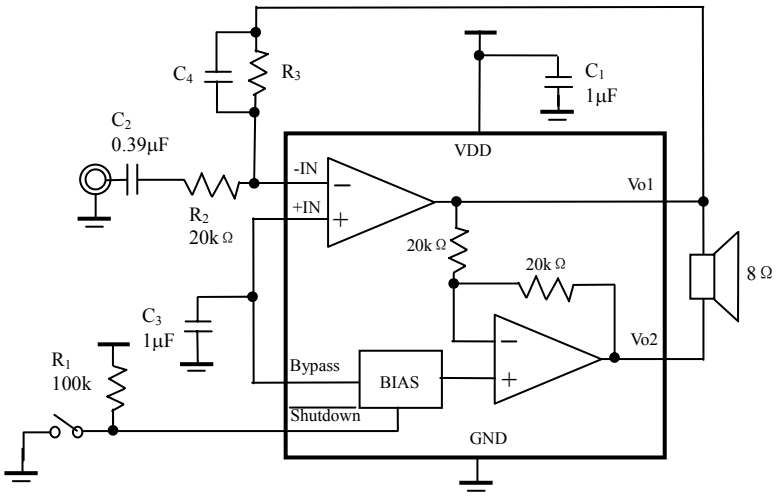


Figure 2. High Gain Audio Amplifier

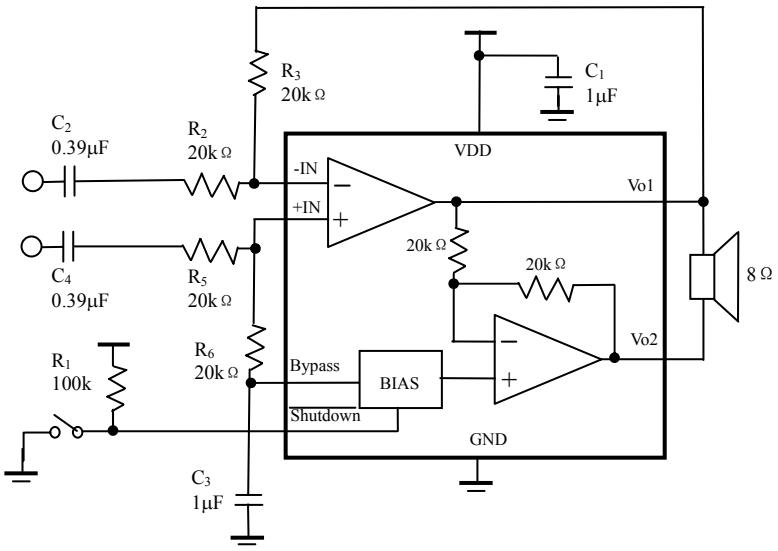


Figure 3. Fully-differential Application for PT5301

Thermal Considerations for Driving 4ΩLoad

When driving 4Ω load, the internal power dissipation of the PT5301 must be carefully considerated. Failing to optimize thermal design may compromise the PT5301's high power performance and activate unwanted, though necessary, thermal protection. In all circumstances and conditions, the junction temperature must be held below 150°C to prevent activating the PT5301's thermal protection. The maximum allowable power dissipation is limited by thermal resistance of the package. When the supply voltage is higher than 4V, the PT5301's MSOP or SMD package isn't recommended to drive 4Ω load.

The PT5301's exposed-PAD QFN package provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. The result is a low voltage audio power amplifier that produces 2W at ≤1% THD with a 4Ω load.

This high power is achieved through careful consideration of necessary thermal design. The QFN package must have its exposed-PAD soldered to a copper pad on the PCB. The exposed-PAD's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the exposed-PAD's copper pad to the inner layer or backside copper heat sink area with several vias. Ensure efficient thermal conductivity by plating through and solder-filling the vias. Best thermal performance is achieved with the largest practical copper heat sink area.

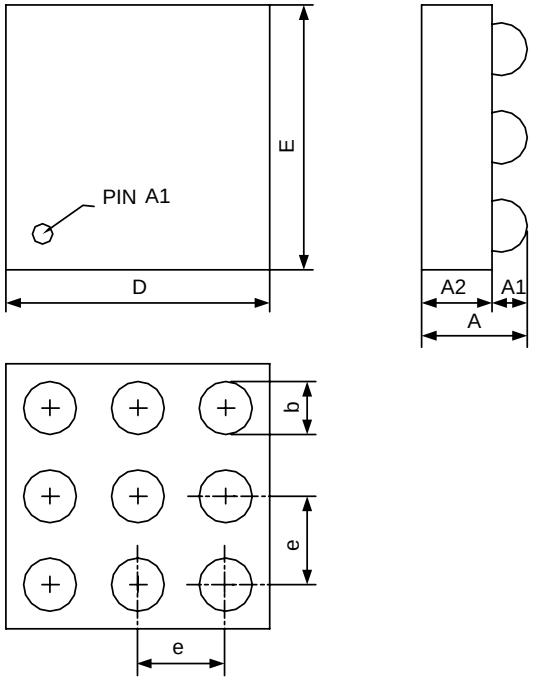
PCB Layout and Supply Regulation Considerations for Driving 4ΩLoad

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.0W to 1.9W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing

PACKAGE INFORMATION

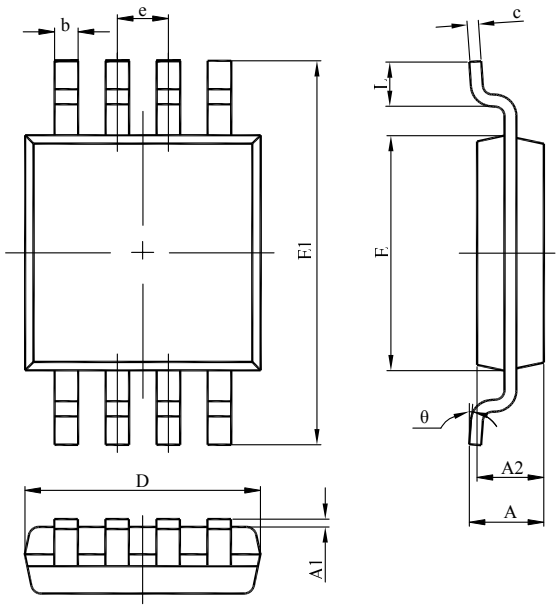
SMD9 Package



SYMBOL	MILLIMETERS	
	MIN	MAX
A	0.635	0.735
A1	0.209	0.249
A2	0.426	0.486
b	0.25	0.35
D	1.47	1.53
E	1.47	1.53
e	0.50 BSC	

PACKAGE INFORMATION

MSOP8 Package



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

PACKAGE INFORMATION

DFN8 Package