PT5322

Dual 2.2W Audio Amplifier plus Stereo Headphone Function

GENERAL DESCRIPTION

The PT5322 is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.1W to a 4Ω load or 2.4W to a 3Ω load with less than 1.0% THD+N. In addition, the headphone input pin allows the amplifiers to operate in single-ended mode when driving stereo headphones.

The PT5322 has a HP (headphone) enable input, which activates the single ended headphone mode and disables the BTL output mode. The HP_Sense input is for use with a normal stereo headphone jack.

The PT5322 features a low-power consumption shutdown mode and thermal shutdown protection. It also utilizes circuitry to reduce "pop and click" during device turn-on. The PT5322 is available in a 16 or 20 pin TSSOP package.

FEATURES

- P_O@1% THD+N:
  3Ω, 4Ω loads: 2.2W (typ), 2.0W (typ)
  8Ω load: 1.3W (typ)
- SE mode THD+N@75mW into 32Ω: 0.01%(max)
- Shutdown current: 0.7μA (typ)
- Supply voltage range: 2.5V to 5.5V
- PSRR@217Hz: 80dB (typ)
- Stereo headphone amplifier mode
- "Click and pop" suppression circuitry
- Unity-gain stable
- Thermal shutdown protection circuitry
- TSSOP and SOP packages

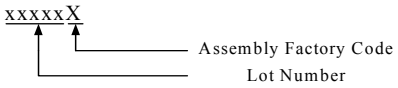
APPLICATIONS

- Cell phones
- Multimedia monitors
- Portable and desktop computers
- Portable audio systems

ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDERING PART NUMBER	TRANSPORT MEDIA	MARKING
TSSOP-16	-40 °C to +85 °C	PT5322TSOP	Tape and Reel, 3000 units	PT5322 xxxxxX
			Tube, 60 units	
SOP-16	-40 °C to +85 °C	PT5322 ESOP	Tube, 45 units	PT5322 xxxxxX

Note:



TYPICAL APPLICATION

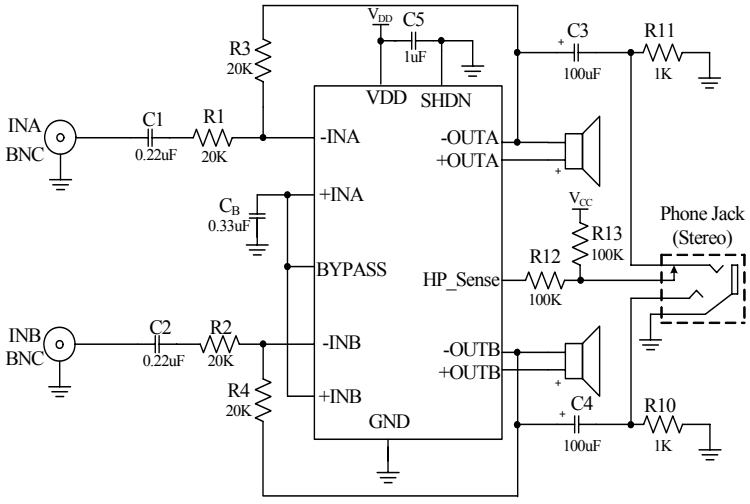
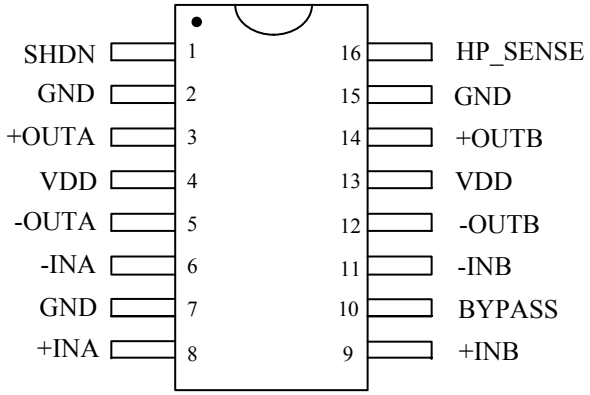


Figure 1. Typical Audio Amplifier Application Circuit

PIN ASSIGNMENT



TSSOP-16 / SOP-16

PIN DESCRIPTIONS

TSSOP-16/ SOP-16	PIN NAME	DESCRIPTION
2,7,15	GND	Ground
3	+OUTA	The non-inverting output of channel-A
4,13	VDD	Power Supply
5	-OUTA	The inverting output of channel-A
6	-INA	The inverting input of channel-A
8	+INA	The non-inverting input of channel-A
9	+INB	The non-inverting input of channel-B
11	-INB	The inverting input of channel-B
10	BYPASS	Tap to voltage divider for internal mid-supply bias supply. Connect to a 0.1uF to 1uF low ESR capacitor for best performance.
12	-OUTB	The inverting output of channel-B
14	+OUTB	The non-inverting output of channel-B
16	HP_SENSE	The HP_SENSE input is for use with a normal stereo headphone jack to select the operational output mode.
1	SHDN	Puts the device in shutdown mode when held high.

ABSOLUTE MAXIMUM RATINGS (NOTE1)

SYMBOL	PARAMETER		VALUE	UNIT
V_{DD}	Supply Voltage		6.0	V
T_{STG}	Storage Temperature		-65~+150	°C
V_{INPUT}	Input Voltage		-0.3~V_{DD}+0.3	V
P_{MAX}	Power Dissipation (Note 2)		Internally limited	W
	ESD (HBM) (Note 3)		2	KV
T_J	Junction Temperature		150	°C
T_{SOLDER}	Solder Temperature		220	°C
θ_{JA}	Thermal Resistance	TSSOP-16	105	°C/W
		SOP-16	80	

RECOMMENDED OPERATING RANGE

SYMBOL	PARAMETER	VALUE	UNIT
V_{DD}	Supply Voltage	2.5~5.5	V
T_{OPT}	Operational Temperature	-40~+85	°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Range indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Range. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through a 1.5kΩ resistor.

ELECTRICAL CHARACTERISTICS (VDD = 5V) (Note 4,5,9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		2.5		5.5	V
I_{DD}	Quiescent PowerSupply Current	V_{IN}=0, I_O=0A, BTL mode V_{IN}=0, I_O=0A, SE mode		5.5 2.6	10 6	mA
I_{SD}	Shutdown Current	V_{SHDN}=V_{DD}		0.1	1	uA
V_{IH}	Headphone Sense High Input Voltage		4	3.7		V
V_{IL}	Headphone Sense Low Input Voltage			2.6	0.8	V
V_{IHSD}	Shutdown High Input Voltage		1.4	1.2		V
V_{ILSD}	Shutdown Low Input Voltage			1	0.4	V
T_{WU}	Turn On Time	1uF Bypass Cap		200		ms

ELECTRICAL CHARACTERISTICS FOR BTL MODE OPTERATION (Note 4,5,9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Output Offset Voltage	V_{IN}=0V		5	25	mV
P_O	Output Power (Note 7, 8)	THD+N=1%, f=1KHz, R_L=3Ω THD+N=1%, f=1KHz, R_L=4Ω THD+N=1%, f=1KHz, R_L=8Ω	1.0	2.2 2.0 1.3		W
		THD+N=10%, f=1KHz, R_L=3Ω THD+N=10%, f=1KHz, R_L=4Ω THD+N=10%, f=1KHz, R_L=8Ω		2.7 2.4 1.6		
THD+N	Total Harmonic Distortion + Noise	1KHz, A_{VD}=2, R_L=4Ω, P_O=1W 1KHz, A_{VD}=2, R_L=8Ω, P_O=1W		0.10 0.06		%
PSRR	Power Supply Rejection Ratio	Input Unterminated,217Hz, V_{RIPPLE}=200mV_{p-p},C_B=1uF,R_L=8Ω		80		dB
		Input Unterminated,1KHz, V_{RIPPLE}=200mV_{p-p},C_B=1uF, R_L=8Ω		80		dB
		Input grounded, 217Hz , V_{RIPPLE}=200mV_{p-p} ,C_B=1uF, R_L=8Ω		65		dB
		Input grounded, 1KHz, V_{RIPPLE}=200mV_{p-p} ,C_B=1uF, R_L=8Ω		65		dB
X_{TALK}	Channel Separation	f=1KHz, CB=1uF		80		dB
V_{NO}	Output Noise Voltage	1KHz, A-weighted		20		uV

ELECTRICAL CHARACTERISTICS FOR SINGLE-ENDED MODE OPERATION (Note 4,5,9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output Power (Note 7)	THD+N=0.05%, f=1KHz, R_L=32Ω	75	85		mW
THD+N	Total Harmonic Distortion + Noise	1KHz, R_L=32Ω, P_O=20mW		0.02		%
PSRR	Power Supply Rejection Ratio	Input Unterminated,217Hz, V_{RIPPLE}=200mV_{p-p},C_B=1uF, R_L=32Ω		70		dB
		Input Unterminated,1KHz, V_{RIPPLE}=200mV_{p-p},C_B=1uF, R_L=32Ω		72		dB
		Input grounded, 217Hz, V_{RIPPLE}=200mV_{p-p} ,C_B=1uF, R_L=32Ω		65		dB
		Input grounded, 1KHz, V_{RIPPLE}=200mV_{p-p} ,C_B=1uF, R_L=32Ω		70		dB
X_{TALK}	Channel Separation	f=1KHz, CB=1uF, 3D_Control = Low		75		dB
V_{NO}	Output Noise Voltage	1KHz, A-weighted		10		uV

ELECTRICAL CHARACTERISTICS (VDD = 3V) (Note 4,5,9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Quiescent Power Supply Current	V_{IN}=0, I_O=0A, BTL mode V_{IN}=0, I_O=0A, SE mode		4.5 2.5		mA
I_{SD}	Shutdown Current	V_{SHDN}=V_{DD}		0.1	1	uA
V_{IH}	Headphone Sense High Input Voltage			2.2		V
V_{IL}	Headphone Sense Low Input Voltage			1.5		V
V_{IHSD}	Shutdown High Input Voltage		1.4	1		V
V_{ILSD}	Shutdown Low Input Voltage			0.8	0.4	V
T_{WU}	Turn On Time	1uF Bypass Cap		200		ms

ELECTRICAL CHARACTERISTICS FOR BTL MODE OPERATION (Note 4,5,9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Output Offset Voltage	V_{IN}=0V		5		mV
P_O	Output Power (Note 7, 8)	THD+N=1%, f=1KHz, R_L=3Ω THD+N=1%, f=1KHz, R_L=4Ω THD+N=1%, f=1KHz, R_L=8Ω		0.82 0.70 0.43		W
		THD+N=10%, f=1KHz, R_L=3Ω THD+N=10%, f=1KHz, R_L=4Ω THD+N=10%, f=1KHz, R_L=8Ω		1.0 0.85 0.53		
THD+N	Total Harmonic Distortion + Noise	1KHz, R_L=4Ω, P_O=280mW 1KHz, R_L=8Ω, P_O=200mW		0.10 0.05		%
PSRR	Power Supply Rejection Ratio	Input Unterminated,217Hz, V_{RIPPLE}=200mV_{p-p},C_B=1uF, R_L=8Ω		80		dB
		Input Unterminated,1KHz, V_{RIPPLE}=200mV_{p-p},C_B=1uF, R_L=8Ω		80		dB
		Input grounded, 217Hz,V_{ripple}=200mV_{p-p}, C_B=1uF, R_L=8Ω		65		dB
		Input grounded, 1KHz, V_{RIPPLE}=200mV_{p-p}, C_B=1uF, R_L=8Ω		70		dB
X_{TALK}	Channel Separation	f=1KHz, CB=1uF, 3D_Control = Low		80		dB
V_{NO}	Output Noise Voltage	1KHz, A-weighted		20		uV

ELECTRICAL CHARACTERISTICS FOR SINGLE-ENDED MODE OPERATION

(Note 4,5,9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output Power (Note 7)	THD+N=0.05%, f=1KHz, R_L=32Ω		35		mW
THD+N	Total Harmonic Distortion + Noise	1KHz, R_L=32Ω, P_O=20mW		0.02		%
PSRR	Power Supply Rejection Ratio	Input Unterminated,217Hz, V_{RIPPLE}=200mV_{p-p},C_B=1uF, R_L=32Ω		71		dB
		Input Unterminated,1KHz, V_{RIPPLE}=200mV_{p-p} ,C_B=1uF, R_L=32Ω		72		dB
		Input grounded, 217Hz, V_{RIPPLE}=200mV_{p-p} ,C_B=1uF, R_L=32Ω		65		dB
		Input grounded, 1KHz, V_{RIPPLE}=200mV_{p-p} , C_B=1uF, R_L=32Ω		72		dB
X_{TALK}	Channel Separation	f=1KHz, CB=1uF, 3D_Control = Low		75		dB
V_{NO}	Output Noise Voltage	1KHz, A-weighted		10		uV

Note 4: Typicals are measured at 25˚C and represent the parametric norm.

Note 5: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

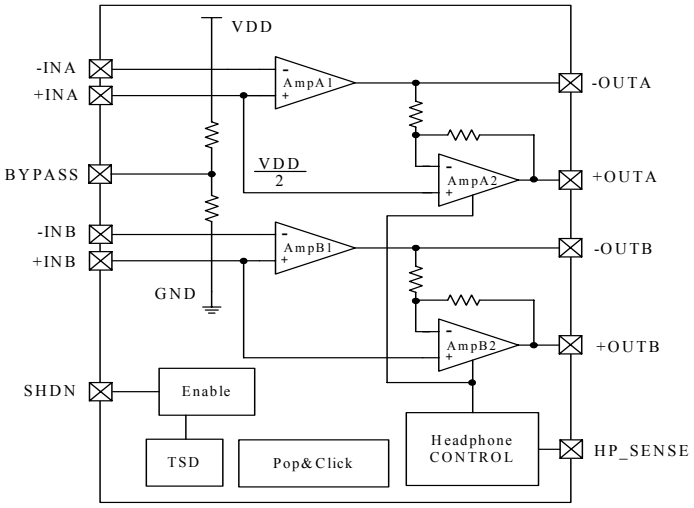
Note 6: The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.

Note 7: Output power is measured at the device terminals.

Note 8: When driving 3Ω or 4Ω loads and operating on a 5V supply, the θ_{JA} of PT5322 must be below 150 °C

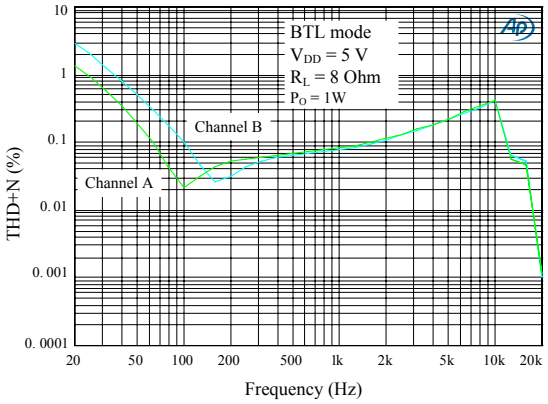
Note 9: All measurements taken from Applications Diagram (*Figure 1*).

SIMPLIFIED BLOCK DIAGRAM

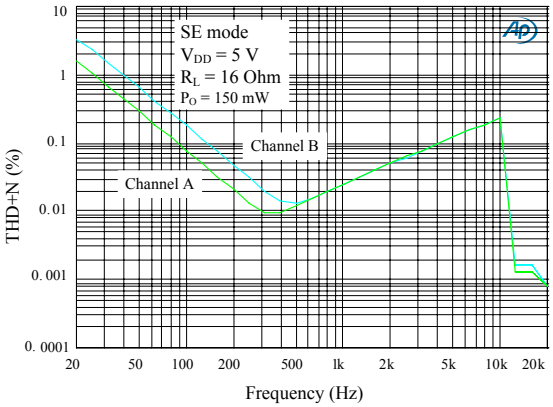


TYPICAL PERFORMANCE CHARACTERISTICS

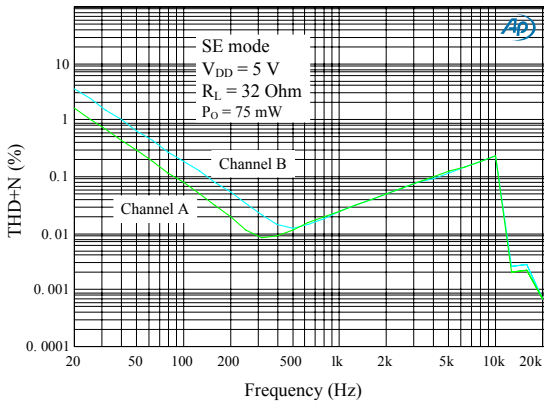
THD+N vs. Frequency



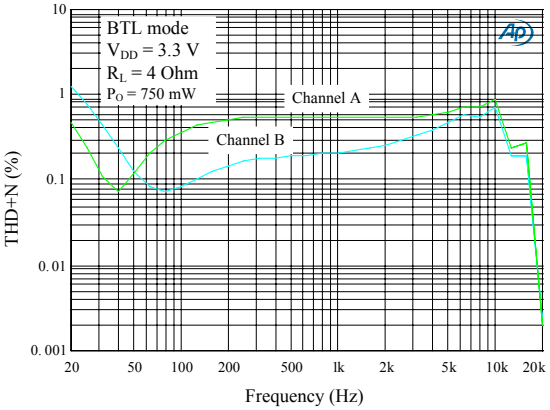
THD+N vs. Frequency



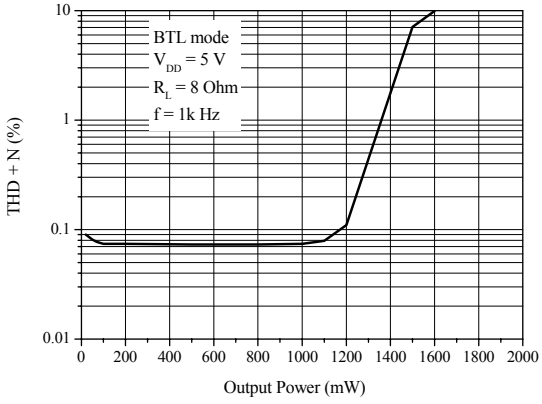
THD+N vs. Frequency



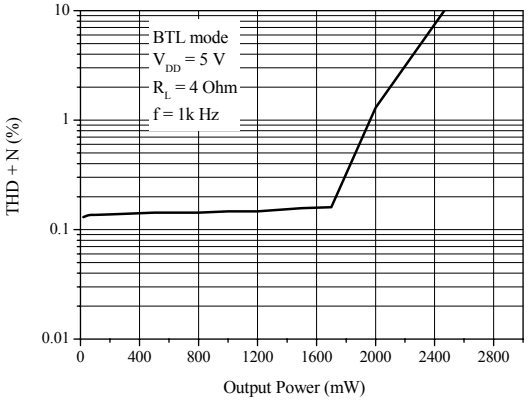
THD+N vs. Frequency



THD+N vs. Output Power

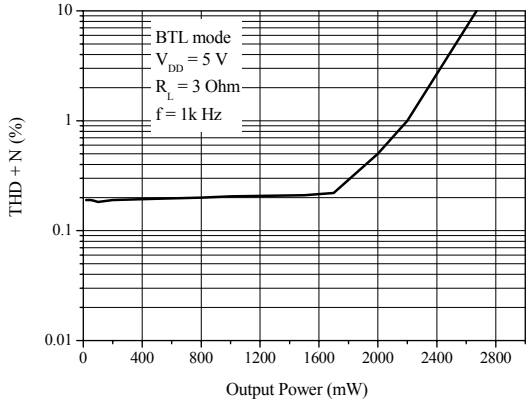


THD+N vs. Output Power

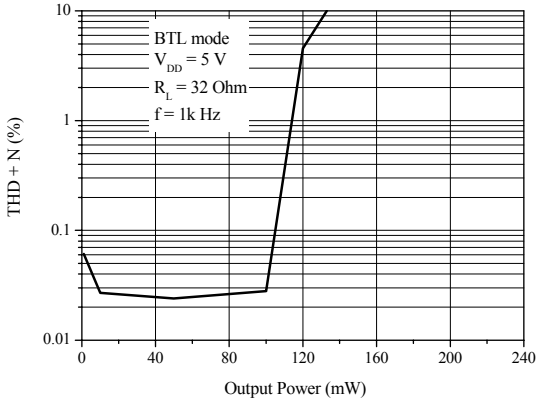


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

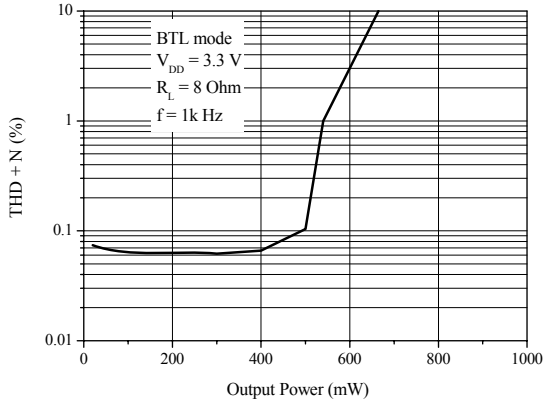
THD+N vs. Output Power



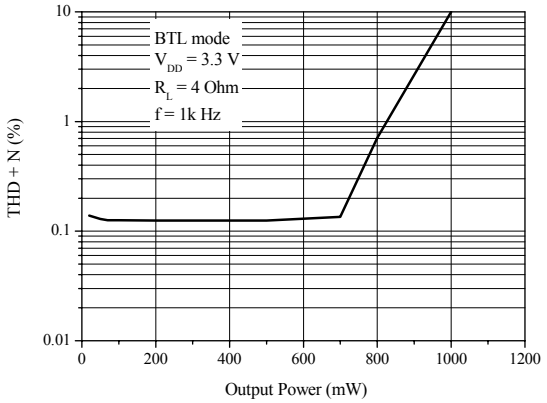
THD+N vs. Output Power



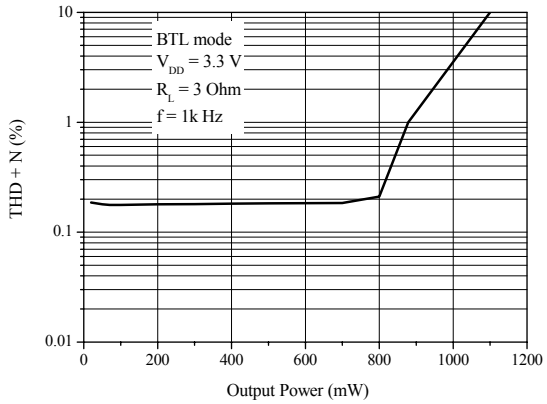
THD+N vs. Output Power



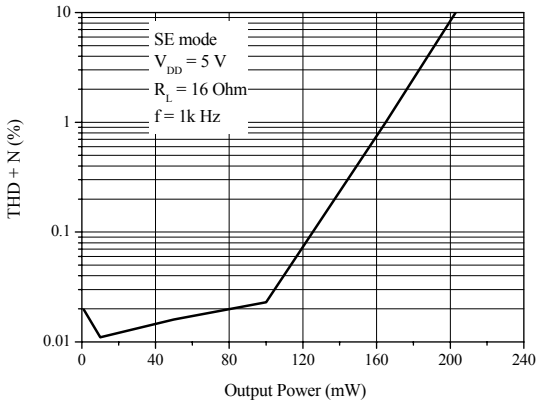
THD+N vs. Output Power



THD+N vs. Output Power

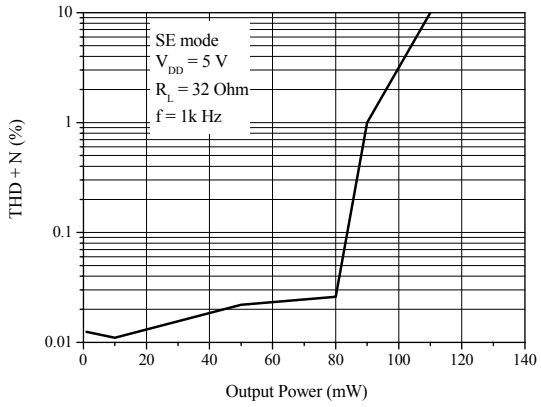


THD+N vs. Output Power

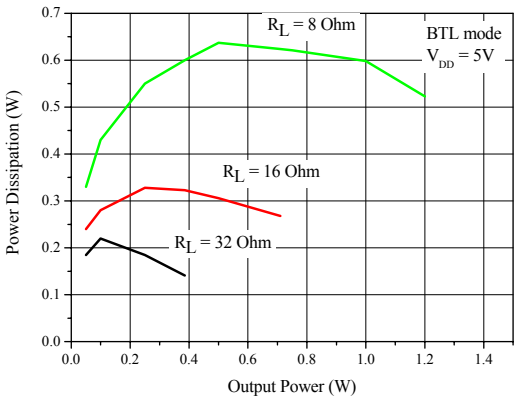


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

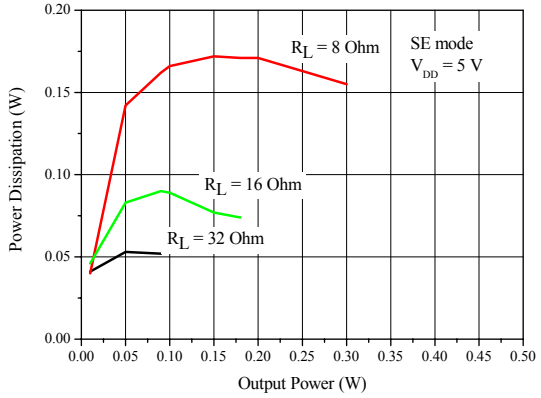
THD+N vs. Output Power



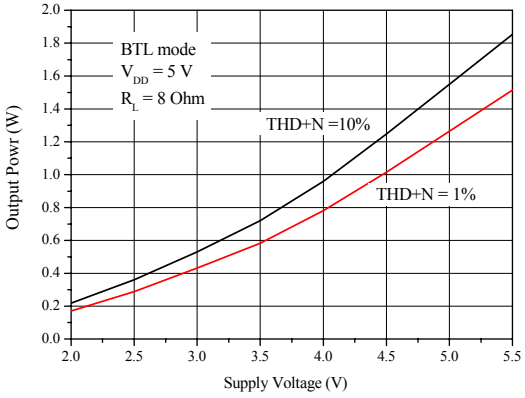
Power Dissipation vs. Output Power



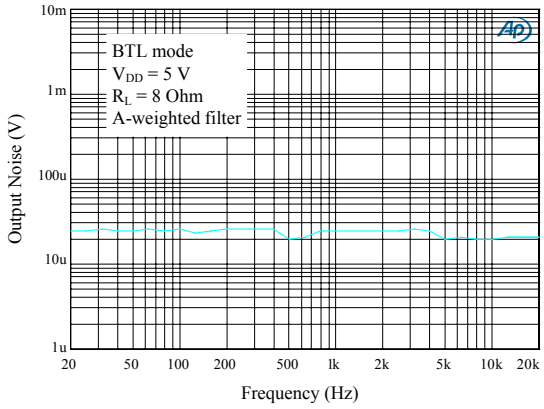
Power Dissipation vs. Output Power



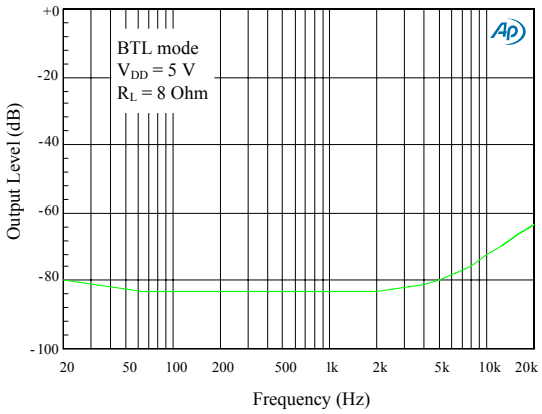
Output Power vs. Supply Voltage



Noise Floor

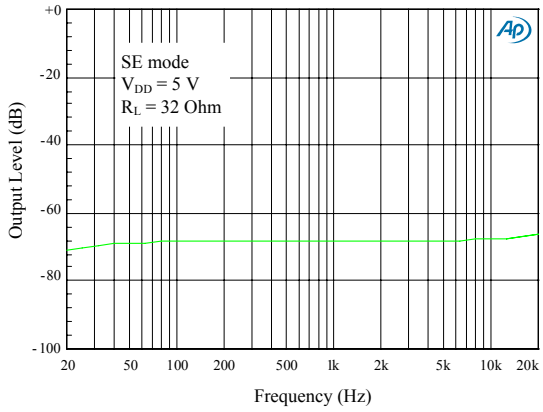


Crosstalk vs. Frequency

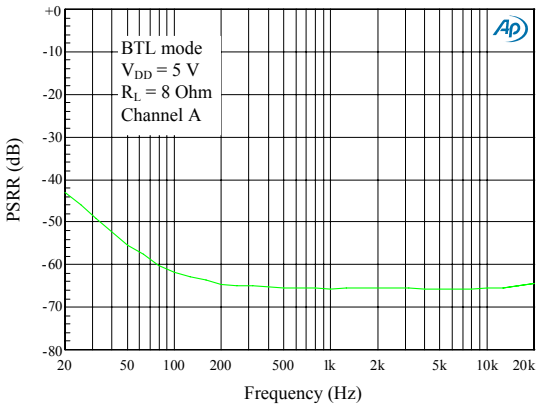


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

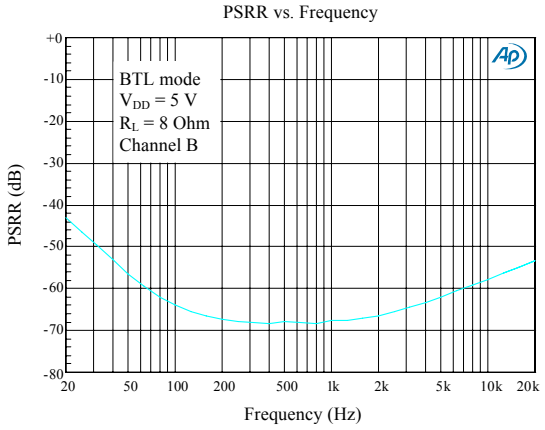
Crosstalk vs. Frequency



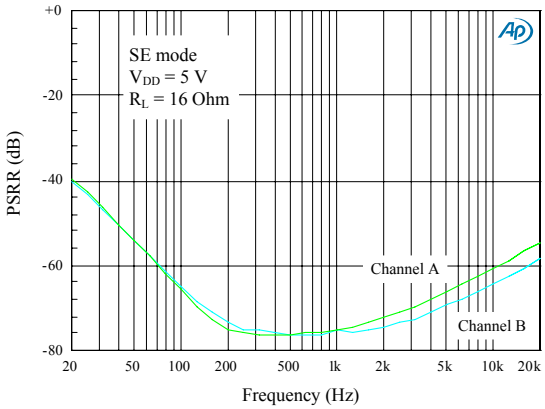
PSRR vs. Frequency



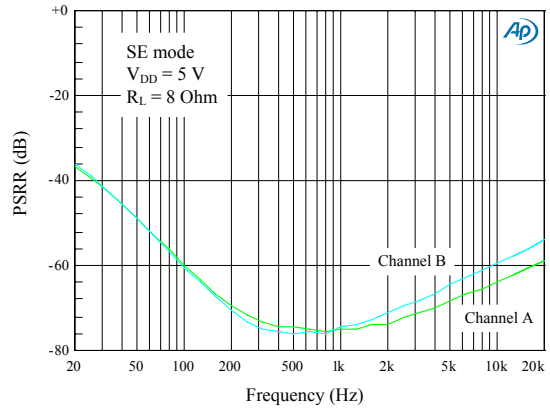
PSRR vs. Frequency



PSRR vs. Frequency



PSRR vs. Frequency



APPLICATION INFORMATION

Bridge Configuration Explanation

As shown in Figure1, the PT5322 has two internal operational amplifiers per channel. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure1shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180˚. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_f/Ri)$$

or

$$A_{VD} = 2 * (R3/R1) \quad (1)$$

or

$$A_{VD} = 2 * (R4/R2)$$

By driving the load differentially through outputs +OUTA and –OUTA (or +OUTB, -OUTB), an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in PT5322, also creates a second advantage over single-ended amplifiers. Since the differential outputs, +OUTA and –OUTA (or +OUTB, -OUTB), are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

Power Dissipation

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. Equation (2) states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \quad \text{Single-Ended} \quad (2)$$

A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the PT5322 has two operational amplifiers per channel in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 3.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad \text{Bridge Mode} \quad (3)$$

The PT5322's power dissipation is twice that given by Equation (2) or Equation (3) when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$P_{DMAX}' = (T_{JMAX} - T_A)/\theta_{JA} \quad (4)$$

The PT5322's T_{JMAX} = 150°C. The θ_{JA} of PT5322 in the TSSOP-16 package is 105°C/W, and the θ_{JA} of PT5322 in the SOP-16 package is 80°C/W. At any given ambient temperature T_A, use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (4) and substituting P_{DMAX} for P_{DMAX}' results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the PT5322's maximum junction temperature.

$$T_A = T_{JMAX} - 2*P_{DMAX} *\theta_{JA} \quad (5)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 84°C or 100°C for the TSSOP-16 or SOP-16 package

respectively.

$$T_{JMAX} = P_{DMAX} * \theta_{JA} + T_A \qquad (6)$$

Equation (6) gives the maximum junction temperature T_{JMAX}. If the result violates the PT5322's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures. The above examples assume that a device is a surface mount part operating around the maximum power dissipation point.

Since internal power dissipation is a function of outut power, higher ambient temperatures are allowed as output power decreases. If the result of Equation (2) and Equation (3) is greater than that of Equation (4), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}.

Power Supply Bypassing

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. However, their presence does not eliminate the need for bypassing the supply nodes of the PT5322. The selection of a bypass capacitor, especially C_B, is dependent upon PSRR requirements, click and pop performance (as explained in the section, **Proper Selection of External Components**), system cost, and size constraints.

Shutdown Function

In order to reduce power consumption while not in use, the PT5322 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry whenever the Shutdown pin is put at logical "high". While the device may be disabled with shutdown voltages in between ground and supply, the idle current may be greater than the typical value of 0.1µA. Therefore, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry, which provides a quick, smooth transition to shutdown. Another solution is to use a single-throw switch in conjunction with an external pull-up resistor (or pull-down, depending on shutdown high or low application). This scheme guarantees that the shutdown pin will not float, thus preventing unwanted state changes.

Table 1. Logic Level Truth Table

SHDN PIN	HP_Sense PIN	Operational Mode
Low	High	Single-Ended amplifiers
Low	Low	Bridged amplifiers
High	Don't Care	Shutdown

Headphone Logic in Functions

Applying a logic level to the PT5322's HP_Sense headphone control pin turns off AmpA2 (+OUTA) and AmpB2 (+OUTB) muting a bridged-connected load. Quiescent current consumption is reduced when the IC is in this single-ended mode.

Figure 2 shows the implementation of the

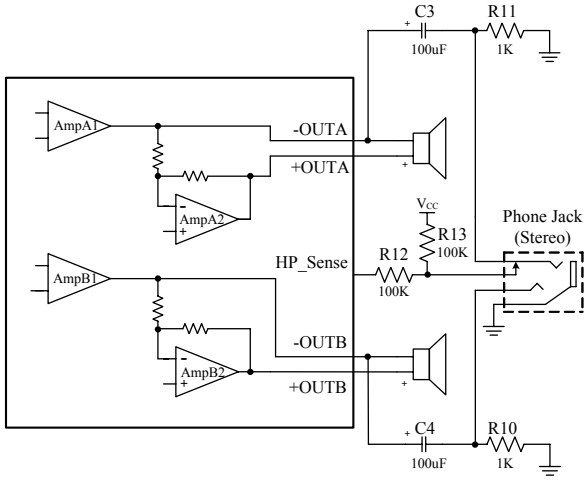


Figure 2. Headphone Circuit

PT5322's headphone control function. With no headphones connected to the headphone jack, the R11-R13 voltage divider sets the voltage applied to the HP_Sense pin (pin 20) at approximately 50mV. This 50mV enables AmpA2 (+OUTA) and AmpB2 (+OUTB) placing the PT5322 in bridged mode operation. While the PT5322 operates in bridged mode, the DC potential across the load is essentially 0V. Therefore, even in an ideal situation, the output swing cannot cause a false single-ended trigger. Connecting headphones to the headphone jack disconnects the headphone jack contact pin from −OUTA and allows R13 to pull the HP_Sense

pin up to VDD. This enables the headphone function, turns off AmpA2 (+OUTA) and AmpB2 (+OUTB) which mutes the bridged speaker. The amplifier then drives the headphones, whose impedance is in parallel with resistors R10 and R11. These resistors have negligible effect on the PT5322's output drive capability since the typical impedance of headphones is 32Ω. *Figure 2* also shows the suggested headphone jack electrical connections. The jack is designed to mate with a three wire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve should carry the ground return. A headphone jack with one control pin contact is sufficient to drive the HP Sense pin when connecting headphones.

Proper Selection of External Components

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the PT5322 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The PT5322 is unity-gain stable which gives the designer maximum system flexibility. The PT5322 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection.

Input Capacitor Value Selection

Besides gain, one of the major considerations is the closed loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure1*. The input resistors (R1, R2) coupling capacitor, C_i (C1, C2), forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance. Equation (7) states the -3dB cutoff frequency of the input high pass filter.

$$f_{-3dB} = \frac{1}{2\pi RiCi} = \frac{1}{2\pi R1C1} \qquad (7)$$

In addition to system cost and size, click and pop performance is affected by the size of the input coupling capacitor, C_i (C1, C2). A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally $V_{DD}/2$). The amplifier's output charges the input capacitor through the feedback resistors, R2 and R8. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the PT5322 turns on. The slower the PT5322's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), should produce a virtually pop&click free shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0µF is recommended in all but the most cost sensitive designs.

Audio Power Amplifier Design

A 1W/8Ω Audio Amplifier

Given:

Power Output:	$1W_{rms}$
Load Impedance:	8Ω
Input Level:	$1V_{rms}$
Input Impedance:	20kΩ
Bandwidth:	100Hz–20kHz ± 0.25dB

5V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the PT5322 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power**

Dissipation section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 8.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \qquad (8)$$

From Equation 8, the minimum A_{VD} is 2.83. For this example, let A_{VD} =3. The amplifier's overall gain is set using the input (R1 and R2) and feedback resistors R3 and R4.

$$R_f / R_i = R3 / R1 = R4 / R2 = A_{VD} / 2 \qquad (9)$$

Since the desired input impedance was 20kΩ, with a ratio of 1.5:1 of R_f to R_i results in an allocation of R_i = 20kΩ and R_f = 30kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of −3dB frequency points. Five times away from a −3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified.

f_L = 100Hz/5 = 20Hz

and

f_H = 20kHz×5= 100kHz

As mentioned in the **External Components** section, R_i in conjunction with C_i create a high-pass filter. Find the coupling capacitor's value using Equation (10).

$$C_i \geq 1/(2\pi R_1 f_L) \qquad (10)$$

This result is

$$Ci \geq 1/(2\pi * 20k\Omega * 20Hz) = 0.397\mu F$$

Use a 0.39µF capacitor, the closest standard value.
The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With an A_{VD} = 3 and f_H = 100k Hz, the resulting the closed-loop gain bandwidth product (GBWP) is 300k Hz which is much smaller than the PT5322's GBWP.

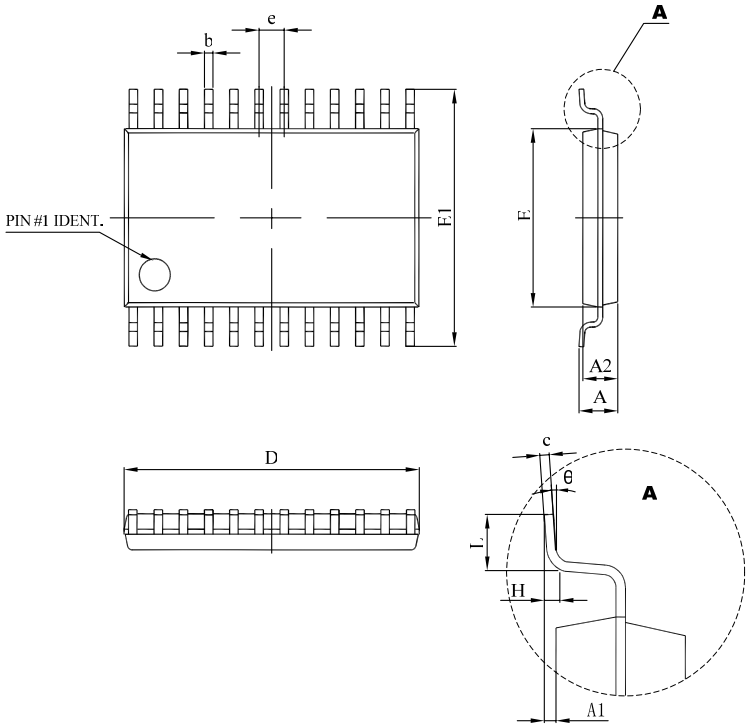
PCB Layout and Supply Regulation Considerations for Driving 3Ωand 4ΩLoads

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.1W to 2.0W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

PACKAGE INFORMATION

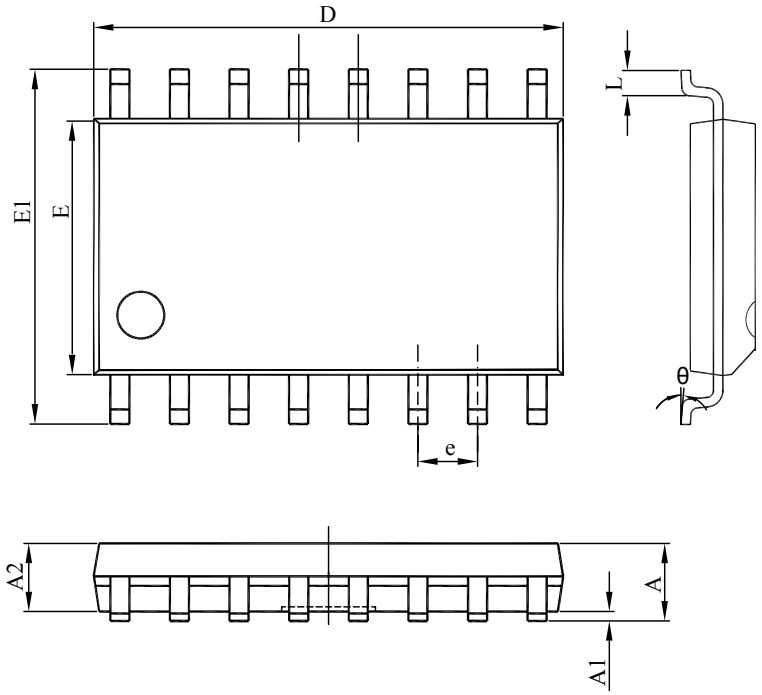
TSSOP-16



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65		0.026	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

PACKAGE INFORMATION

SOP-16



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.30	2.70	0.090	0.106
A1	0.10	0.30	0.004	0.012
A2	2.10	2.50	0.083	0.099
D	10.10	10.50	0.398	0.414
E	7.30	7.70	0.287	0.303
E1	10.10	10.50	0.398	0.414
e	1.27 TYP.		0.050 TYP.	
L	0.60	0.80	0.0236	0.0316
θ	0°	7°	0°	7°