PT6111

Analog Front End for 3~8 cells Battery Monitoring and Balancing

GENERAL DESCRIPTION

PT6111 is a highly integrated battery charge/discharge and balancing management analog front end which support 3 to 7 cells serially connected Li-ion, Li-polymer or 3 to 8 cells serially $LiFePO_4$ battery pack. It is applicable in cordless electrical tools, vacuum cleaner or other multi-cell battery powered systems. PT6111 use a high precision amplifier to buffer each battery cell voltage to an analog output pin. All output voltages are alternatively selected by the co-working MCU and digitized by the ADC within that MCU. The integrated battery balance circuitry in the PT6111 provides a shunt current of 50mA without the need of any external transistors. The chip also includes important features such as an integrated LDO which power for an external MCU, charge and discharge power MOSFETs driver

PT6111 works together with an MCU performs battery safety protections against battery over-voltage, under-voltage and cell balancing. PT6111 is available in QFN-24(4x4) package.

FEATURES

- Battery Voltage Sample and Buffer
  - ✧ 8 channels for cell voltage measurements
  - ✧ High-precision cell voltage detection: ±15mV @4.2V
  - ✧ 1:1 buffer for cell voltage output
- Integrated Charge and Discharge MOSFET driver
- Integrated 50mA cell balance driver
- Integrated 5V LDO for external MCU: >45mA
- Internal thermal shutdown (TSD)
- Low power consumption in sleep mode: <12μA (EN=0)

APPLICATIONS

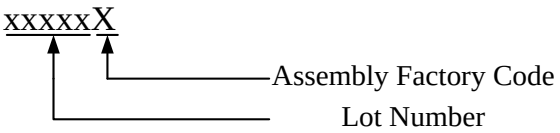
- Vacuum cleaner
- Power tools
- Multi-cell battery pack in portable devices

ORDERING INFORMATION

原厂技术支持：联系人：徐俐湘　联系电话：18565820880

PACKAGE	TEMPERATURERANGE	ORDERING PART NUMBER	TRANSPORT MEDIA	MARKING
QFN-24	-40°C to 85°C	PT6111EQFN	Tape and Reel 5000 units	PT6111 xxxxxX

Note:



TYPICAL APPLICATION EXAMPLE

原厂技术支持：联系人：徐俐湘　　联系电话：18565820880

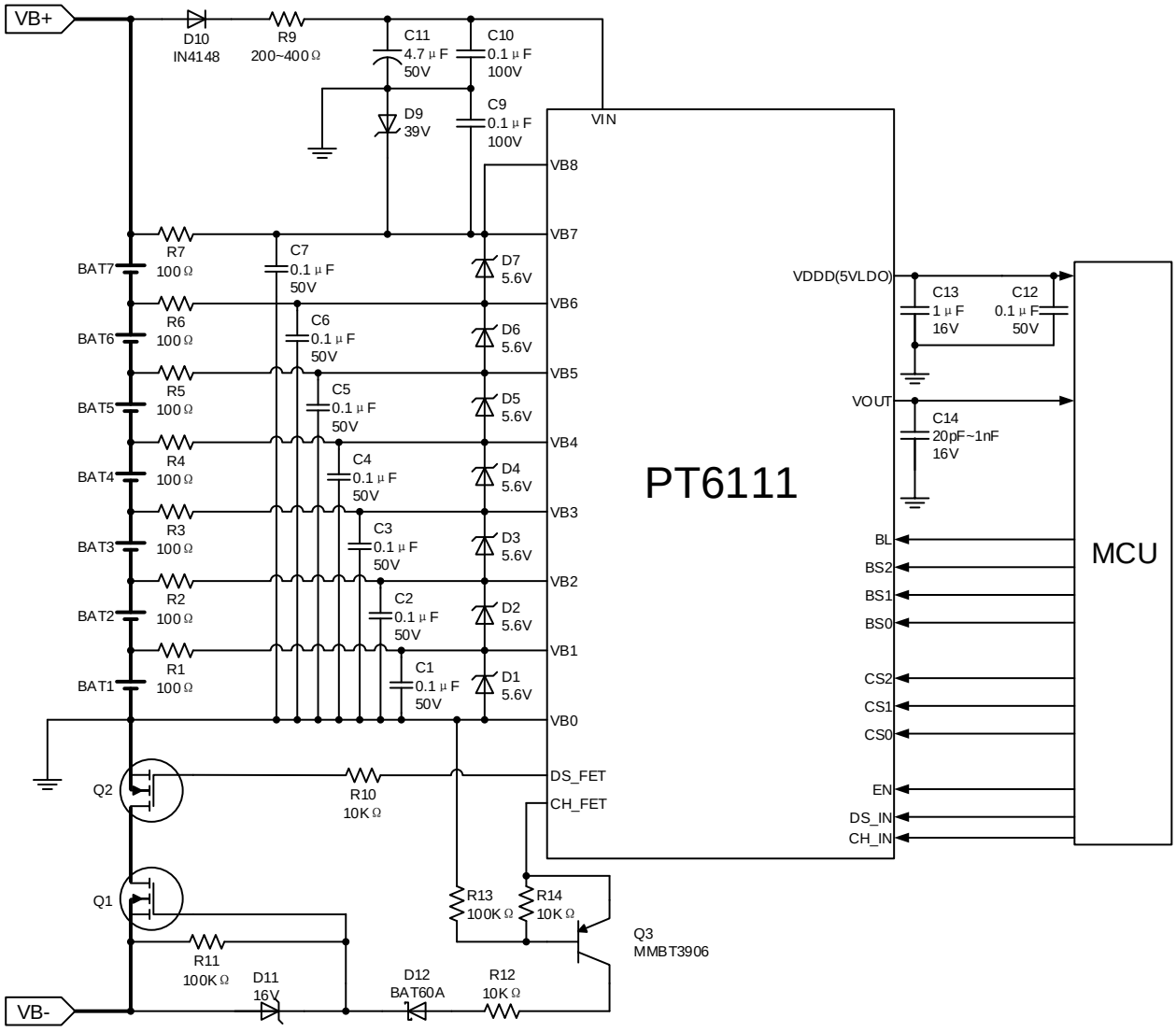
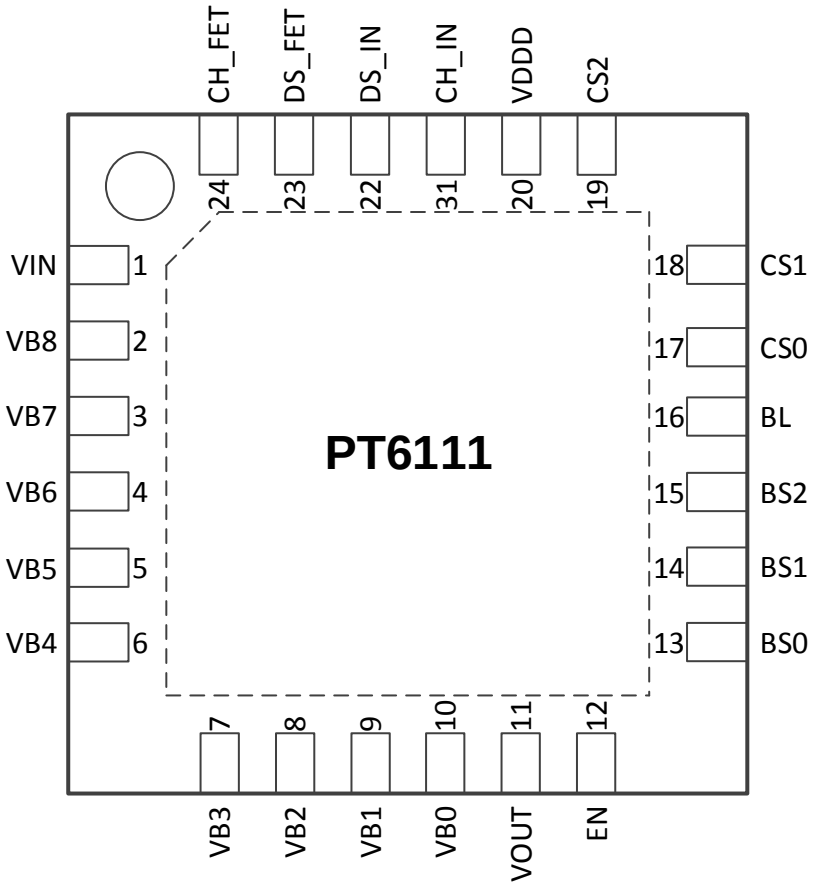


Figure 1. Typical application of PT6111 for 7 cells Li-ion battery

PIN ASSIGNMENT

原厂技术支持：联系人：徐俐湘　联系电话：18565820880



QFN-24

PIN DESCRIPTION

Pin #(QFN-24)	Name	Description
1	VIN	Power supply
2	VB8	Positive input Battery cell 8
3	VB7	Negative input Battery cell 8, Positive input Battery cell 7
4	VB6	Negative input Battery cell 7, Positive input Battery cell 6
5	VB5	Negative input Battery cell 6, Positive input Battery cell 5
6	VB4	Negative input Battery cell 5, Positive input Battery cell 4
7	VB3	Negative input Battery cell 4, Positive input Battery cell 3
8	VB2	Negative input Battery cell 3, Positive input Battery cell 2
9	VB1	Negative input Battery cell 2, Positive input Battery cell 1
10	VB0	Negative input Battery cell 1, ground
11	VOUT	Battery voltage buffer output
12	EN	Enable/Sleep the chip; EN=1, enable the chip; EN=0, sleep
13	BS0	Balance Select: BS2,BS1,BS0=000, 1st (lowest) battery cell; BS2,BS1,BS0=001, 2nd battery cell; BS2,BS1,BS0=010, 3rd battery cell; BS2,BS1,BS0=011, 4th battery cell; BS2,BS1,BS0=100, 5th battery cell; BS2,BS1,BS0=101, 6th battery cell; BS2,BS1,BS0=110, 7th battery cell; BS2,BS1,BS0=111, 8th battery cell;
14	BS1	
15	BS2	
16	BL	Enable/disable the balance current; BL=1, Balance enable
17	CS0	Cell Select: CS2,CS1,CS0=000, 1st (lowest) battery cell; CS2,CS1,CS0=001, 2nd battery cell; CS2,CS1,CS0=010, 3rd battery cell; CS2,CS1,CS0=011, 4th battery cell; CS2,CS1,CS0=100, 5th battery cell; CS2,CS1,CS0=101, 6th battery cell; CS2,CS1,CS0=110, 7th battery cell; CS2,CS1,CS0=111, 8th battery cell;
18	CS1	
19	CS2	
20	VDDD	5V LDO output
21	CH_IN	Charge control input
22	DS_IN	Discharge control input
23	DS_FET	Discharge MOSFET driver controlled by DS_IN (DS_IN=1, DS_FET out high; DS_IN=0, DS_FET output low)
24	CH_FET	Charge MOSFET Driver controlled by CH_IN (CH_IN=1, CH_FET source current; CH_IN=0, high impedance)
PAD		Thermal Pad, Connect to GND.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEMS	VALUE	UNIT
V_{IN}	Power Supply Voltage (V_{IN}-VB0)	-0.5 to 40	V
VB1	VB1 to VB0	-0.5 to 6	V
VB2	VB2 to VB0	-0.5 to 12	V
VB3	VB3 to VB0	-0.5 to 18	V
VB4	VB4 to VB0	-0.5 to 25	V
VB5	VB5 to VB0	-0.5 to 28	V
VB6	VB5 to VB0	-0.5 to 32	V
VB7	VB5 to VB0	-0.5 to 35	V
VB8	VB5 to VB0	-0.5 to 40	V
ΔVBi (i=1~n)	VBn–VB(n-1) (n=1~8)	-0.5 to 6	V
DS_FET	DS_FET to VB0 Voltage	-0.5 to 18	V
CH_FET	CH_FET to VB0 Voltage	-15 to 18	V
	CH_FET to VIN Voltage	≥ -40	V
All other pins	Terminal to VB0 Voltage	-0.5 to 5.5	V

RECOMMANDED OPERATING RANGE

SYMBOL	ITEMS	VALUE	UNIT
V_{IN}	Power Supply Voltage	6 to 35	V
ΔVBi (i=1~n)	VB_n–$VB_{(n-1)}$ (n=1~5)	2.0 to 4.3	V
DS_FET, CH_FET	Terminal Voltage	-0.5 to 16	V
All other pins	Terminal Voltage	≤ 5	V
	Temperature Range	-40 to +85	°C

ELECTRICAL CHARACTERISTICS

(VIN = 25V, T_A = 25°C, unless otherwise specified.)

SYMBOL	ITEMS	CONDITIONS	Min	Typ	Max	UNIT
VIN	Input Voltage	Full function guaranteed (Note1)	6		35	V
I_{SLEEP}	Supply Current at Sleep Mode	EN = 0, LDO without loading		8	12	μA
I_{NORMAL}	Supply Current at normal mode	EN = 1, LDO without loading, no balance current		1.2		mA
I_{BAL}	Balance Current	Balance select enable without external resistance	45	50		mA
I_{detect}	Cells Detect Current when Cell Select on	△VBi (i = 1~8) = 3.7V, Sink current from VB1		8		μA
		△VBi (i = 1~8) = 3.7V, Sink current from VB2		45		μA
		△VBi (i = 1~8) = 3.7V, Sink current from VB3~VB8		80		μA
t_{OUT}	VOUT Setup Time from Cell Select change or EN = 1	With 20pF load capacitance			10	μs
VDDD	LDO Output Voltage	T = -20~85°C, EN = 1, no load	4.8	5	5.2	V
		EN = 0, no load	4.3		5.5	
I_{LDODRV}	LDO Output Current capability	Normal operation (EN = 1, VDDD drop to 90%)	45			mA
		Sleep mode (EN = 0, VDDD drop to 3.5V)	4			
		EN = 1, Short to ground		10	40	
TSD	Internal Thermal Shutdown			150		°C
△TSD	TSD Hysteresis			20		
$I_{\_DSFET}$	DS_FET Source Current	DS_IN = 1, DS_FET pull down to GND	45			mA
	DS_FET Sink Current	DS_IN = 0, DS_FET pull up to V_{O_DSFET}	45			
$I_{\_CHFET}$	CH_FET Source Current	CH_IN = 1, CH_FET pull down to GND	45			
	CH_FET Sink Current	CH_IN = 0 (note2)	High impedance			
V_{O_DSFET}	DS_FET output voltage	VIN > 12V, DS_IN = 1	10	12	16	V
		6V < VIN < 12V, DS_IN = 1		VIN		
		DS_IN = 0		0.1	0.5	
V_{O_CHFET}	CH_FET output voltage	VIN > 12V, CH_IN = 1	10	12	16	
		6V < VIN < 12V, CH_IN = 1		VIN		
△VOUT	Battery Voltage Measure Error	△VBi = 4.2V (i = 1~8) (note3)	-15		15	mV
		△VBi = 2.0V (i = 1~8)	-40		40	
V_{IL}	Digital Input Voltage Low Logic	CS0~CS2, BS0~BS2, CH_IN, DS_IN, EN, BL			0.2	VDDD
V_{IH}	Digital Input Voltage High Logic	CS0~CS2, BS0~BS2, CH_IN, DS_IN, EN, BL	0.6			VDDD

Note1: The VOUT is correct under such VIN input range;

Note2: When CH_IN = 0, CH_FET pin is high impedance and charge MOSFET pull low is dependent on the resistor between gate and source node of charge MOSFET;

Note3: If △VB2-△VB1>400mV, the measurement accuracy of △VB2 will decrease.

FUNCTIONAL BLOCK DIAGRAM

原厂技术支持：联系人：徐俐湘　联系电话：18565820880

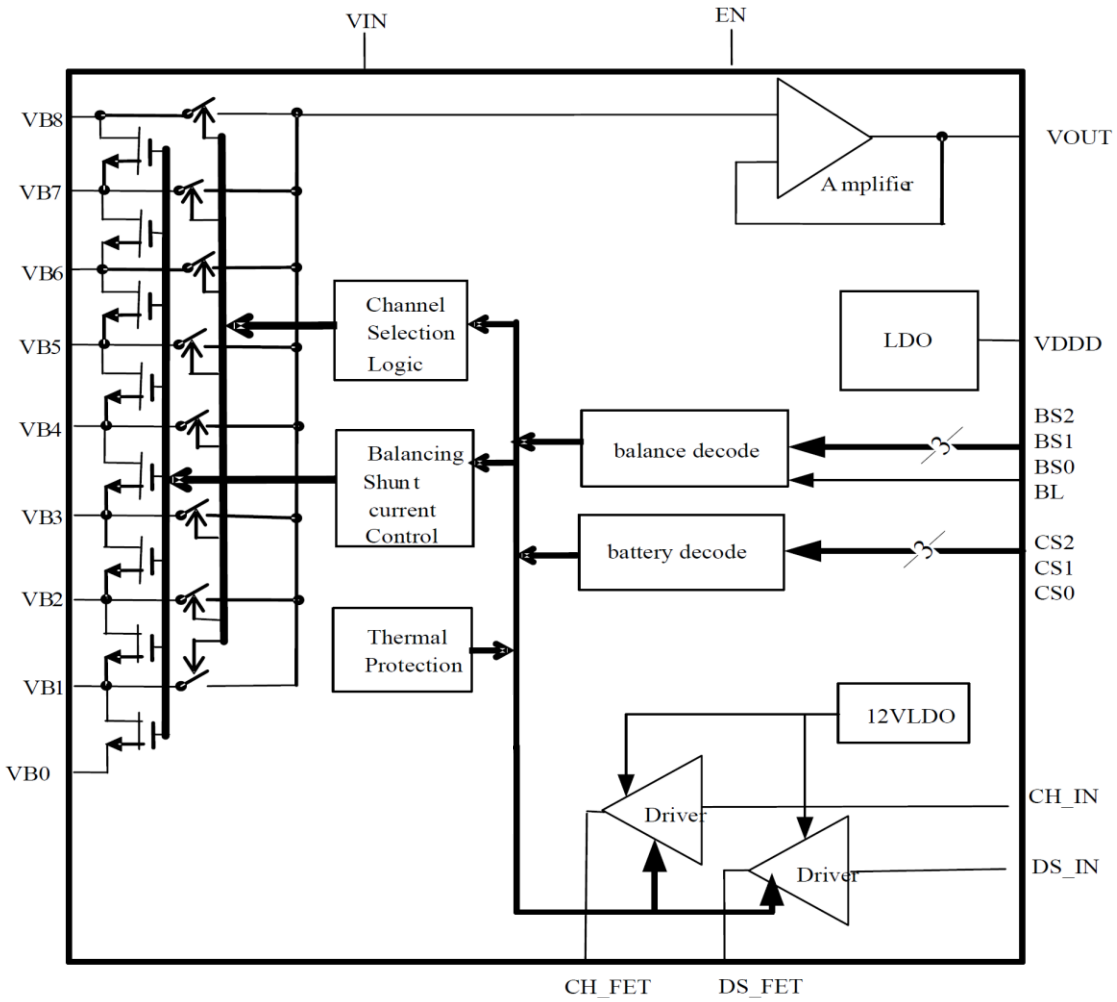


Figure3. Simplified functional block diagram of PT6111

FUNCTION DESCRIPTION

1. Cell Voltage Monitor Function

PT6111 includes five level shift circuits and a high precision amplifier for cell voltage monitoring. The level shift circuit can transfer the voltage of one of cells to the input of amplifier. The amplifier will export the voltage to MCU as a buffer through VOUT pin. MCU can select corresponding level shift circuit by controlling CS0, CS1, and CS2 to monitor different cell's voltage by ADC, and then determine the state of battery pack.

CS2	CS1	CS0	VOUT State
0	0	0	1st cell's voltage
0	0	1	2nd cell's voltage
0	1	0	3rd cell's voltage
0	1	1	4th cell's voltage
1	0	0	5th cell's voltage
1	0	1	6th cell's voltage
1	1	0	7th cell's voltage
1	1	1	8th cell's voltage

A ceramic capacitor near VOUT pin is necessary to stabilize the voltage of VOUT pin. The ADC of MCU can't sample the voltage of VOUT pin until the voltage reach a steady-state value after cell was selected.

2. Cell Balance Function

PT6111 can provide a shunt current of 50mA for every cell without any external components by integrating cell balance circuits. MCU can determine which balance shunt current is enabled by controlling BS0, BS1, BS2 and BL after the state of cells was detected. At the same time PT6111 can only balance one cell. The balance current will be limited by external resistance of RC filter.

BL	BS2	BS1	BS0	Balance Current
0	X	X	X	No cell selected
1	0	0	0	1st cell on
1	0	0	1	2nd cell on
1	0	1	0	3rd cell on
1	0	1	1	4th cell on
1	1	0	0	5th cell on
1	1	0	1	6th cell on
1	1	1	0	7th cell on
1	1	1	1	8th cell on

3. 5V LDO

PT6111 integrated a LDO of 5V, which can supply power to MCU from VDDD pin. The input of the LDO is VIN pin and a resistor between positive of battery pack and VIN is necessary to reduce the power loss on chip. A ceramic capacitor near VDDD pin is necessary to stabilize the LDO output voltage.

The LDO can supply a current of at least 45mA in normal mode when EN = 1, and then will turn to a low power mode when EN = 0, in which the output current capability will reduce to 4mA and the output voltage accuracy will drop.

When the output of LDO was shorted to ground, the output current will be limited at 10mA. But still there is a risk to damage when short to ground because of insufficient response time.

4. Charge and Discharge MOSFETs Control

PT6111 integrates external charge and discharge MOSFETs driver, which powered by an internal LDO of 12V and which controlled by CH_IN and DS_IN. The driver of discharge MOSFET (DS_FET pin) can sink and source a current to close and open discharge MOSFET, but the driver of charge MOSFET (CH_FET pin) is an open-drain output which can only source a current to open charge MOSFET and then a resistor between gate and source of charge MOSFET is necessary for turning off the charge MOSFET when CH_FET is high impedance.

5. Thermal Shutdown

When the junction temperature of PT6111 exceeds 150°C (typical), the chip will turn off the charge and discharge MOSFETs and stop cell balance function until the junction temperature drops below 130°C (typical). When thermal shutdown, VDDD still supply power for MCU.

6. Sleep mode

When EN=0, PT6111 enter sleep mode, all the function blocks will stop work except 5V LDO, charge and discharge MOSFET will be switch off, power consumption is about 8uA (typical).

7. 3~8 Cell Li-ion Battery Packs Application

PT6111 can be used to monitor cells voltage, balance cells and control charge/discharge MOSFETs at 3~8 cell Li-ion battery packs as analog front end.

For the application of 8 cells, circuit connection is as Figure4.

For the application of 7 cells, circuit connection is as following Figure1. VB8 and VB7 are connected.

For the application of 6 cells, circuit connection is as following Figure5. VB8, VB7 and VB6 are connected.

A zener diode between VB8 and VB0 is necessary to prevent VB8 pin suffering over stress.

The maximum voltage from VBi to VBi-1 (i = 1~8) cannot exceed 6V. The zener diodes between VBi and VBi-1 (i = 1~8) can be used to protect VBi to VBi-1 (i = 1~8) from high voltage when some of abnormal conditions happened.

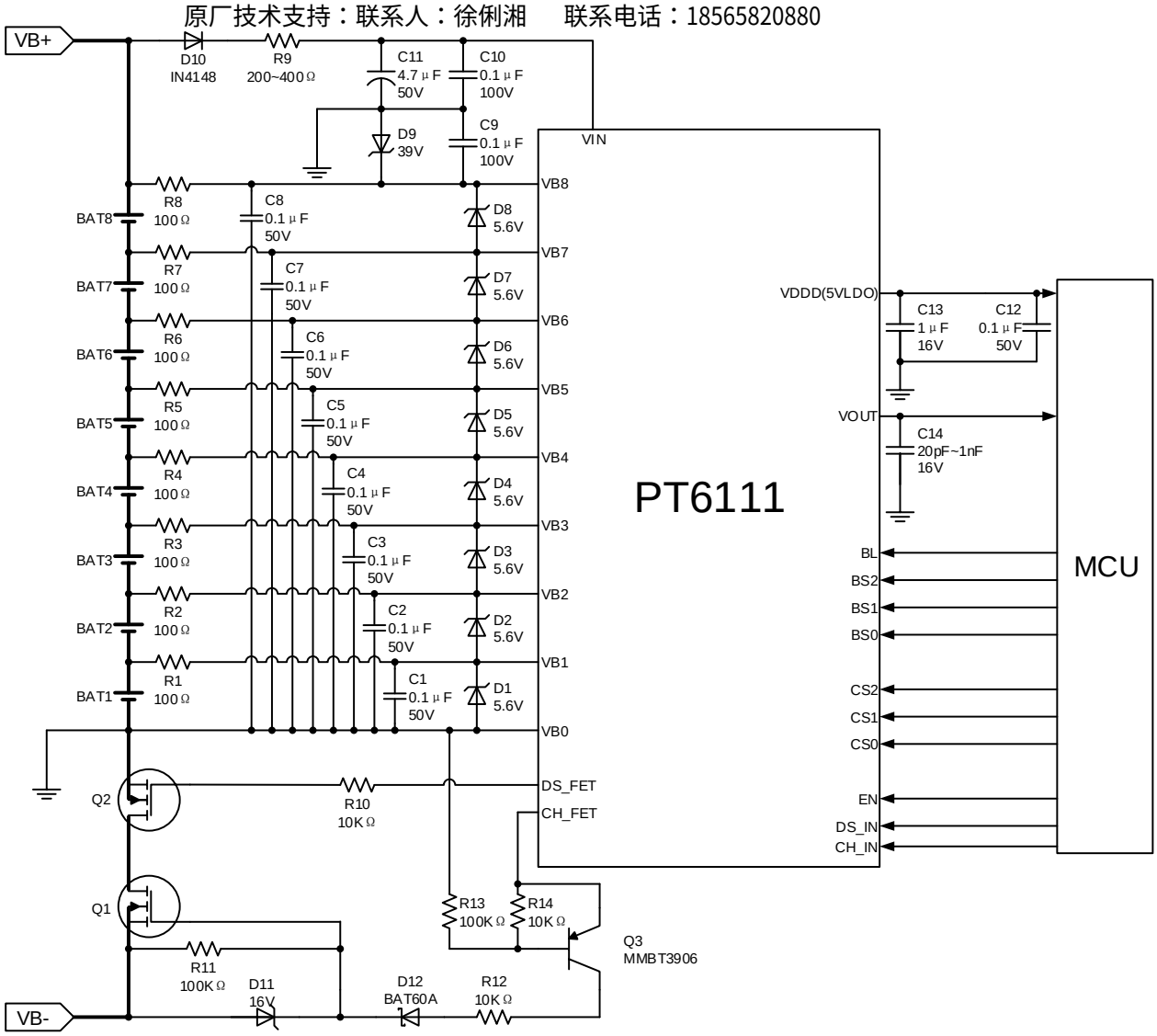


Figure 4. Typical application of PT6111 for 8 cell LiFePO4 battery

(Note: 8 cells application is only for LiFePO4, because chip max rating voltage is 40V)

原厂技术支持：联系人：徐俐湘　联系电话：18565820880

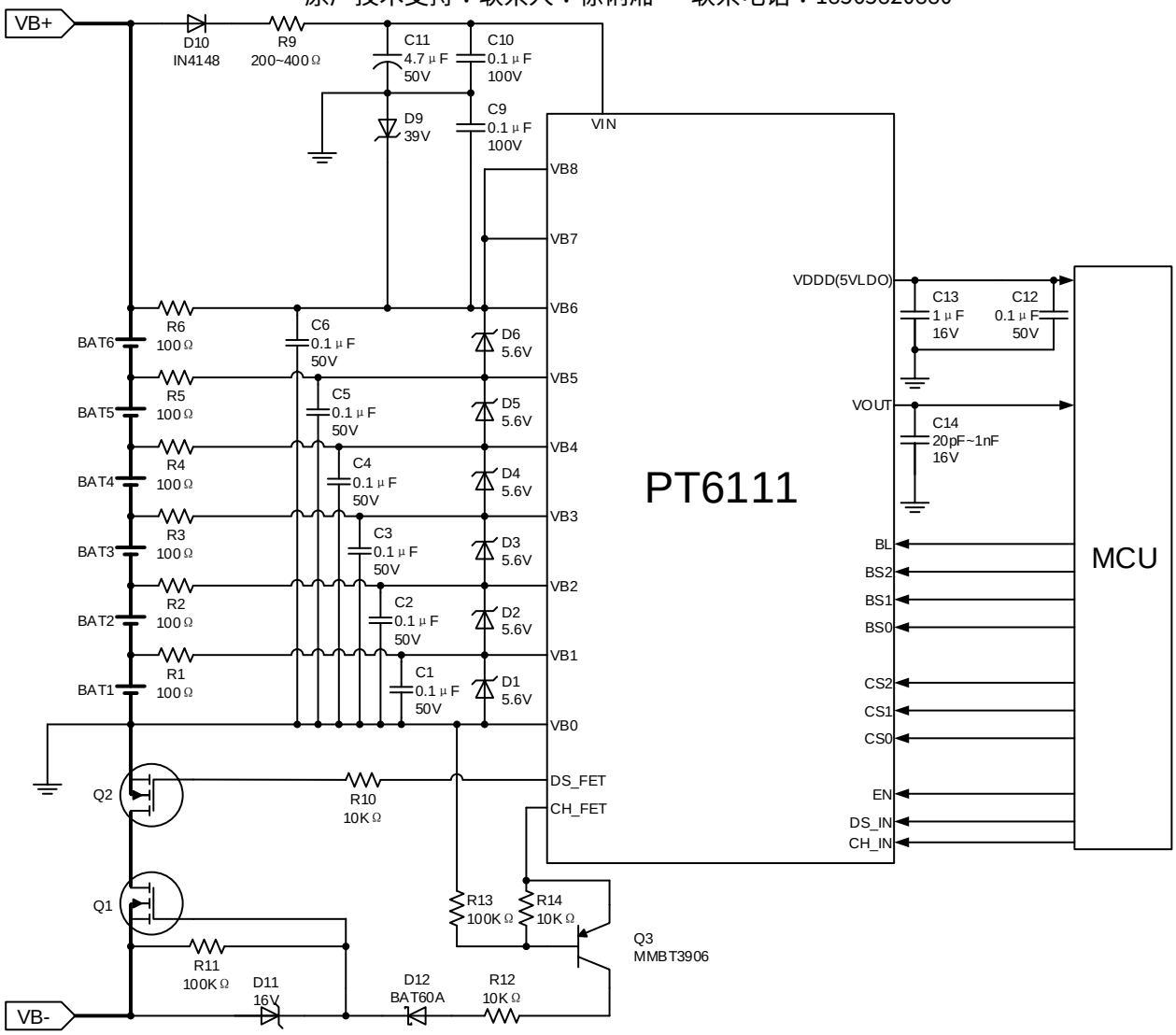
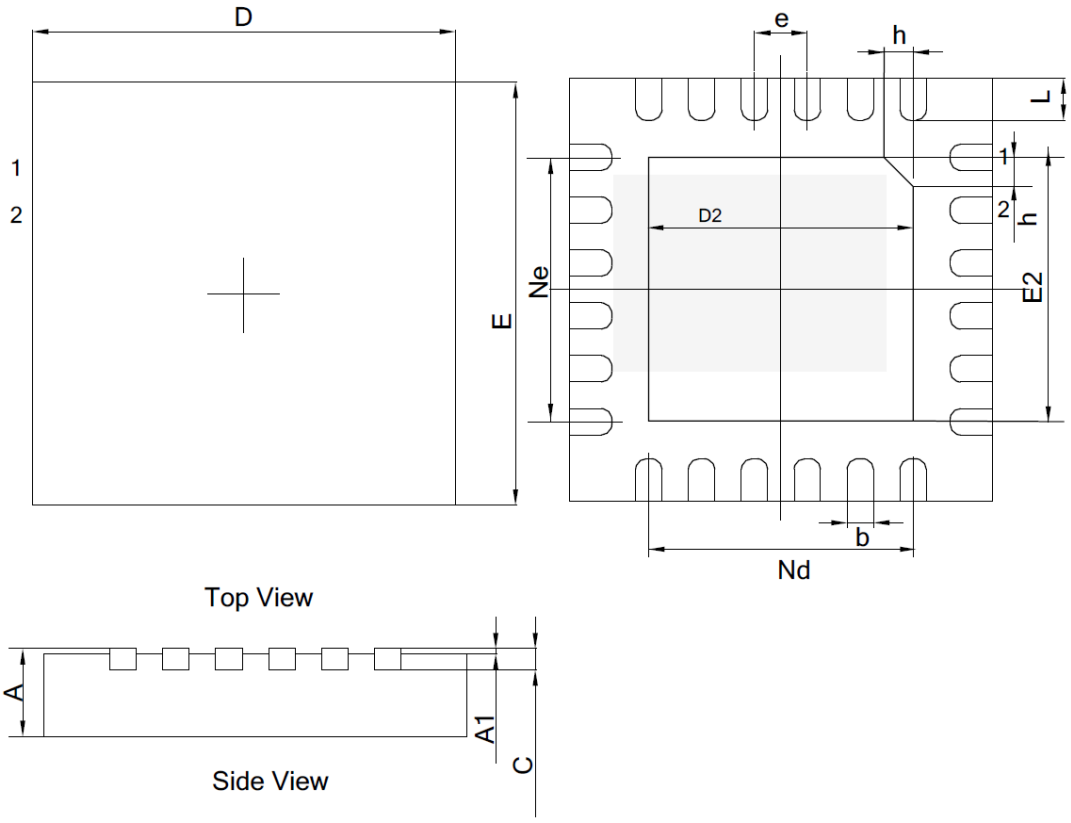


Figure 5. Typical application of PT6111 for 6 cells Li-ion battery

PACKAGING INFORMATION

原厂技术支持：联系人：徐俐湘　联系电话：18565820880

QFN-24 4x4



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.01	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.50REF		
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.50REF		
L	0.35	0.40	0.45
h	0.30	0.35	0.40

IMPORTANT NOTICE

POWTWCH (SHANGHAI) CO., LTD. reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services and to discontinue any product or service. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to POWTECH’s terms and conditions of sale supplied at the time of order acknowledgment.

POWTECH warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in POWTECH’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent POWTECH deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

POWTECH assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using POWTECH components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

No POWTECH components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those POWTECH components which POWTECH has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of POWTECH components which have not been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use

Unless POWTECH has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use, POWTECH will not be responsible for any failure of such components to meet such requirements.