DESCRIPTION

The PT6586 is 1/4 duty general-purpose LCD driver that can be used for frequency display in electronic tuners under the control of a microcontroller. The PT6586 can drive an LCD with up to 140 segments directly. The PT6586 can also control up to 4 general-purpose output ports.

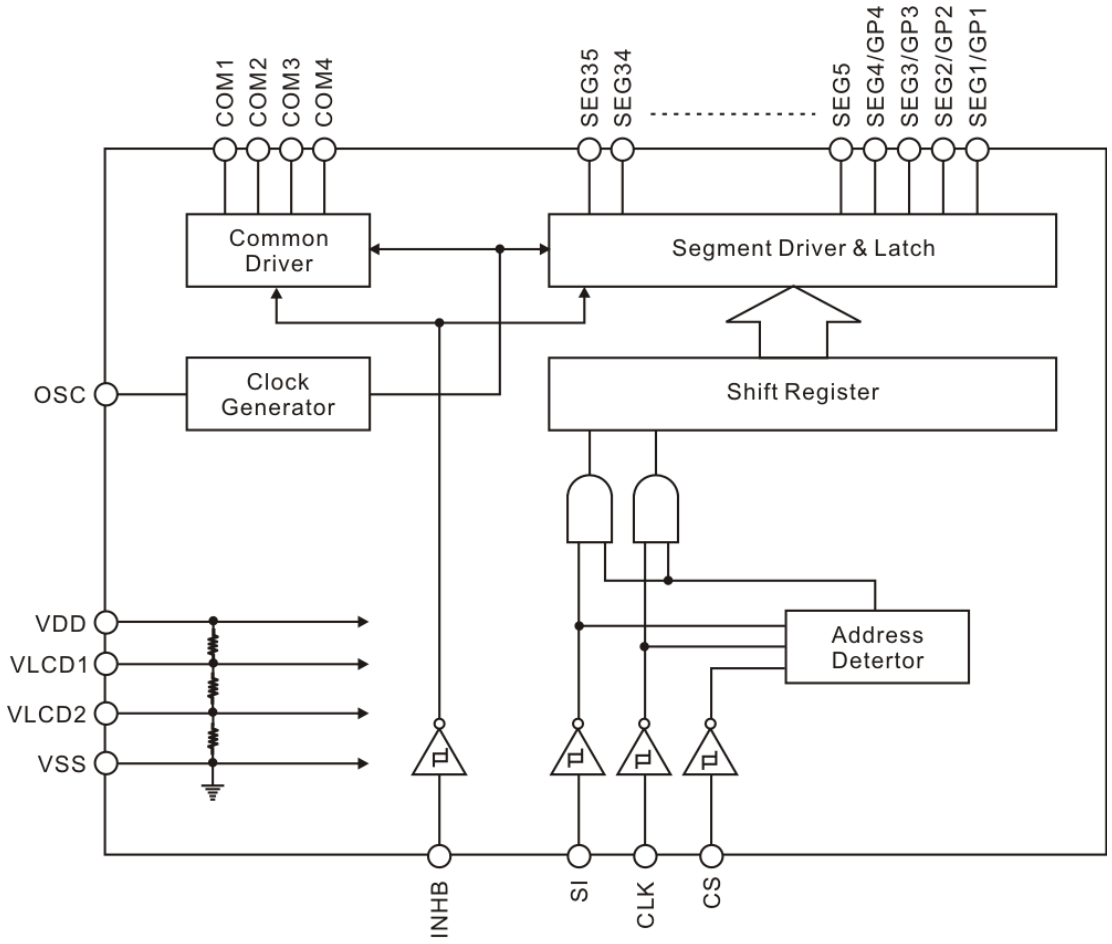
APPLICATION

- Electronic equipment with LCD Display

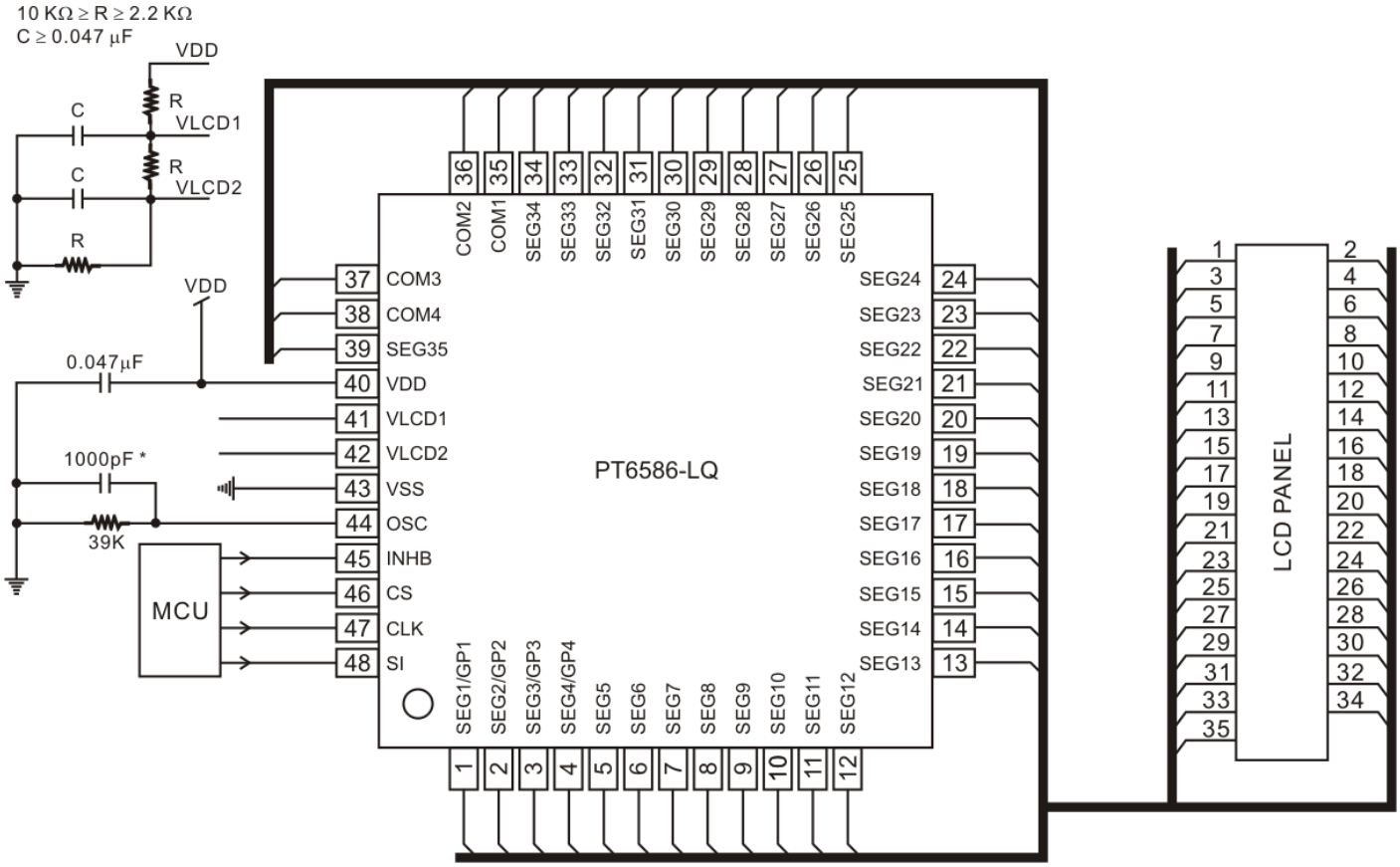
FEATURES

- Up to 140 segments for 1/4 duty drive can be displayed
- Serial interface for clock, Data Input, Strobe pins
- Serial data control of the power-saving mode based backup function and all the segments forced off function
- Serial data control of switching between the segment output port and the general-purpose output port functions
- Serial data control of frame frequency for common and segment output waveforms
- High generality, since display data is displayed directly without decoder intervention
- The INHB pin can force the display to the off state
- RC oscillator circuit

BLOCK DIAGRAM



APPLICATION CIRCUIT

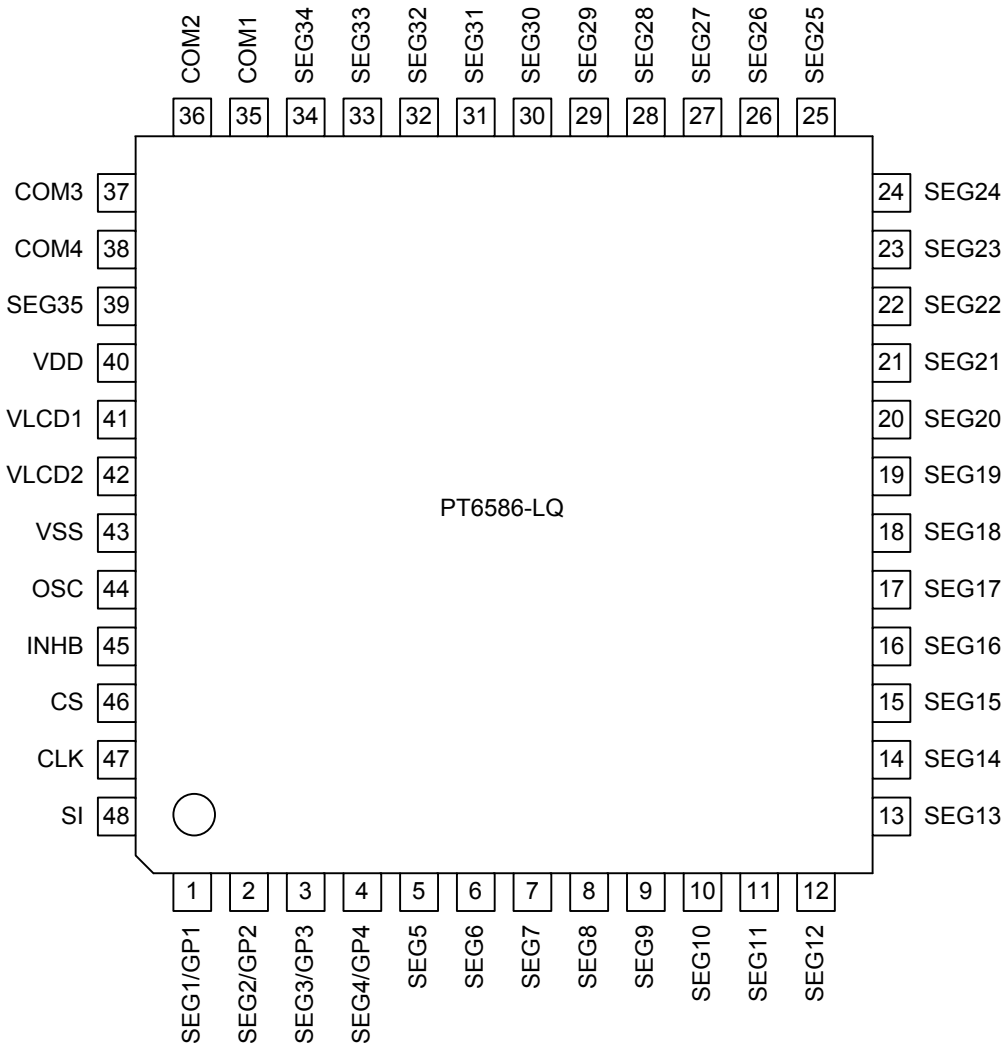


Note:* = When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6586-LQ	48-pin, LQFP	PT6586-LQ

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Active	Handling when unused	Function	Pin No.
SEG1/GP1 to SEG4/GP4	O	-	Open	Segment outputs for displaying the display data transferred by serial data input. The pins SEG1/GP1 to SEG4/GP4 can be used as general-purpose output ports when so set up by the control data.	1 to 4
SEG5 to SEG34					5 to 34
SEG35					39
COM1 to COM4	O	-	Open	Common driver outputs. The frame frequency is f_O Hz.	35 to 38
VDD	-	-	-	Logic block power supply. Provide a voltage in the range 4.5 to 6.0V.	40
VLCD1	I	-	Open	LCD drive 2/3 bias voltage (middle level) supply. It is possible to supply the 2/3 VDD voltage to this pin externally.	41
VLCD2	I	-	Open	LCD drive 1/3 bias voltage (middle level) supply. It is possible to supply the 1/3 VDD voltage to this pin externally.	42
VSS	-	-	-	Ground pin. Connect to ground.	43
OSC	I/O	-	VDD	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor to this pin.	44
INHB	I	L	GND	Display off control input • INHB = low (VSS)…off SEG1/ GP1 to SEG4/GP4 = low (VSS) (These pins are forcibly set to the segment output port function and fixed at the VSS level) SEG5 to SEG35 = low (VSS) COM1 to COM4 = low (VSS) • INHB = high (VDD)…on Note that serial data transfers can be performed when the display is forced off by this pin.	45
CS	I	H	GND	Serial data transfer inputs. These pins are connected to the control microprocessor. CS: Chip enable CLK: Synchronization clock SI: Transfer data	46
CLK	I	↑			47
SI	I	-			48

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

Princeton Technology Corp.
2F, 233-1, Baociao Road,
Sindian, Taipei 23145, Taiwan
Tel: 886-2-66296288
Fax: 886-2-29174598
http://www.princeton.com.tw

REVISION HISTORY

Date	Revision No.	Reference No.	Modification
4/8/2009 5/11/2009	PT6586 REF1.0	Request no.: 090314 Approval no.:	1. p5, Modify “Input pin: CLK, CS, SI, INHB”
7/1/2009	PT6586 PRE1.0	MAC0906007	P1, Modify Block Diagram P3, Redraw Pin Configuration Modify all “GPxx/SEGxx→SEGxx/GPxx, Gx→GPx P5, Modify “Input/Output Configuration” P7, Modify “Serial Data Transfer Format”裡的”When CLK is stopped at the high level” P8, Modify “serial data transfer example” P13, Modify “the INHB pin and display control” P14, Modify “Absolute Maximum Ratings” & “ Allowable Operating Ranges” P16, Redraw “ Condition 1” & “Condition 2” Add Package Information
02/26/2010	PT6586 V1.0	MAC1002018	1. P13, Modify The INHB pin and Display Control 2. P14, Correct the title to “Absolute maximum ratings” 3. P15, Modify Electrical Characteristics 4. P16, Modify Figure 4
6/1/2010	PT6586 V1.1	MAC1005025	P6, When clk is stopped at the low level P7, When clk is stopped at the high level P17, Package Information