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DESCRIPTION

PT6904 is a constant-current LED driver IC utilized constant frequency, controls buck, boost or buck-boost switch converter. In each control mode, PT6904 adopts the inductance current continuous conduction, peak current control mode and the feedback of the output current. It's controlled by the internal transconductance operational amplifier and external adjustable slope compensation, it is able

The typical functions of PT6904 such as UVLO (Under Voltage Lockout), input current limit, open LED protection, output short circuit protection, output current precision control, linear dimming, PWM dimming, etc. In addition, multiple the sync pin of PT6904s or input the same clock signal, these ICs will operate on the same frequency.

Input voltage of PT6904 is 9V to 36V, the oscillator frequency is 25KHz~350KHz that setting by the external resistors, and the output PWM signal drive external power NMOS. PWM dimming input can accept an external control signal with a duty cycle 0~100% and a frequency between 100Hz to a few KHz.

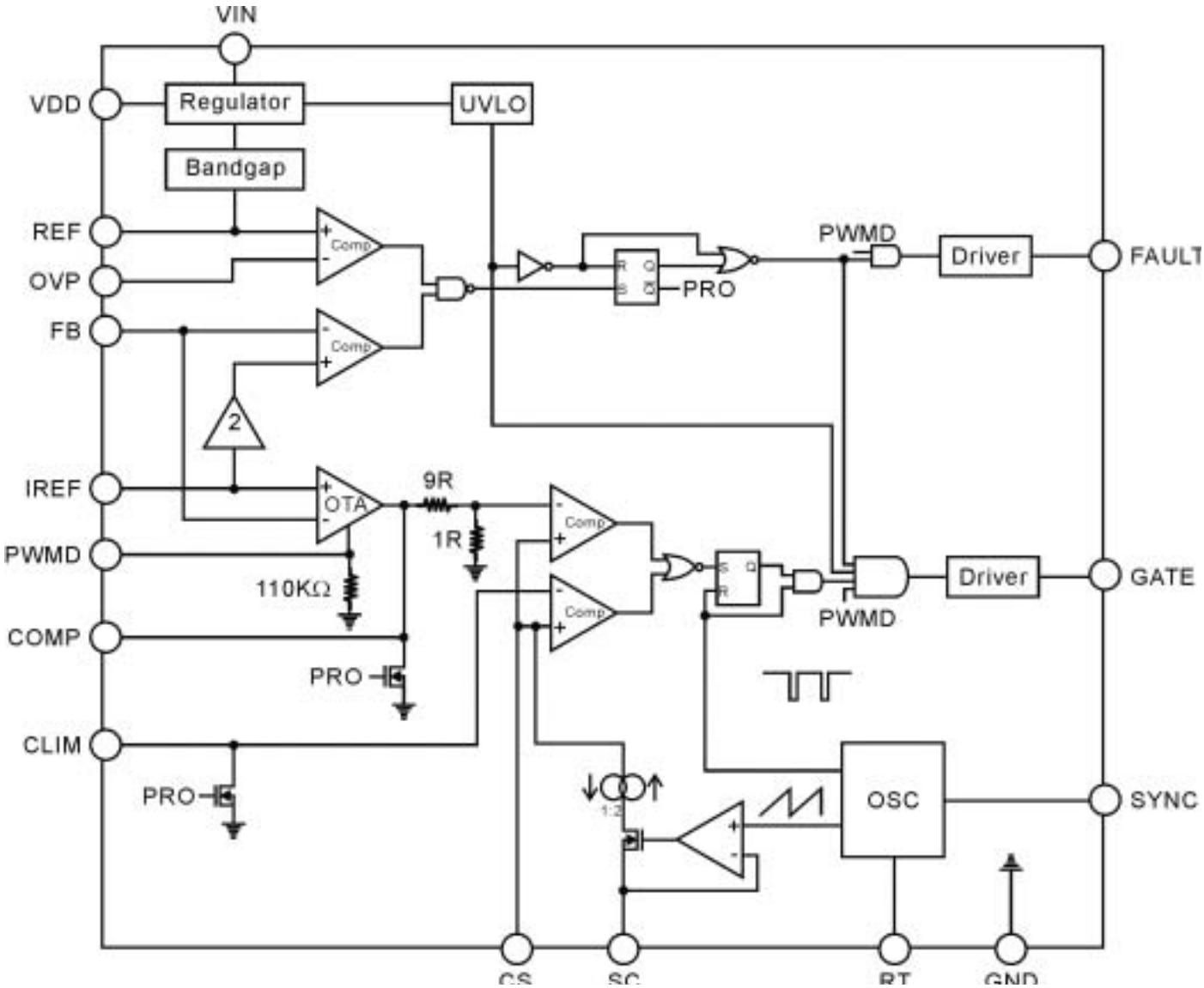
FEATURES

- >90% Efficiency
- Operating voltage: 9V~36V
- Constant-current driver
- Switch control mode: Buck, Boost, Buck-Boost
- Stable operation frequency
- Slope compensation
- Output current closed loop control
- Input current limit, output over voltage protection, output short-circuit protection
- Linear dimming & PWM dimming
- Synchronization
- Soft start

APPLICATIONS

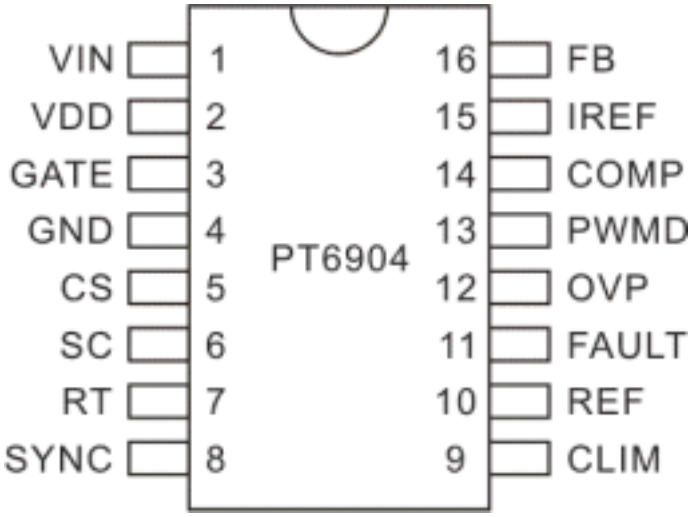
- LED backlight
- Automotive LED lighting
- Other DC/DC LED

BLOCK DIAGRAM



PIN CONFIGURATION

16 PINS, SOP



PIN DESCRIPTION

Pin Name	Description	Pin No.
VIN	Input voltage 9V~36V DC.	1
VDD	Internal regulated voltage.	2
GATE	Drives the gate of external N-channel MOSFET.	3
GND	Ground.	4
CS	Senses the external MOSFET current.	5
SC	Slope compensation for current sense.	6
RT	Oscillator frequency control.	7
SYNC	Synchronization control.	8
CLIM	Input current limit & Soft start.	9
REF	Reference voltage.	10
FAULT	Drives the gate of external N-channel MOSFET. It will be locked at low level when IC works in error condition.	11
OVP	Over voltage protection.	12
PWMD	Low frequency PWM dimming pin, also enable pin.	13
COMP	Output of OTA, stable closed loop control.	14
IREF	Sets the LED string current level.	15
FB	LED string current feedback & output short circuit protection.	16

FUNCTION DESCRIPTION

LINEAR REGULATOR

PT6904 will adjust the input voltage from 9V~36V DC to 5V and 8V as internal demand. And the 8V voltage is extracted by VDD pin that connected with a 10μF electrolytic capacitor.

REFERENCE

PT6904 provides a 1.18V reference voltage at the REF pin. It is used to set the output over voltage protection threshold. Meanwhile, the potential reference of input current limit and output current can be setup by resistance division. The maximum output current of REF is up to 1mA.

OSCILLATOR

PT6904 operates in the constant-frequency mode. Through the RT Pin connecting external resistor to ground, the oscillator frequency can be set as following.

$$f \quad \frac{6.4\times10^{10}}{R_T}$$

SLOPE COMPENSATION

Working in the constant frequency, under the inductance peak current control mode, when the duty cycle is more than 50%, the slope compensation becomes necessary in order to ensure the stability. The slope compensation can be achieved by adding a voltage ramp, whose upward slope is one half of the inductor current's downward slope, to the inductor current's puts voltage Vcs. And this can be done through the setting of two resistors – Rslope and Rsc. Suppose the inductor current's downward slope is DS (A/μS), then:

$$R_{SLOPE} = \frac{4.2\times R_{SC} \times}{f_{CS}}$$

Note: The maximum output current of SC Pin is 100μA, which will limit the minimum value of Rslope to be 12KΩ. In case the Rslope, which is calculated by the mentioned formula above, is less than 12KΩ, the Rsc must be increased. The proposed choice range for Rslope is 12KΩ to 25KΩ. If the duty cycle is less than 50%, the compensate slope can be omitted, and SC Pin can be left vacant.

CURRENT SENSE

Tblank is defined as a fixed turn-on time of 300ns set within PT6904. IC takes the reduced voltage which is 1/10 of Tansconductance operational amplifier's output voltage (COMP voltage) as the reference potential to compare with the inductor current sampling signals. When the sampling signal is greater than the reference potential, the GATE output will close.
Note: It is better to choose appropriate resistance Rcs, and set the comparison reference potential of the PWM comparator to be 250mV.

CURRENT LIMIT & SOFT START

The comparison reference potential of input current limit is achieved by dividing the 1.18V reference voltage offered by IC through the resistor divider. Suppose the maximum current of inductance is I_{LM}, limit the input current to be 120% of inductance maximum current, then the current limit voltage can be set as:

$$V_{CLIM} \geq 1.2 \times I_{LM} \times R_{CS} + \frac{2.36 \times R_{SC}}{R_{SLOPE}}$$

At CLIM pin, connecting the capacitor with ground to rise the CLIM voltage slowly can achieve the soft-start function.

OVER VOLTAGE PROTECTION

Compare the sampling voltage of output which is got through the resistor divider with the IC's 1.18V reference voltage, when the sampling voltage is greater than 1.18V, the over voltage protection function acts and the outputs of GATE and FAULT close. After the protection acts, IC cannot work normally until it is re-powered.

OUTPUT SHORT CIRCUIT PROTECTION

IREF voltage can be got by dividing the REF voltage through the resistor divider and as the reference potential of output current. $I_{OUT} = \frac{V_{IREF}}{R_S}$, when the output current exceeds twice of the presupposed current, the output over current protection function will act and the outputs of GATE and FAULT close. After the protection acts, IC cannot work normally until it is re-powered.

LINEAR DIMMING

Adjusting the IREF voltage can implement the linear dimming of output current.
Note: When IREF voltage is very little, the offset voltage of output short-circuit protection comparator may cause a short-circuit protection.

PWM DIMMING

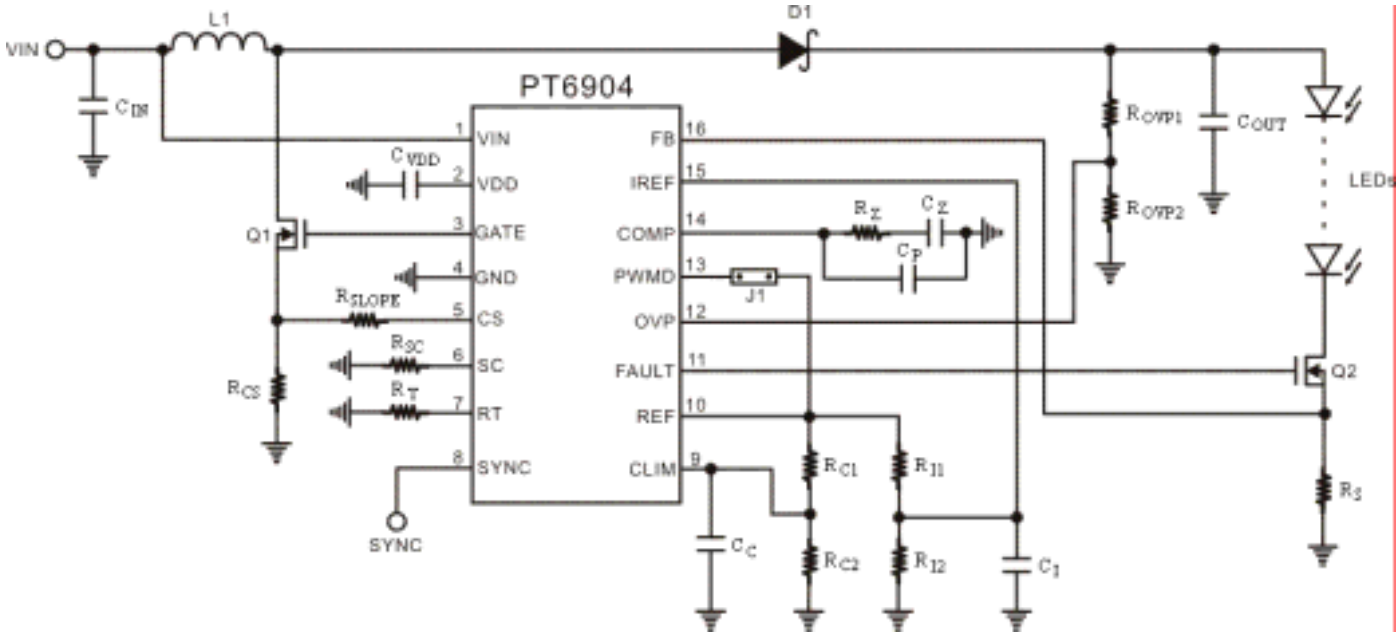
PWM Dimming can be achieved by PWMD Pin input PWM signal. The input signal frequency can be from 100Hz to several KHz, with the duty cycle range of 0 to 100%. PT6904's PWM Dimming function is able to achieve very fast PWM dimming response: when the PWMD signal is low, GATE signal and FAULT signal will close the output, the LED current will almost drop to zero immediately, no discharging access will be for the output capacitor. What's more, the disconnection between operational transconductance amplifier's output and compensation circuit can help maintain the voltage of compensation circuit not to be changed. When the PWMD signal is high, the circuit will resume steady at once, preventing from causing the output current's long time adjustment and the prodigious output surge current.

SYNCHRONIZATION

When a single PT6904 works, SYNC can be left vacant or connected to ground through the pull-down resistor. If multiple PT6904s are connected by their SYNC pin, they will work in the same frequency which is the highest operating frequency among all of these ICs. It also works to import a clock signal to SYNC pin. The IC's operating frequency will be the same as the clock signal in this case.

Note: When multiple ICs work in the same frequency, it is better to choose the same RT.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
VIN to GND		-0.3 ~ +40	V
VDD to GND		-0.3 ~ +40	V
CS to GND		-0.3 ~ 6	V
SC to GND		-0.3 ~ 6	V
RT to GND		-0.3 ~ 6	V
REF to GND		-0.3 ~ 6	V
OVP to GND		-0.3 ~ 6	V
PWMD to GND		-0.3 ~ 6	V
IREF to GND		-0.3 ~ 6	V
FB to GND		-0.3 ~ 6	V
Operating temperature	Topr	-40 ~ +85	℃
Storage temperature	Tstg	-65 ~ +150	℃

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, VIN=36V, Ta=25℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input DC supply voltage	V_{IN}	DC input voltage	9	-	36	V
Shut-down supply current	I_{INSD}	PWMD to GND	-	-	1.4	mA
Active supply current	I_{INAC}	PWMD to REF	-	-	2.0	mA
Internal regulated voltage	VDD	CVDD=10μF, IDD=0, PWMD=GND	7.2	8.2	9.2	V
VIN under voltage lockout threshold	UVLO	VIN rising	6.5	6.9	7.2	V
VIN under voltage lockout hysteresis	△UVLO	VIN falling	-	500	-	mV
Reference voltage	V_{REF}	IREF=0, PWMD=GND	1.15	1.18	1.21	V
Load regulation of reference voltage	V_{REFL}	IREF=0-1mA, PWMD=GND	-	-	10	mV
PWMD input low voltage	V_{PL}		-	-	0.5	V
PWMD input high voltage	V_{PH}		1.0	-	-	V
PWMD pull-down resistance	R_{PWMD}		90	110	130	KΩ
Oscillator frequency	fOSC	RT=680KΩ	80	110	140	KHz
Maximum duty cycle	D_{MAX}	VCS=GND	-	90	-	%
Leading edge blanking	T_{BLANK}	VCS=REF	200	300	400	ns
Transconductance of OTA	g_m		-	550	-	μA/V
OVP voltage	V_{OVP}	OVP rising	1.15	1.18	1.21	V
Amplifier gain at IREF pin	G_{OCP}		-	2	-	-
Current sourced out of SC pin	I_{SLOPE}		0	-	100	μA
Internal current mirror ratio	G_{SLOPE}	$R_{SLOPE}=R_{SC}$	-	2	-	-
GATE output rise time	T_{RG}	C_{GATE}=1nF	-	-	80	ns
GATE output fall time	T_{FG}	C_{GATE}=1nF	-	-	40	ns
Fault output rise time	T_{RF}	C_{FAULT}=1nF	-	-	200	ns
Fault output fall time	T_{FF}	C_{FAULT}=1nF	-	-	120	ns

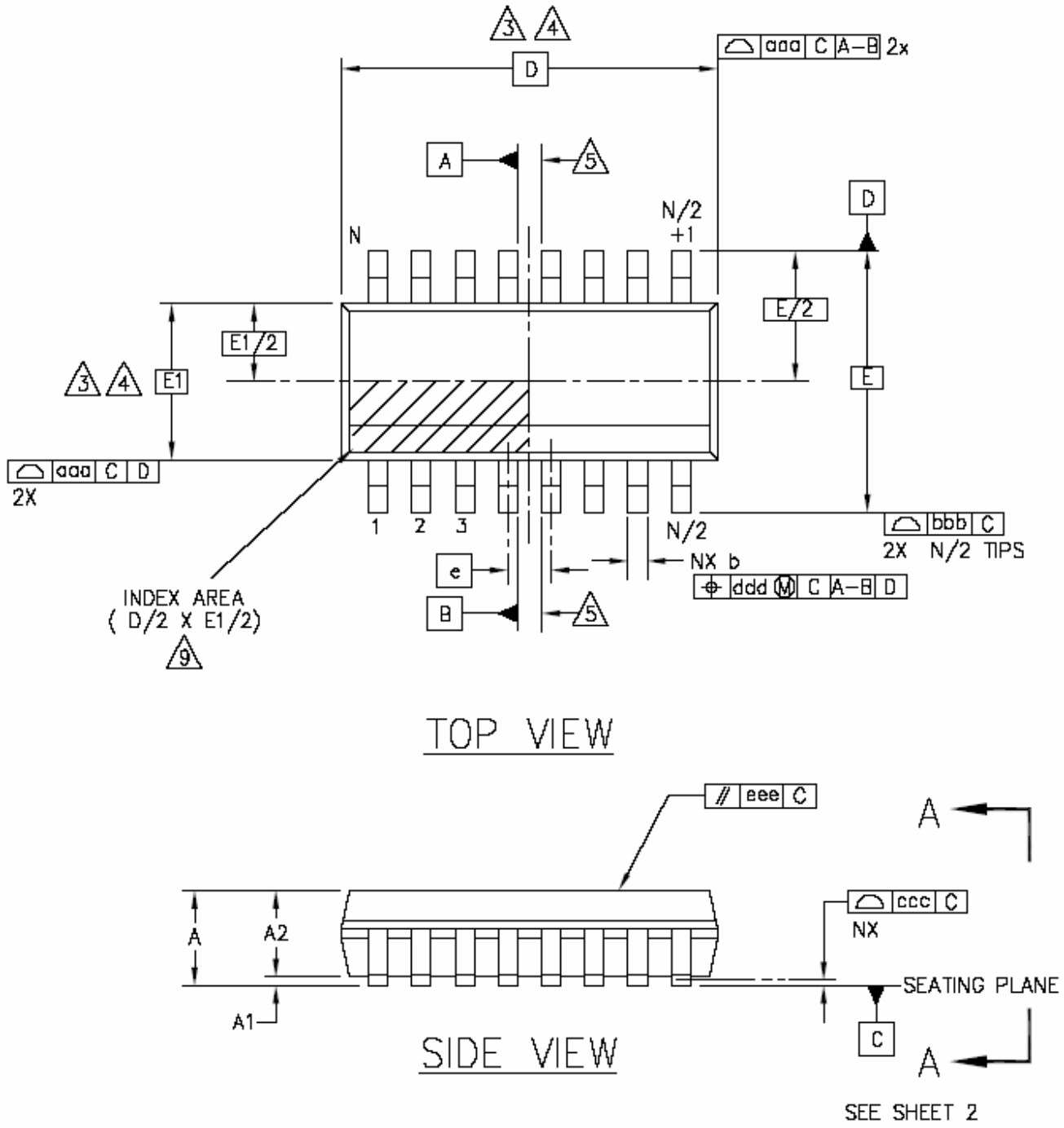
ORDER INFORMATION

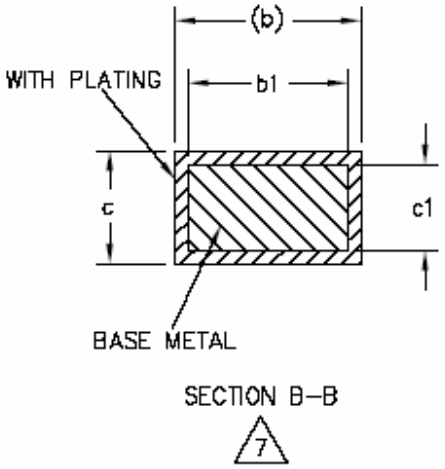
Valid Part Number	Package Type	Top Code
PT6904-S (L)	16 Pins, SOP, 150mil	PT6904-S

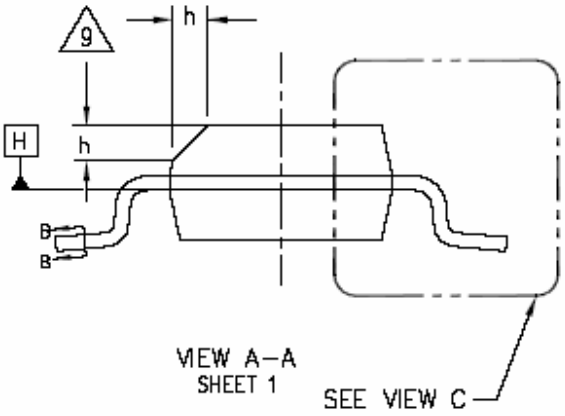
Notes:
1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the date code.

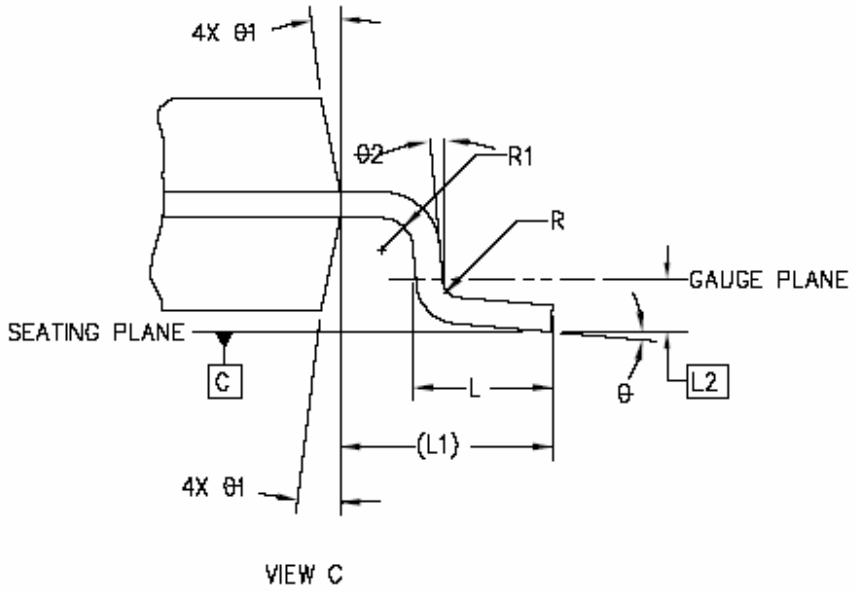
PACKAGE INFORMATION

16 PINS, SOP, 150MIL

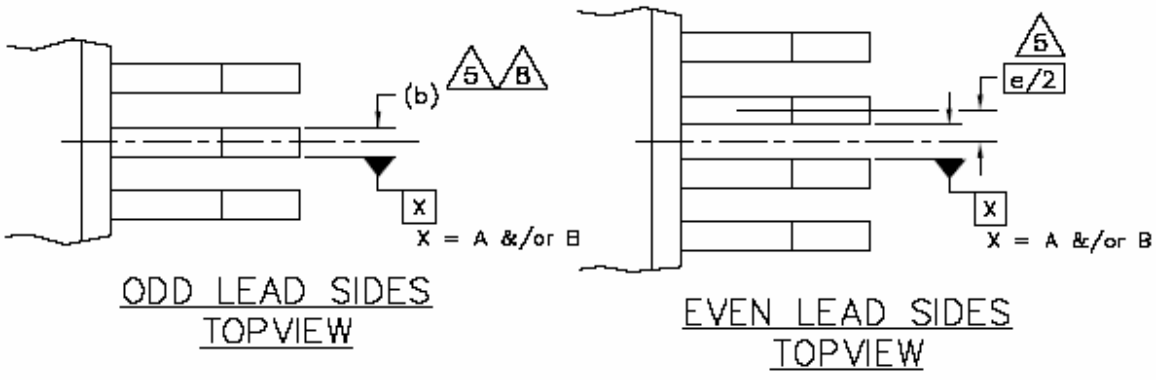



(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B–B
7


9
h
H
h
B
B
VIEW A–A
SHEET 1
SEE VIEW C


4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1

VIEW C


(b)
5
B
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW
5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	9.90 BSC.		
E	6.00 BSC.		
E1	3.90 BSC.		
e	1.27 BSC.		
L	0.40	-	1.27
L1	1.04 REF.		
L2	0.25 BSC.		
R	0.07	-	-
R1	0.07		-
h	0.25	-	0.50
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Notes

1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body. Datums A & B to be determined at datum H.
5. N is the number of terminal positions. (N=16)
6. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
7. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be
8. 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AC.

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