DESCRIPTION

PT6967 is an LED Controller driven on a 1/5 to 1/8 duty factor. 10 segment output lines, 4 grid output lines, 5 segment/grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to PT6967 via a four-line serial interface. Housed in a 32-pin SOP and QFN, PT6967 pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

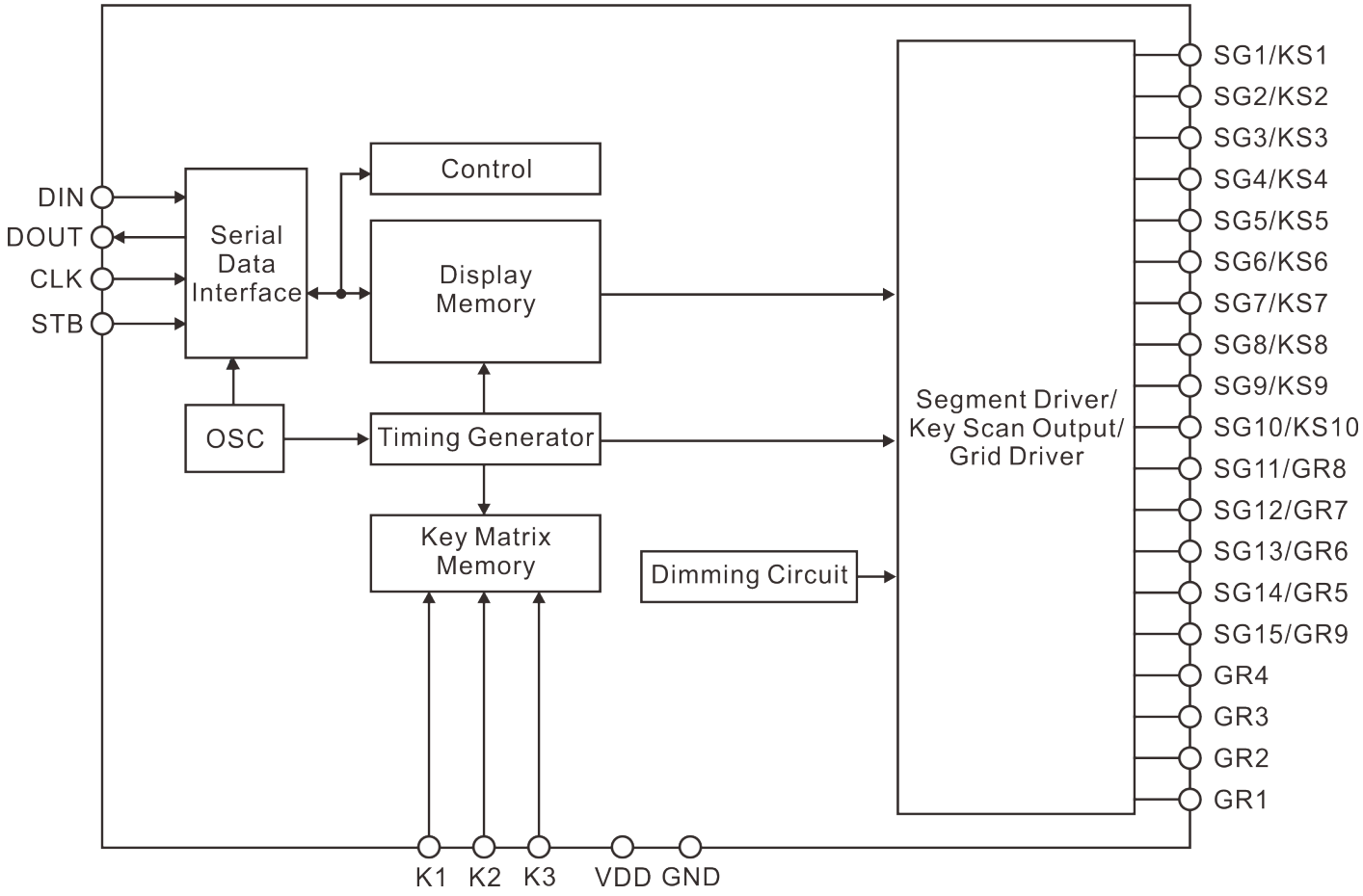
FEATURES

- CMOS technology
- Low power consumption
- Multiple display modes (15 segment, 4 Grid to 10 segment, 9 Grid)
- Key scanning (10 x 3 Matrix)
- 8-Step dimming circuitry
- Serial interface for Clock, Data Input, Data Output, Strobe Pins and low voltage operation ability when user's MCU power supply is 3.3V
- Available in 32-pin SOP and QFN

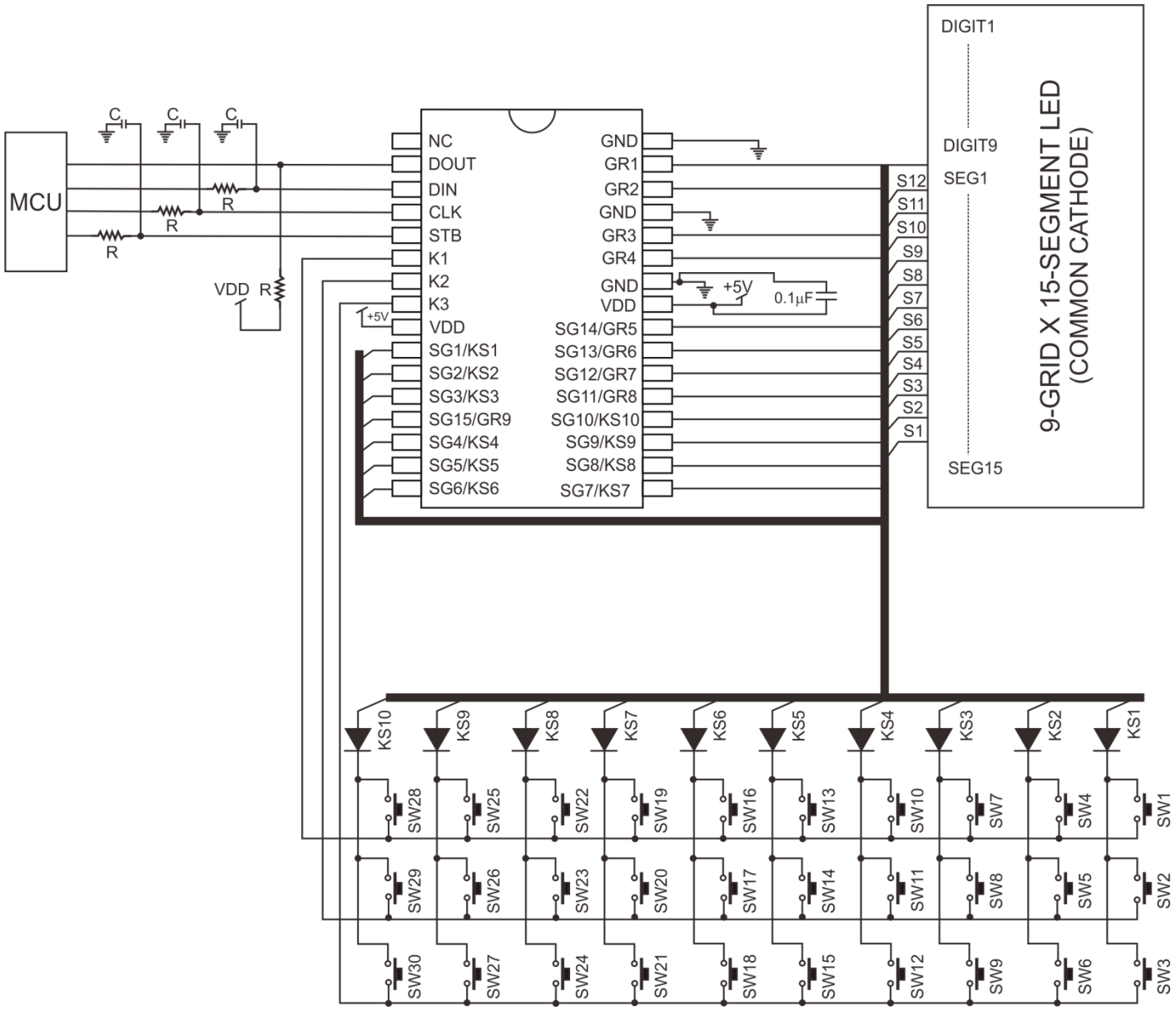
APPLICATIONS

- Micro-computer Peripheral Device
- VCR Set
- Combo Set

BLOCK DIAGRAM

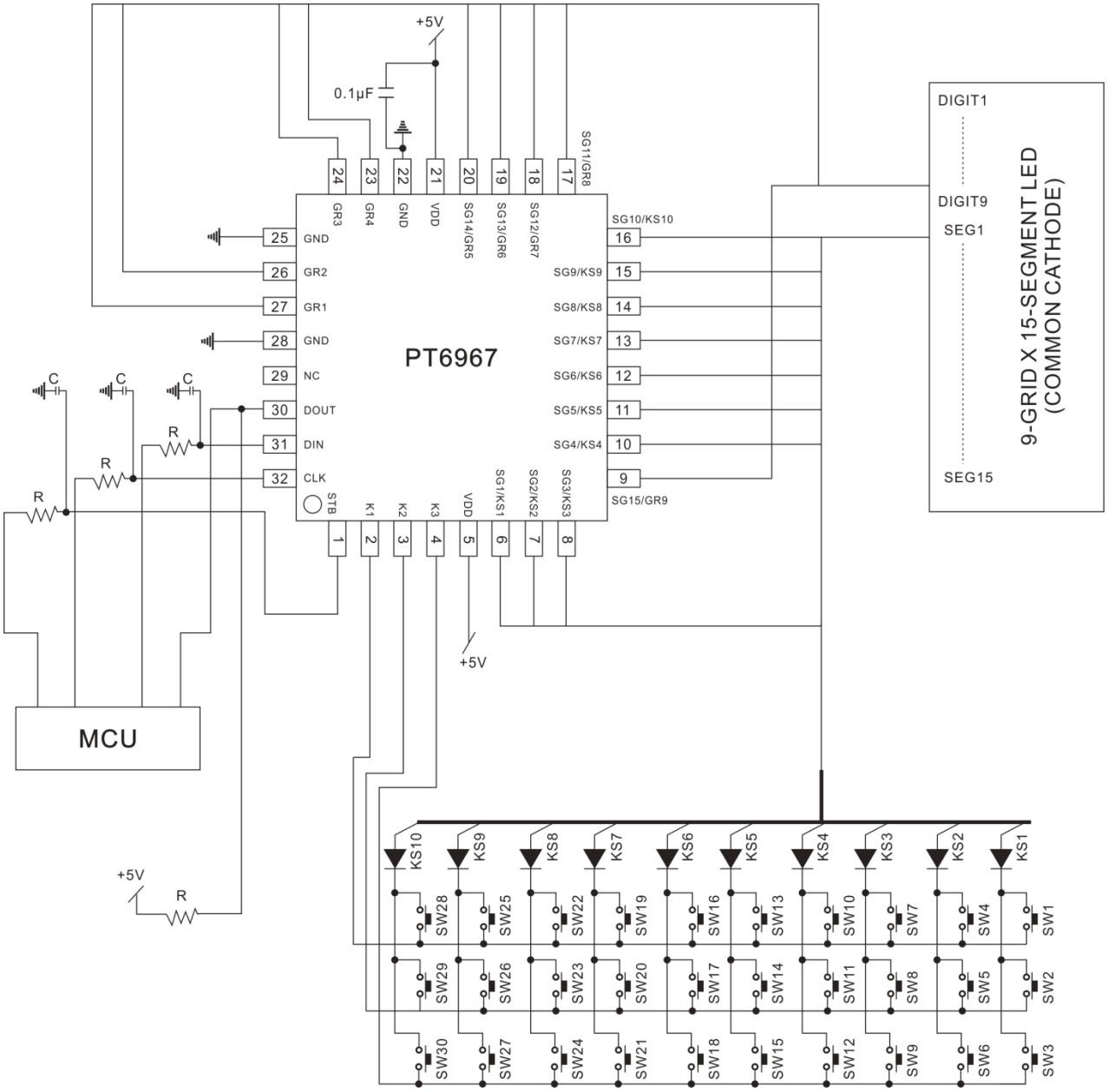


APPLICATION CIRCUITS

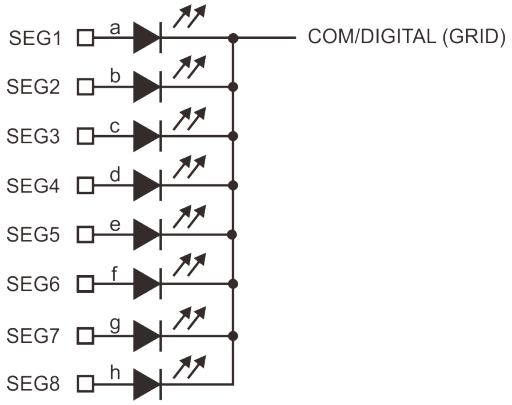


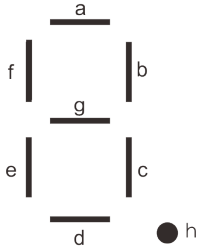
Notes:

1. The capacitor (0.1μF) connected between the GND and the VDD pins must be located as close as possible to the PT6967 chip.
2. It is strongly suggested that the NC pin be connected to the GND.
3. The PT6967 power supply is separate from the application system power supply.
4. DOUT pull high resistor 10KΩ≧R≧1KΩ
5. Input resistor 10KΩ≧R≧1KΩ and capacitor 100pF≧C≧10pF



COMMON CATHODE TYPE LED PANEL



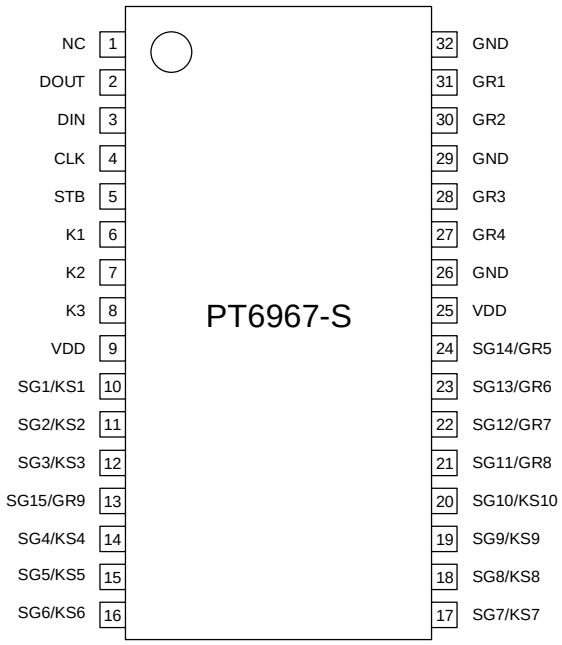


ORDER INFORMATION

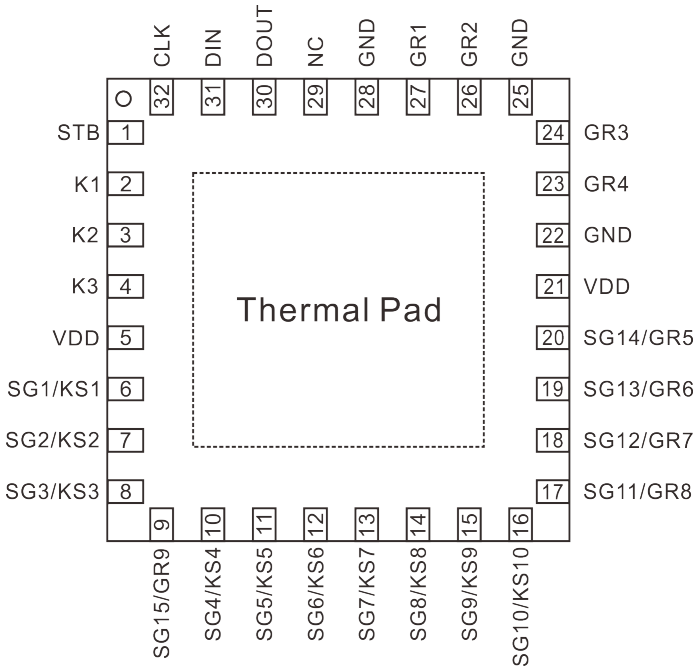
Valid Part Number	Package Type	Top Code
PT6967-S	32 pins, SOP, 300mil	PT6967-S
PT6967	32 pins, QFN	PT6967

PIN DESCRIPTION

SOP



QFN



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.	
			SOP	QFN
NC	-	No Connect	1	29
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock.	2	30
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	3	31
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	4	32
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is “HIGH", CLK is ignored.	5	1
K1 ~ K3	I	Key Data Input Pins The data sent to these pins are latched at the end of the display cycle. (Internal Pull-Low Resistor)	6, 7, 8	2, 3. 4
VDD	-	Power Supply	9, 25	5, 21
SG1/KS1 ~ SG10/KS10	O	Segment Output Pins (p-channel, open drain) Also acts as the Key Source	10 ~ 12 14 ~ 20	6 ~ 8 10 ~ 16
SG15/GR9	O	Segment / Grid Output Pins	13	9
SG11/GR8	O	Segment / Grid Output Pins	21	17
SG12/GR7 ~ SG14/GR5	O	Segment / Grid Output Pins	22, 23, 24	18 ~ 20
GND	-	Ground Pin	26, 29, 32	22, 25, 28
GR4 ~ GR1	O	Grid Output Pins	27, 28, 30, 31	23, 24, 26, 27
Thermal Pad	-	Thermal pad for enhanced thermal performance. Should be soldered to the PCB (connected to board ground)	-	Chip Back-Side

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
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