



## 800V N-Channel MOSFET

Lead Free Package and Finish

### General Features

- Proprietary New Planar Technology
- $R_{DS(ON),typ.}=1.5\ \Omega @ V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

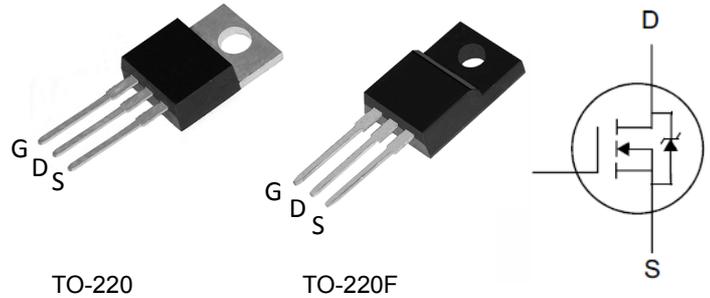
$BV_{DSS}$	$R_{DS(ON),typ.}$	$I_D$
800V	1.5Ω	7.0A

### Applications

- Adaptor
- LCD Panel Power
- Other Applications

### Ordering Information

Part Number	Package	Brand
PTP07N80	TO-220	
PTA07N80	TO-220F	



Package Not to Scale

### Absolute Maximum Ratings

$T_C=25\ ^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	PTP07N80	PTA07N80	Unit
$V_{DSS}$	Drain-to-Source Voltage <sup>[1]</sup>	800		V
$V_{GSS}$	Gate-to-Source Voltage	±30		
$I_D$	Continuous Drain Current	7.0		A
$I_D @ T_C=100\ ^\circ\text{C}$	Continuous Drain Current @ $T_C=100\ ^\circ\text{C}$	Figure 3		
$I_{DM}$	Pulsed Drain Current at $V_{GS}=10V$ <sup>[2]</sup>	Figure 6		
$E_{AS}$	Single Pulse Avalanche Energy	580		mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ <sup>[3]</sup>	5.0		V/ns
$P_D$	Power Dissipation	150	40	W
	Derating Factor above $25\ ^\circ\text{C}$	1.2	0.32	
$T_L$ $T_{PAK}$	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260		$^\circ\text{C}$
$T_J$ & $T_{STG}$	Operating and Storage Temperature Range	-55 to 150		

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

### Thermal Characteristics

Symbol	Parameter	PTP07N80	PTA07N80	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.83	3.125	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	100	



## Electrical Characteristics

### OFF Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	800	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	1	$\mu A$	$V_{DS}=800V, V_{GS}=0V$
		--	--	100		$V_{DS}=640V, V_{GS}=0V, T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Leakage Current	--	--	+100	$nA$	$V_{GS}=+30V, V_{DS}=0V$
		--	--	-100		$V_{GS}=-30V, V_{DS}=0V$

### ON Characteristics

$T_J = 25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance <sup>[4]</sup>	--	1.5	1.8	$\Omega$	$V_{GS}=10V, I_D=3.5A$
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
gfs	Forward Transconductance <sup>[4]</sup>	--	5.5	--	S	$V_{DS}=30V, I_D=7.0A$

### Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$C_{iss}$	Input Capacitance	--	1350	--	$pF$	$V_{GS}=0V, V_{DS}=25V, f=1.0MHz$
$C_{rss}$	Reverse Transfer Capacitance	--	12	--		
$C_{oss}$	Output Capacitance	--	120	--		
$Q_g$	Total Gate Charge	--	34	--	$nC$	$V_{DD}=400V, I_D=7.0A, V_{GS}=0 \text{ to } 10V$
$Q_{gs}$	Gate-to-Source Charge	--	6.0	--		
$Q_{gd}$	Gate-to-Drain (Miller) Charge	--	14	--		

### Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	15	--	$nS$	$V_{DD}=400V, I_D=7.0A, V_{GS}=10V, R_G=12\Omega$
$t_{rise}$	Rise Time	--	25	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	50	--		
$t_{fall}$	Fall Time	--	30	--		



## Source-Drain Body Diode Characteristics

$T_J=25^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
$I_{SD}$	Continuous Source Current <sup>[4]</sup>	--	--	7.0	A	Integral PN-diode in MOSFET
$I_{SM}$	Pulsed Source Current <sup>[4]</sup>	--	--	28		
$V_{SD}$	Diode Forward Voltage	--	--	1.5	V	$I_S=7.0\text{A}$ , $V_{GS}=0\text{V}$
$t_{rr}$	Reverse recovery time	--	185	--	ns	$V_{GS}=0\text{V}$ , $I_F=7.0\text{A}$ , $di_F/dt=100\text{A}/\mu\text{s}$
$Q_{rr}$	Reverse recovery charge	--	0.85	--	$\mu\text{C}$	

### Note:

- [1]  $T_J=+25^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$   
[2] Repetitive rating; pulse width limited by maximum junction temperature.  
[3]  $I_{SD}=7.0\text{A}$   $di/dt < 100\text{A}/\mu\text{s}$ ,  $V_{DD} < BV_{DSS}$ ,  $T_J=+150^{\circ}\text{C}$ .  
[4] Pulse width  $\leq 380\mu\text{s}$ ; duty cycle  $\leq 2\%$ .



## Typical Characteristics

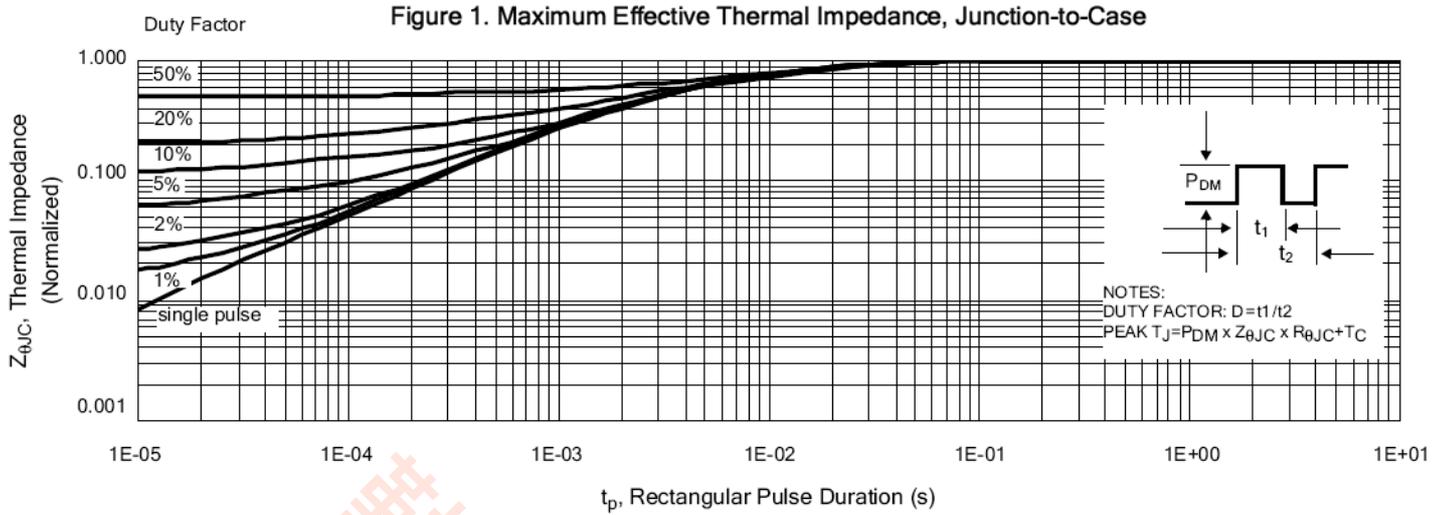


Figure 2. Maximum Power Dissipation vs Case Temperature

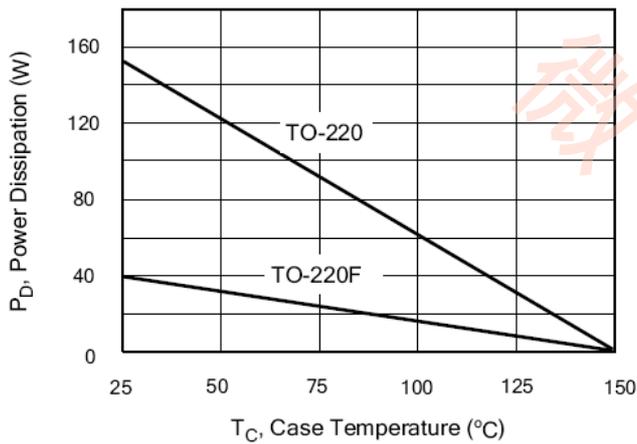


Figure 3. Maximum Continuous Drain Current vs Case Temperature

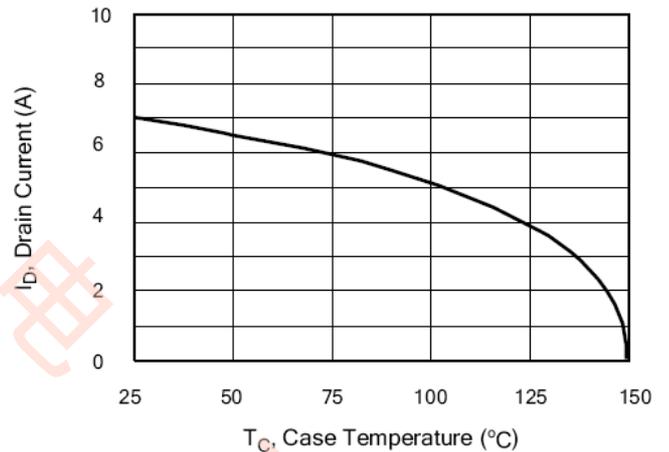


Figure 4. Typical Output Characteristics

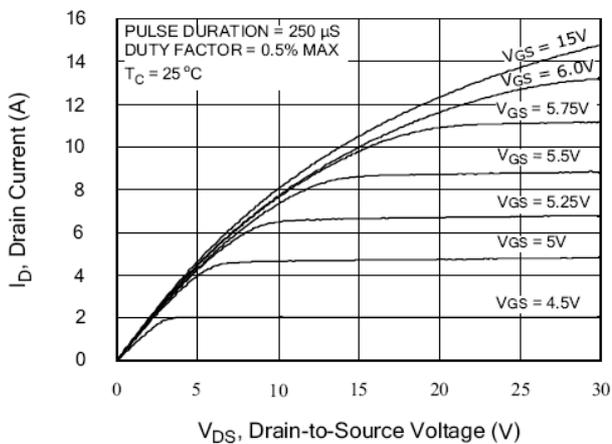
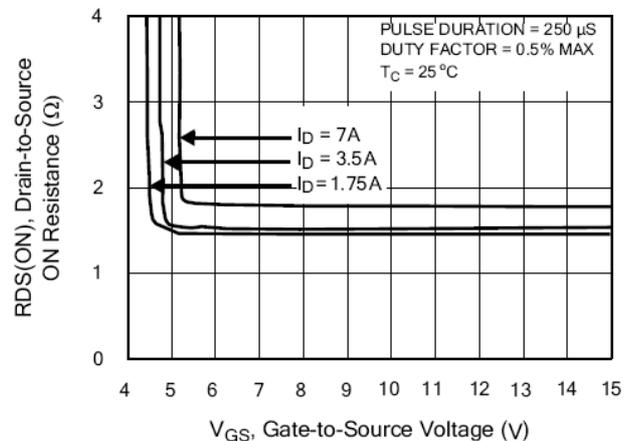


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current





## Typical Characteristics(Cont.)

Figure 6. Maximum Peak Current Capability

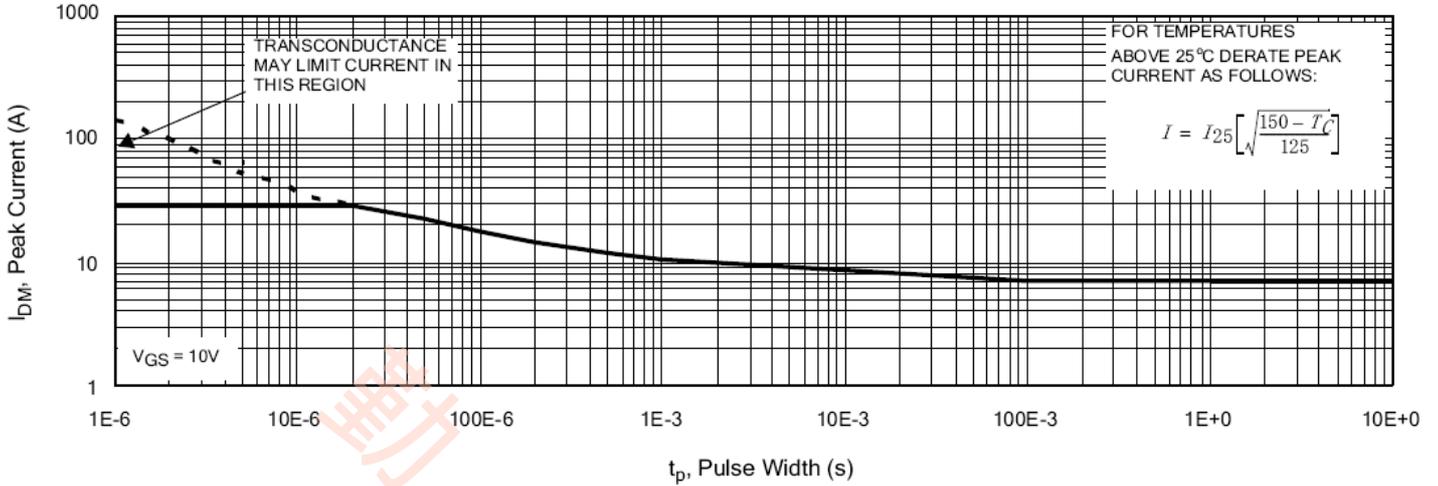


Figure 7. Typical Transfer Characteristics

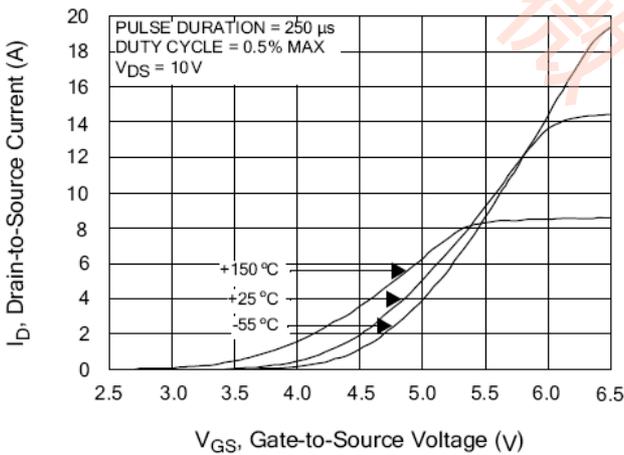


Figure 8. Unclamped Inductive Switching Capability

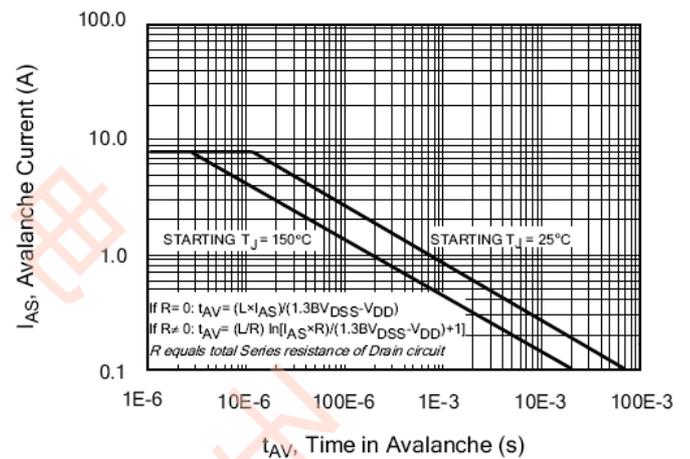


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

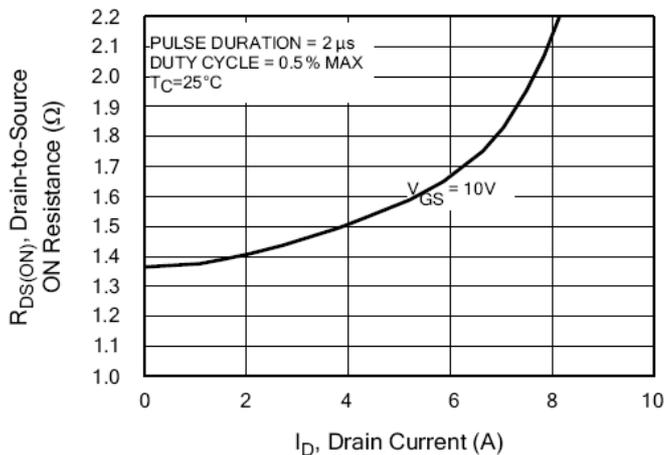
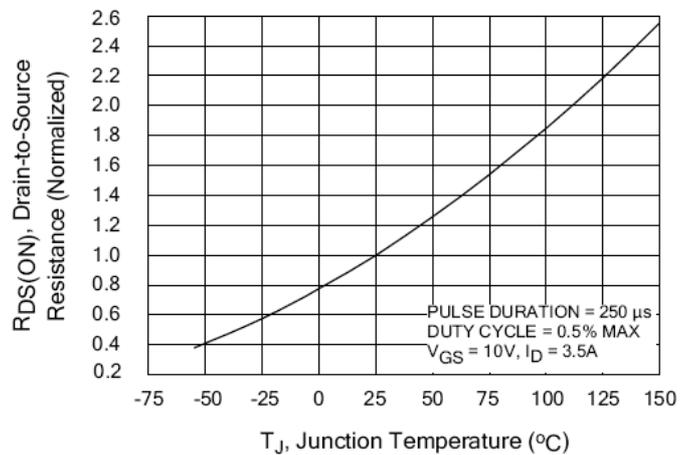


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature





## Typical Characteristics(Cont.)

Figure 11. Typical Breakdown Voltage vs Junction Temperature

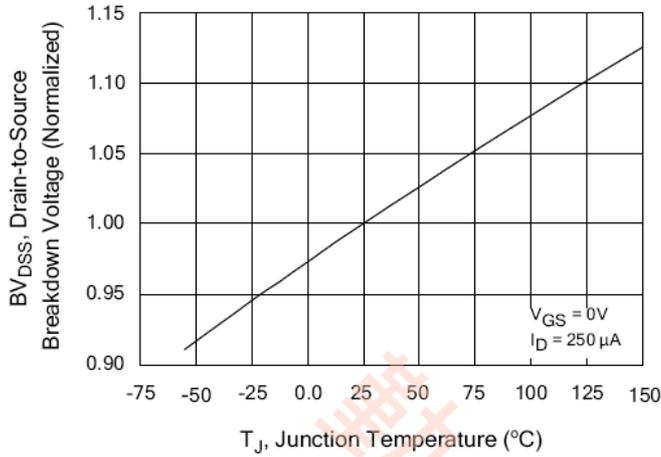


Figure 12. Typical Threshold Voltage vs Junction Temperature

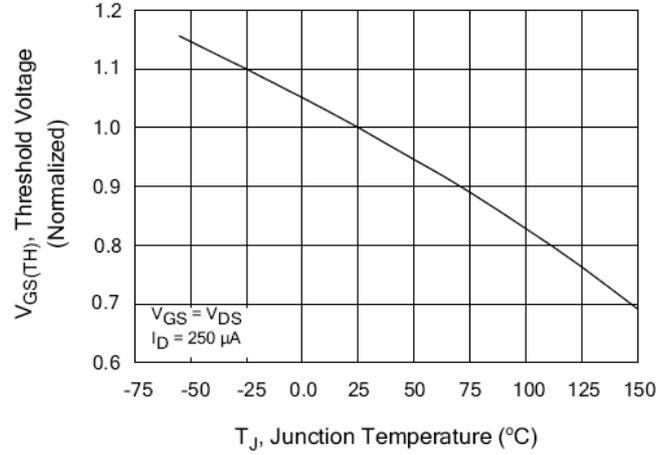


Figure 13. Maximum Forward Bias Safe Operating Area

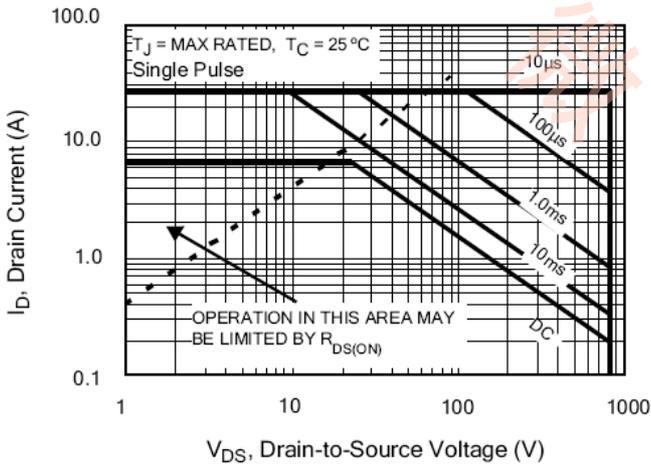


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

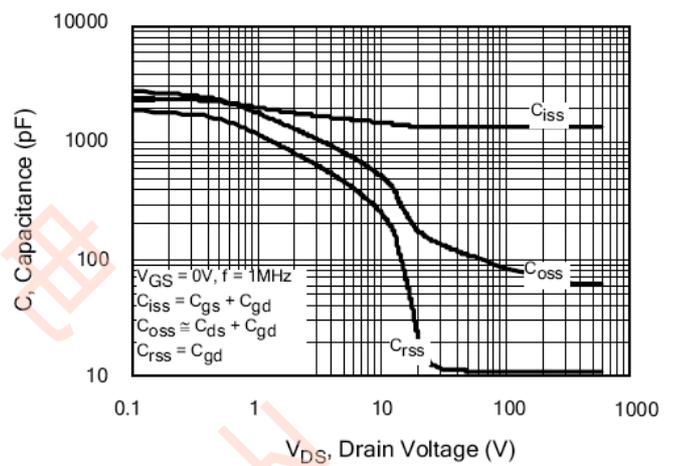


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

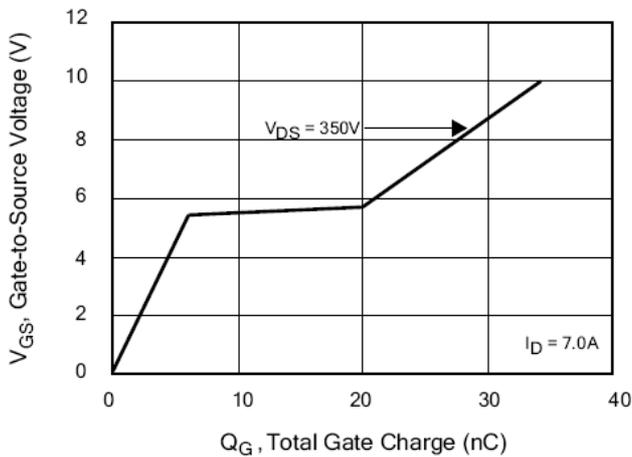
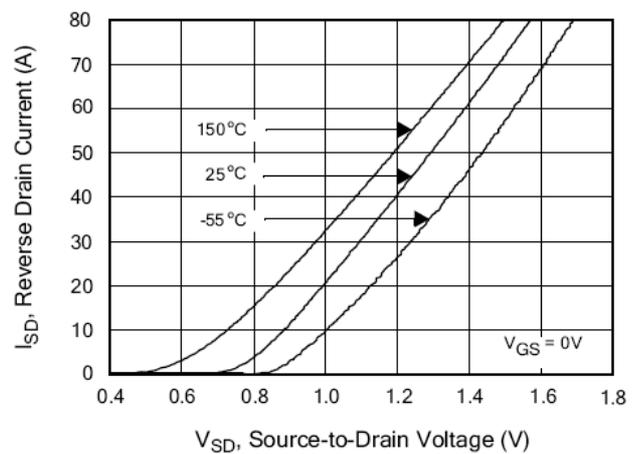


Figure 16. Typical Body Diode Transfer Characteristics





## Test Circuits and Waveforms

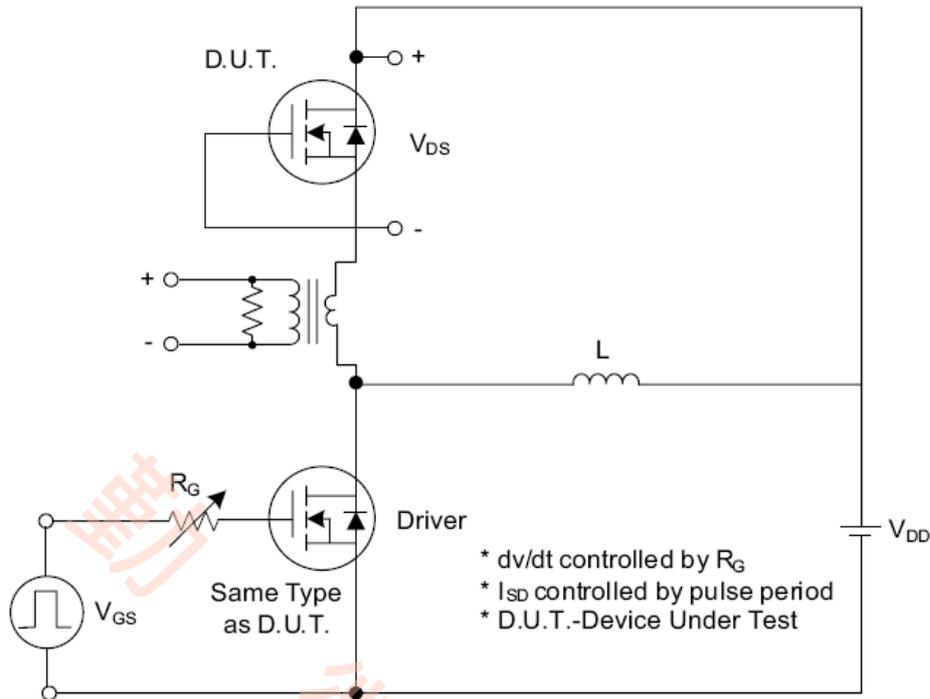


Fig. 1.1 Peak Diode Recovery  $dv/dt$  Test Circuit

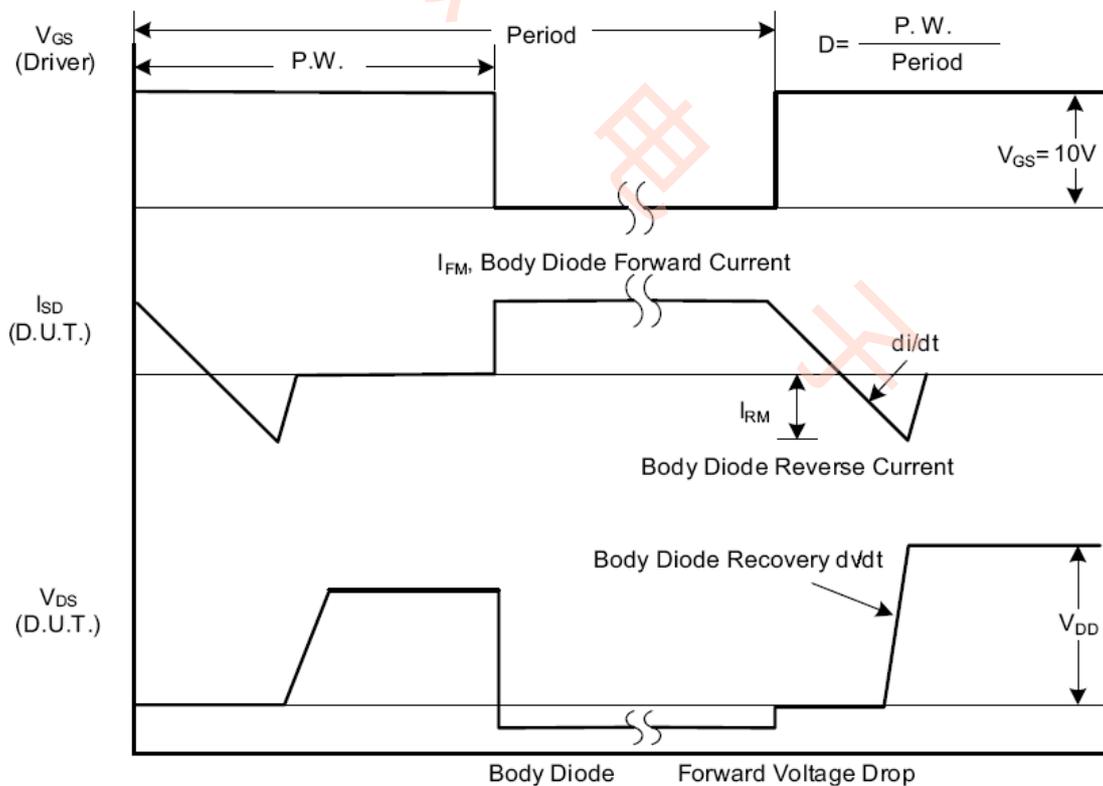


Fig. 1.2 Peak Diode Recovery  $dv/dt$  Waveforms



### Test Circuits and Waveforms (Cont.)

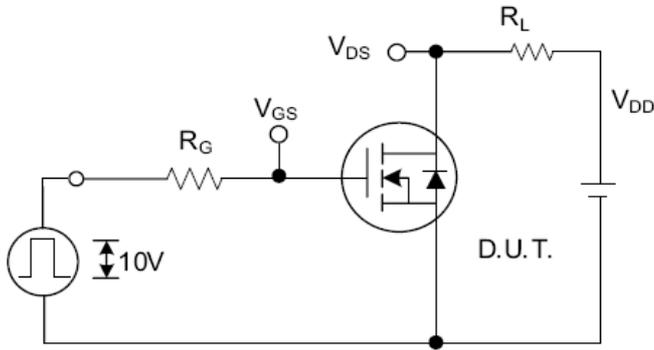


Fig. 2.1 Switching Test Circuit

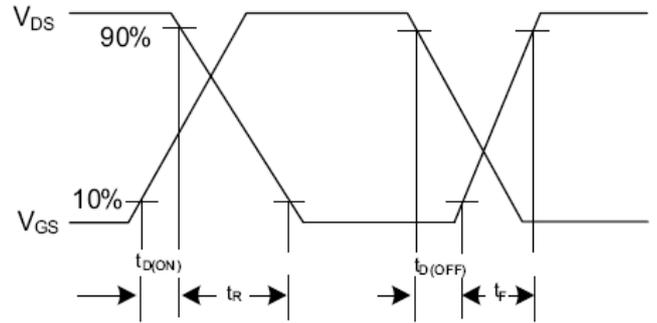


Fig. 2.2 Switching Waveforms

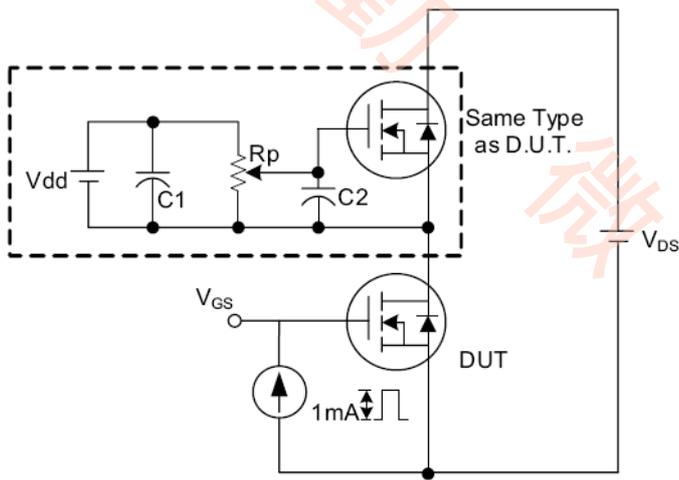


Fig. 3.1 Gate Charge Test Circuit

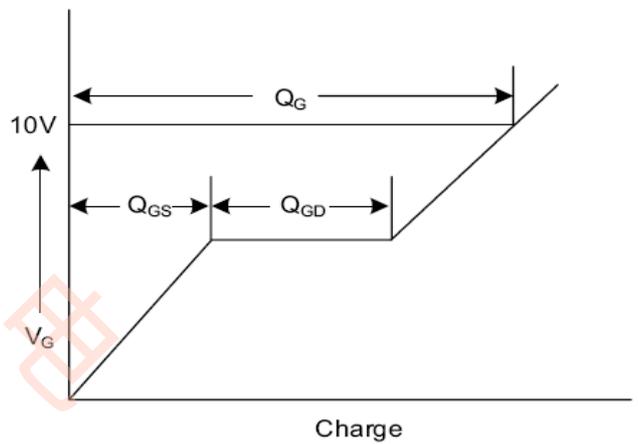


Fig. 3.2 Gate Charge Waveform

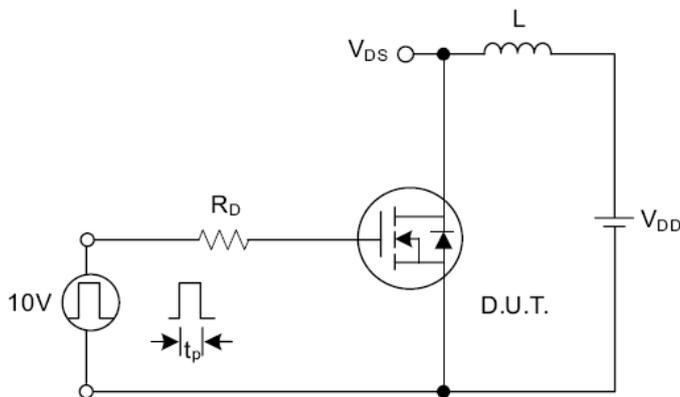


Fig. 4.1 Unclamped Inductive Switching Test Circuit

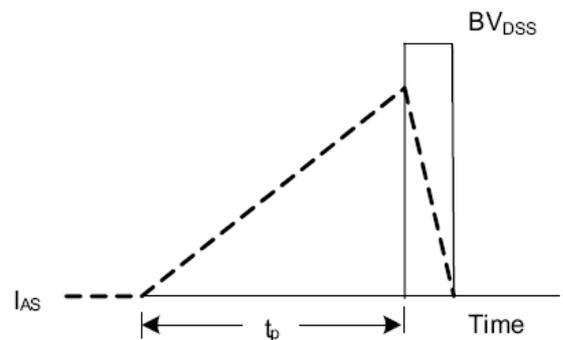


Fig. 4.2 Unclamped Inductive Switching Waveforms



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