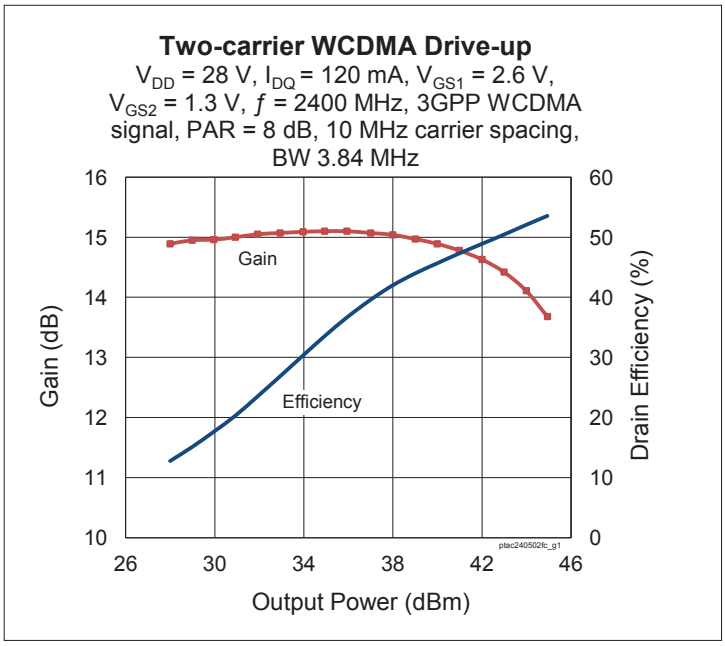
green Product

Thermally-Enhanced High Power RF LDMOS FET
50 W, 28 V, 2300 – 2400 MHz

Description

The PTAC240502FC is a 47-watt LDMOS FET with an asymmetrical design intended for use in multi-standard cellular power amplifier applications in the 2300 to 2400 MHz frequency band. Features include dual-path design, input matching, high gain and thermally-enhanced package with earless flanges. Manufactured with Infineon's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



PTAC240502FC
Package H-37248-4

Features

- Input matched
- Asymmetric Doherty design
  - Main: P1dB = 17 W Typ
  - Peak: P1dB = 33 W Typ
- Typical Pulsed CW performance, 2350 MHz, 28 V, 160 µs pulse width, 10% duty cycle, Doherty Configuration
  - Output power at P_{1dB} = 45.7 W
  - Efficiency = 46.2%
  - Gain = 14.6 dB
- Typical single-carrier WCDMA performance, 2350 MHz, 28 V, 8.4 dB PAR @ 0.01% CCDF
  - Output power = 8.91 W
  - Efficiency = 44.2%
  - Gain = 14.2 dB
  - ACPR = –31 dBc @ 5 MHz
- Capable of handling 10:1 VSWR @28 V, 50 W (CW) output power
- Integrated ESD protection : Human Body Model, Class 1B (per JESD22-A114)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Two-carrier WCDMA Specifications (tested in Infineon Doherty test fixture)
V_{DD} = 28 V, I_{DQ} = 120 mA, P_{OUT} = 10 W avg, V_{GS2} = 1.3 V, f_1 = 2345 MHz, f_2 = 2355 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 8 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Linear Gain	G_{ps}	13	14.3	—	dB
Drain Efficiency	η_D	41	44	—	%
Intermodulation Distortion	IMD	—	–33	–25	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10	µA
On-State Resistance (main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.4	—	Ω
(peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.2	—	Ω
Operating Gate Voltage (main)	V_{DS} = 28 V, I_{DQ} = 120 mA	V_{GS}	2.6	2.7	2.8	V
(peak)	V_{DS} = 28 V, I_{DQ} = 0 mA	V_{GS}	1.2	1.3	1.5	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1	µA

Maximum Ratings

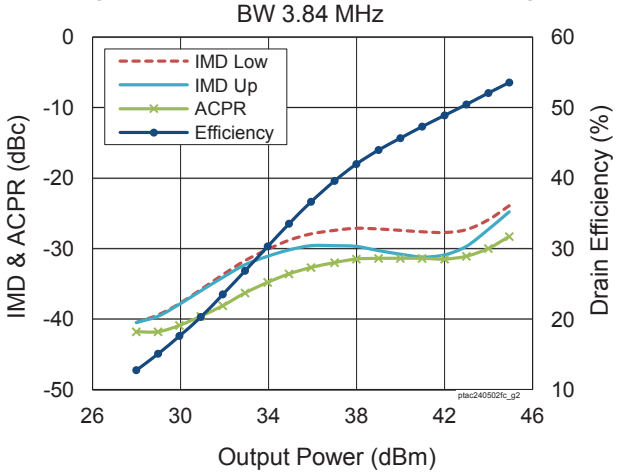
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–6 to +10	V
Operating Voltage	V_{DD}	0 to +32	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C
Thermal Resistance (T_{CASE} = 60°C, 50 W CW)	$R_{\theta JC}$	1.29	°C/W

Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTAC240502FC V1 R0	PTAC240502FCV1R0XTMA1	H-37248-4, earless flange	Tape & Reel, 50 pcs
PTAC240502FC V1 R250	PTAC240502FCV1R250XTMA1	H-37248-4, earless flange	Tape & Reel, 250 pcs

Typical Performance (data taken in a production test fixture)

Two-carrier WCDMA Drive-up
V_{DD} = 28 V, I_{DQ} = 120 mA, V_{GS1} = 2.6 V, V_{GS2} = 1.3 V, f = 2400 MHz, 3GPP WCDMA signal, PAR = 8 dB, 10 MHz carrier spacing, BW 3.84 MHz



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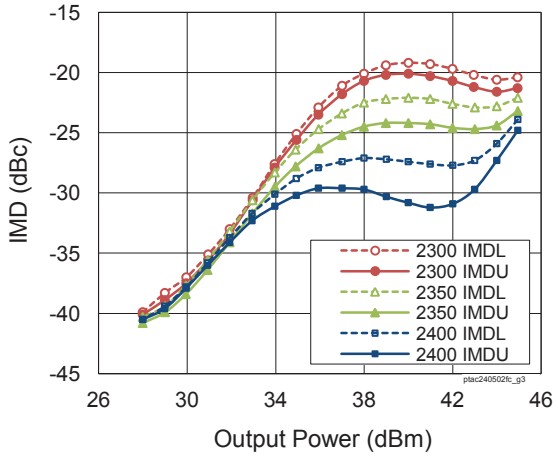
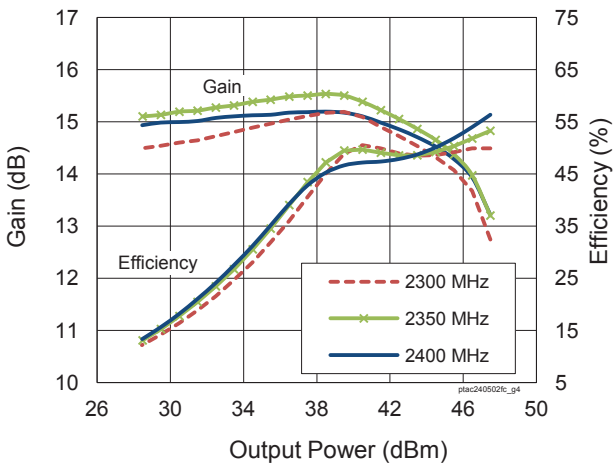
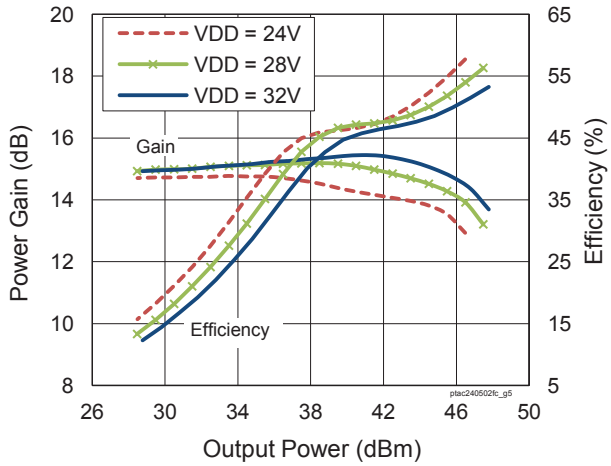


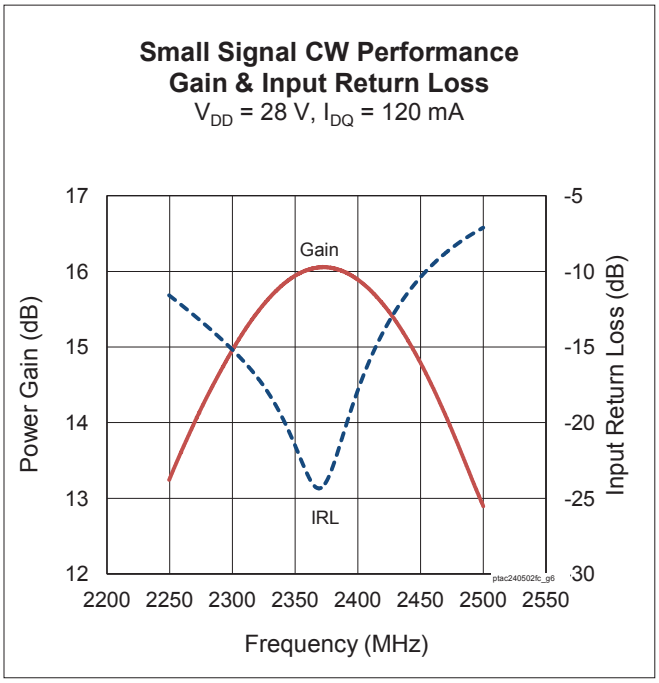
CW Performance
V_{DD} = 28 V, I_{DQ} = 120 mA



CW Performance at various V_{DD}
I_{DQ} = 120 mA, f = 2400 MHz



Typical Performance (cont.)



Load Pull Performance

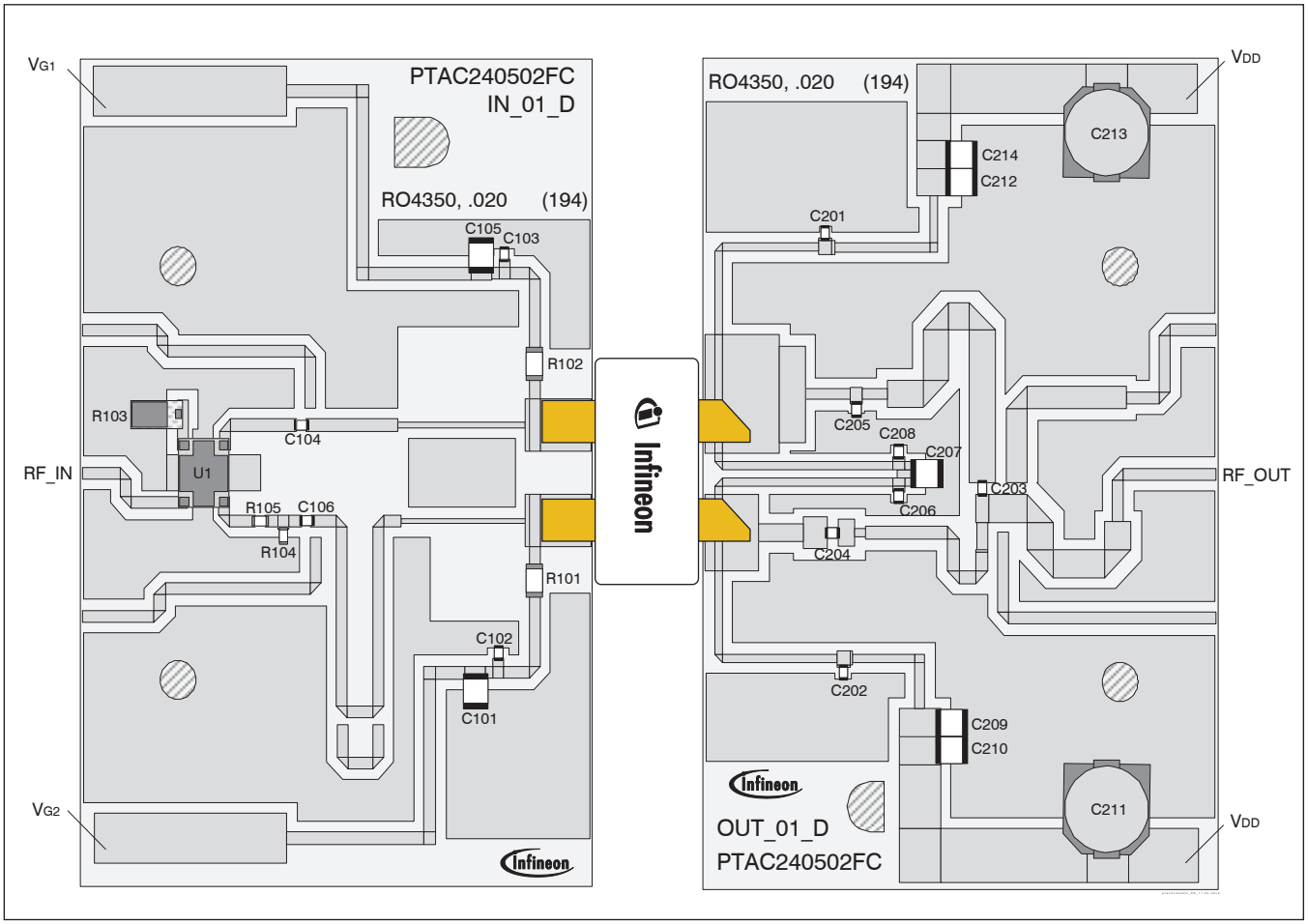
Main Side Load Pull Performance – Pulsed CW signal: 160 µs, 10% duty cycle, 28 V, 114 mA

		P_{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	ZI [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	ZI [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
2300	10–j31	9.4–j11.6	20.96	42.89	19.45	53.2	4.7–j8.3	22.8	41.03	12.68	61.5
2350	12.7–j35	9.7–j12.2	20.7	42.83	19.19	52.7	5.1–j9.4	22.4	41.34	13.61	62.1
2400	16.2–j38	9.31–j12.6	20.8	42.65	18.41	52.6	5.2–j10.2	22.2	41.45	13.96	61.3

Peak Side Load Pull Performance – Pulsed CW signal: 160 µs, 10% duty cycle, 28 V, 252 mA

		P_{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	ZI [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	ZI [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
2300	5.6–j22	3.0–j7.0	18.2	46.50	44.67	52.1	2.2–j5.8	20.5	45.20	33.11	56.9
2350	6.7–j25	2.9–j7.9	17.4	46.46	44.26	48.5	2.2–j5.9	21.1	44.91	30.97	55.9
2400	9.7–j29	3.3–j7.9	17.9	46.62	45.92	49.6	2.2–j6.2	20.8	45.31	33.96	57.2

Reference Circuit , 2300 – 2400 MHz



Reference circuit assembly diagram (not to scale)

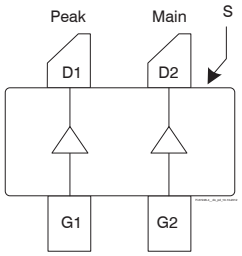
Reference Circuit (cont.)

Reference Circuit Assembly	
DUT	PTAC240502FC V1
Test Fixture Part No.	LTA/PTAC240502FC V1
PCB	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, ε_r = 3.66, f = 2300 – 2400 MHz
Find Gerber files for this test fixture on the Infineon Web site at *http://www.infineon.com/rfpower*	

Components Information

Component	Description	Suggested Manufacturer	P/N
Input			
C101, C105	Capacitor, 4.7 µF	Murata Electronics North America	GRM32ER71H475KA88L
C102, C103, C104, C106	Capacitor, 18 pF	ATC	ATC800A180JT250T
R101, R102	Resistor, 10 Ω	Panasonic Electronic Components	ERJ-8GEYJ100V
R103	Resistor, 50 Ω	Anaren	060120A15Z50
R104	Resistor, 300 Ω	Venkel	CR0603-16W-3010FB
R105	Resistor, 12.1 Ω	Venkel	CR0603-16W-12R1FB
U1	Directional coupler	Anaren	X3C25P1-05S
Output			
C201, C202, C203, C204, C206, C208	Capacitor, 18 pF	ATC	ATC800A180JT250T
C205	Capacitor, 0.5 pF	ATC	ATC800A180JT250T
C207, C210, C214	Capacitor, 4.71 µF	Murata Electronics North America	GRM32ER71H475KA88L
C209, C212	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T
C211, C213	Capacitor, 100 µF	Panasonic Electronic Components	EEE-FP1V101AP

Pinout Diagram (top view)



Pin	Description
D1	Drain device 1 (Peak)
D2	Drain device 2 (Main)
G1	Gate device 1 (Peak)
G2	Gate device 2 (Main)
S	Source (flange)

Lead connections for PTAC240502FC

Package Outline Specifications

Package H-37248-4

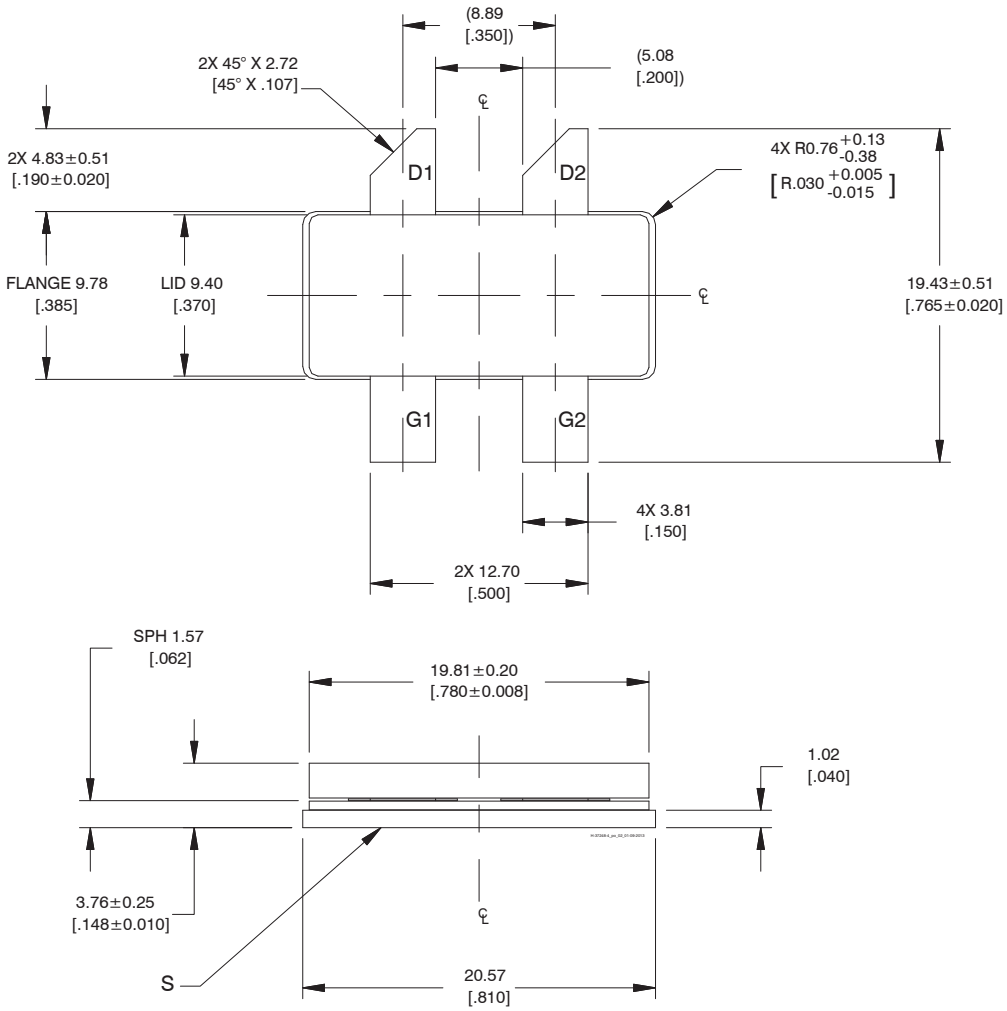


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: D1, D2 – drains; G1, G2 – gates; S – source.
5. Lead thickness: 0.10 + 0.076/–0.025 mm [0.004+0.003/–0.001 inch].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

Find the latest and most complete information about products and packaging at the Infineon Internet page http://www.infineon.com/rfpower

Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2013-07-16	Advance	All	Data Sheet reflects advance specification for product development
02	2013-11-13	Production	All	Data Sheet reflects released product specification
02.1	2013-11-27	Production	1	Revised ESD classification
02.2	2014-05-14	Production	2	Revised juntion temperature in Maximum Ratings table
02.3	2016-06-21	Production	2	Updated ordering information

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Edition 2016-06-21

Published by
Infineon Technologies AG
85579 Neubiberg, Germany

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