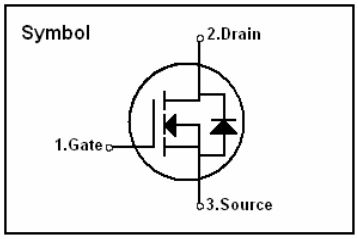
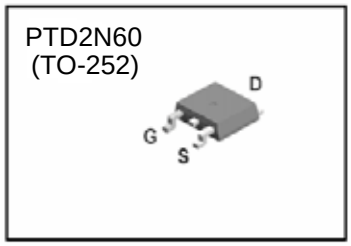
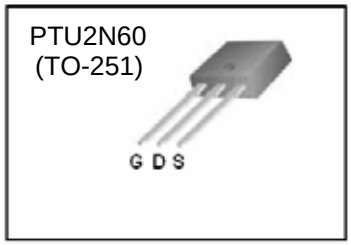
PHILOP
迪浦

PTD2N60/PTU2N60

600V N-Channel MOSFET







Features

- 1.9A, 600V, $R_{DS(on)}$ = 4.70Ω @V_{GS} = 10 V
- Low gate charge (typical 9nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

General Description

This Power MOSFET is produced using PHILOP's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency sw itched mode power supplies, active power factor correction based on half bridge topology.

Absolute Maximum Ratings

Symbol	Parameter		PTD2N60/ PTU2N60	Units
VDSS	Drain to Source Voltage		600	V
ID	Continuous Drain Current(@TC = 25°C)		1.9	A
	Continuous Drain Current(@TC = 100°C)		1.14	A
IDM	Drain Current Pulsed	(Note 1)	7.6	A
VGS	Gate to Source Voltage		±30	V
EAS	Single Pulsed Avalanche Energy	(Note 2)	120	mJ
EAR	Repetitive Avalanche Energy	(Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
PD	Total Power Dissipation(@TC = 25 °C)		44	W
	Derating Factor above 25 °C		0.35	W/ °C
TSTG, TJ	Operating Junction Temperature & Storage Temperature		-55 to +150	°C
TL	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.		300	°C

* Drain current limited by maximum junction temperature.

Thermal Characteristic

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	-	2.87	°C /W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient*	-	50	°C /W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	-	110	°C/W

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	600	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.7	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 480 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.95 A	--	3.6	4.7	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	200	--	pF
C_{oss}	Output Capacitance		--	20	--	pF
C_{rss}	Reverse Transfer Capacitance		--	4	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 2.0A, R_G = 25 Ω (Note 4, 5)	--	10	--	ns
t_r	Turn-On Rise Time		--	25	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	25	--	ns
t_f	Turn-Off Fall Time		--	30	--	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 2.0 A, V_{GS} = 10 V (Note 4, 5)	--	9	-	nC
Q_{gs}	Gate-Source Charge		--	1.5	--	nC
Q_{gd}	Gate-Drain Charge		--	4.0	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	1.9	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	7.6	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.9 A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 2.0 A, dI_F / dt = 100 A/μs (Note 4)	--	230	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.0	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 56 mH, I_{AS} = 2.0 A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 2.0 A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

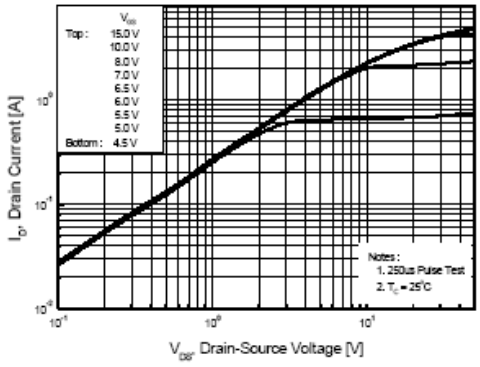


Figure 1. On-Region Characteristics

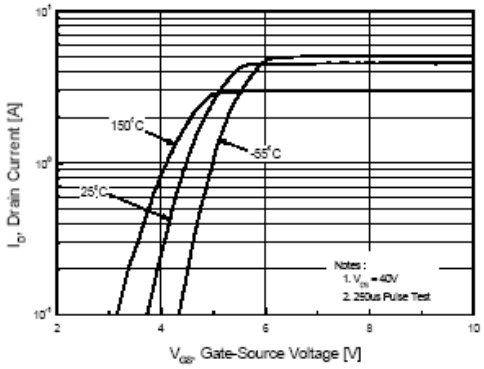


Figure 2. Transfer Characteristics

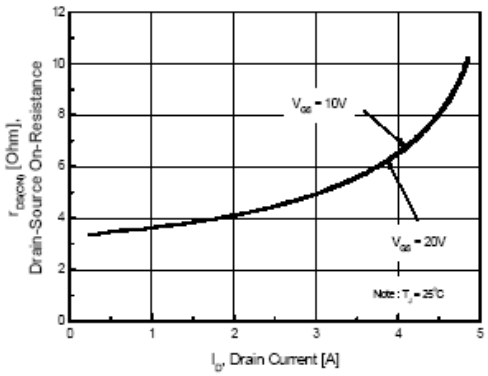


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

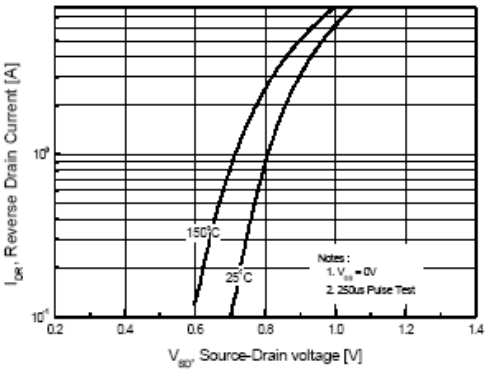


Figure 4. Body Diode Forward Voltage Variation with Source Current

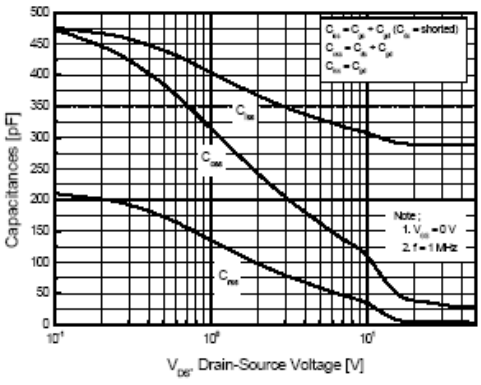


Figure 5. Capacitance Characteristics

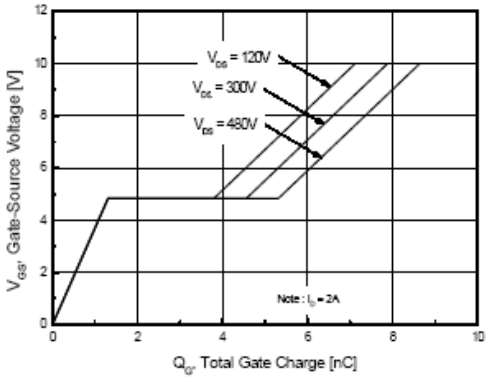


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

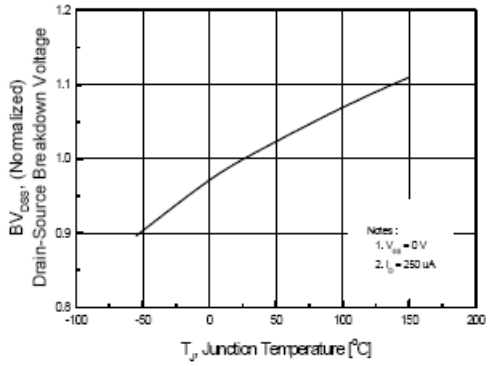


Figure 7. Breakdown Voltage Variation vs Temperature

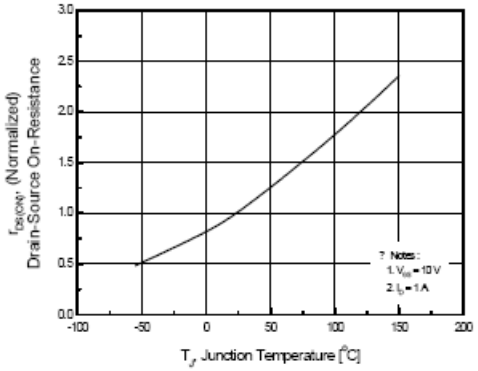


Figure 8. On-Resistance Variation vs Temperature

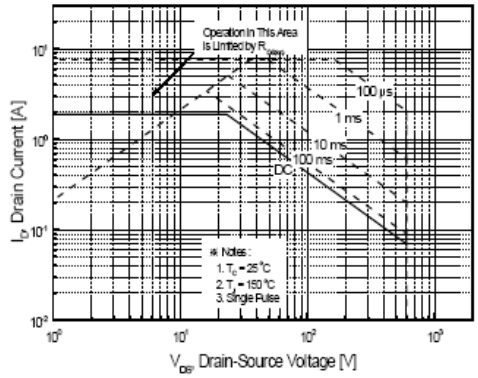


Figure 9. Maximum Safe Operating Area

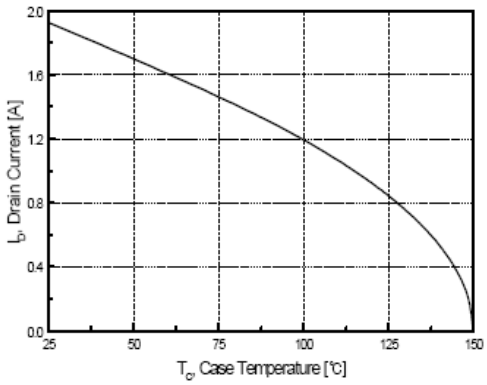


Figure 10. Maximum Drain Current vs Case Temperature

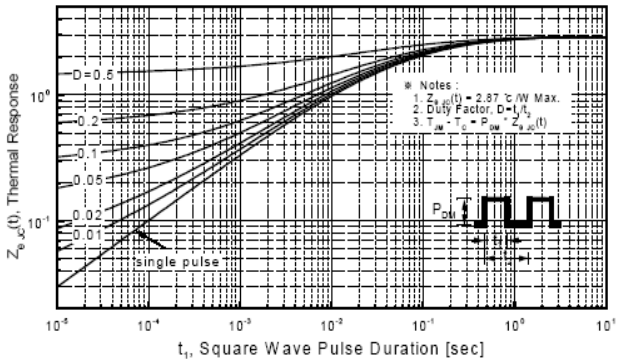


Figure 11. Transient Thermal Response Curve

Fig. 12. Gate Charge Test Circuit & Waveforms

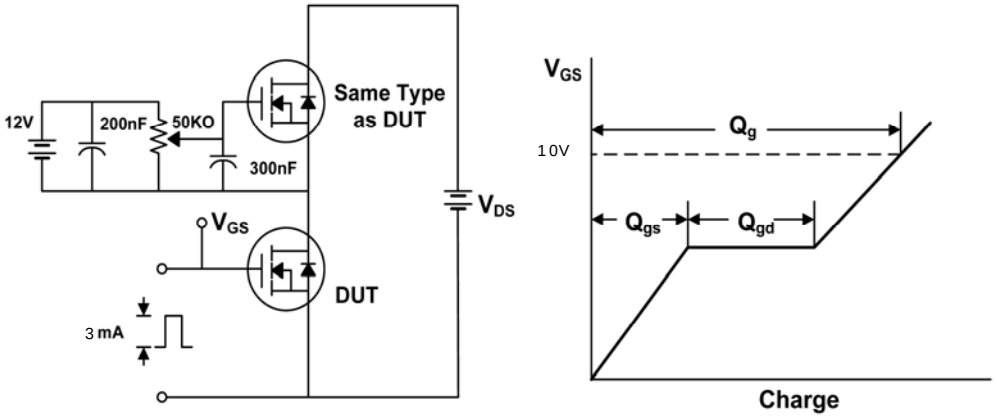


Fig 13. Switching Time Test Circuit & Waveforms

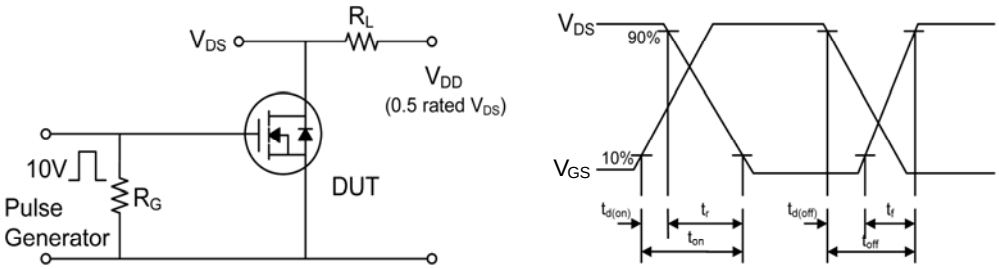
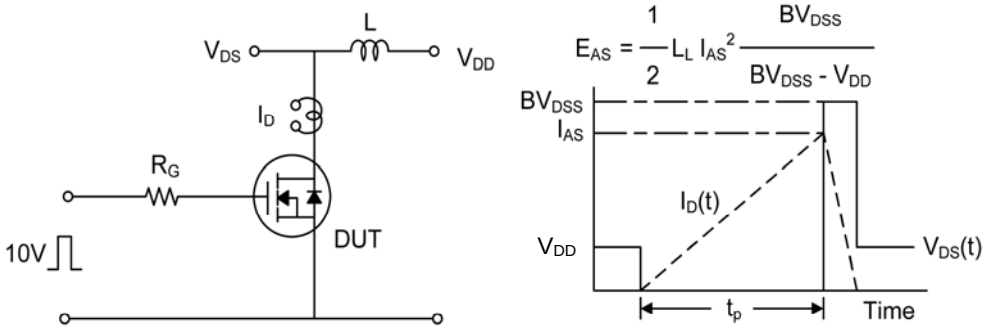


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms