



PTFA091201E
PTFA091201F
green
 Product

Thermally-Enhanced High Power RF LDMOS FETs 120 W, 920 – 960 MHz

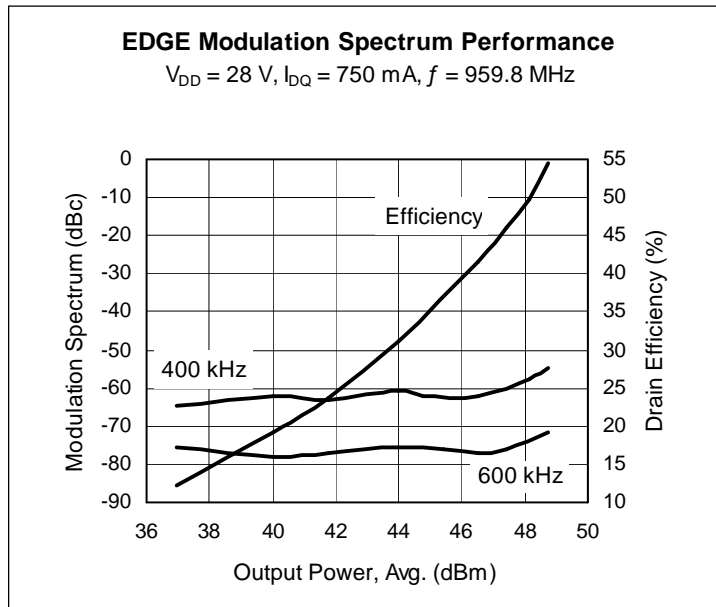
Description

The PTFA091201E and PTFA091201F are 120-watt LDMOS FETs designed for ultra-linear GSM/EDGE power amplifier applications in the 920 to 960 MHz band. Features include input and output matching, and thermally-enhanced packages with slotted or earless flanges. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA091201E
 Package H-36248-2



PTFA091201F
 Package H-37248-2



Features

- Thermally-enhanced packages
- Broadband internal matching
- Typical EDGE performance
 - Average output power = 50 W
 - Gain = 19.0 dB
 - Efficiency = 44%
- Typical CW performance
 - Output power at P-1dB = 135 W
 - Gain = 18.0 dB
 - Efficiency = 64%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Pb-free and RoHS compliant
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 28 V, 120 W (CW) output power

RF Characteristics

EDGE Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ} = 750\text{ mA}$, $P_{OUT} = 50\text{ W}$, $f = 959.8\text{ MHz}$

Characteristic	Symbol	Min	Typ	Max	Unit
Error Vector Magnitude	EVM (RMS)	—	2.5	—	%
Modulation Spectrum @ 400 kHz	ACPR	—	-62	—	dBc
Modulation Spectrum @ 600 kHz	ACPR	—	-74	—	dBc
Gain	G_{ps}	—	19	—	dB
Drain Efficiency	η_D	—	44	—	%

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (tested in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ} = 750\text{ mA}$, $P_{OUT} = 110\text{ W PEP}$, $f = 960\text{ MHz}$, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	18	19	—	dB
Drain Efficiency	η_D	45	48	—	%
Intermodulation Distortion	IMD	—	-31	-28	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1.0	μA
	$V_{DS} = 63\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10.0	μA
On-State Resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.07	—	Ω
Operating Gate Voltage	$V_{DS} = 28\text{ V}$, $I_{DQ} = 750\text{ mA}$	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1.0	μA

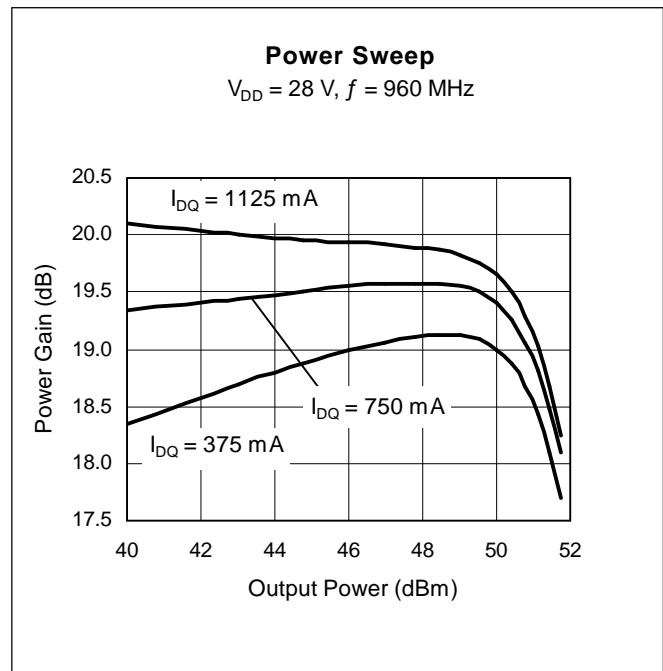
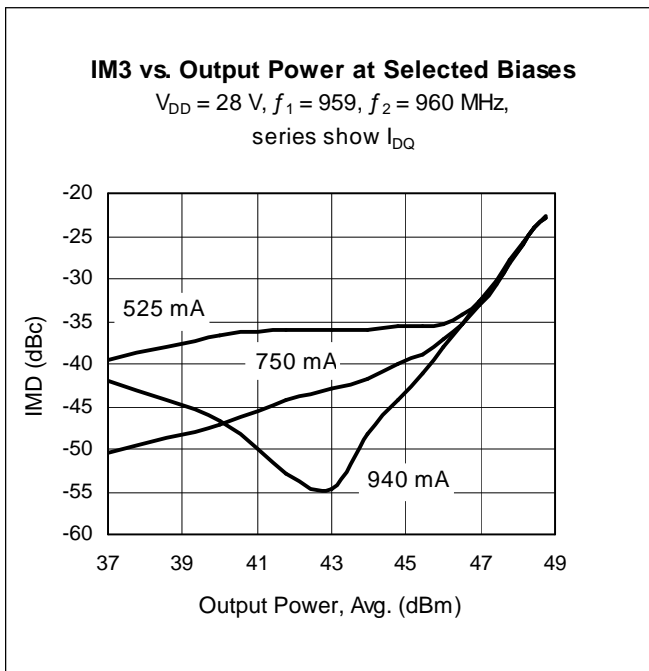
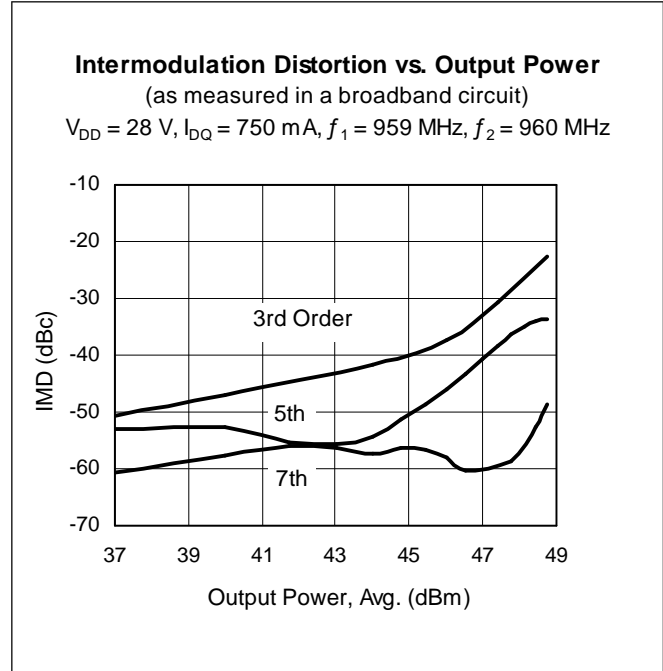
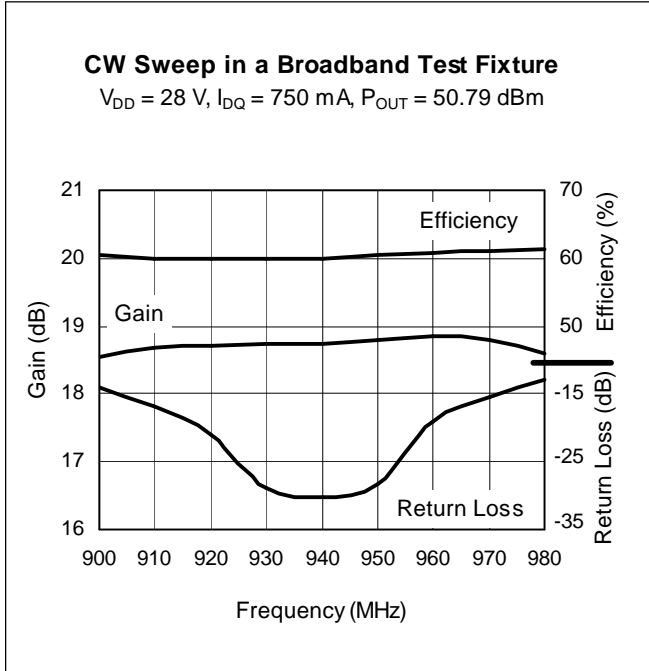
Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	-0.5 to +12	V
Junction Temperature	T_J	200	$^{\circ}\text{C}$
Total Device Dissipation	P_D	427	W
		Above 25 $^{\circ}\text{C}$ derate by	2.44
Storage Temperature Range	T_{STG}	-40 to +150	$^{\circ}\text{C}$
Thermal Resistance ($T_{CASE} = 70^{\circ}\text{C}$, 120 W CW)	$R_{\theta JC}$	0.41	$^{\circ}\text{C/W}$

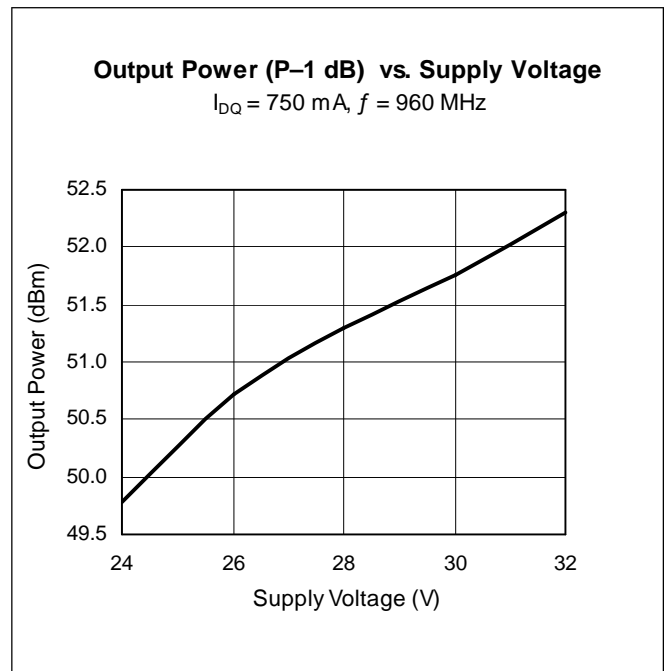
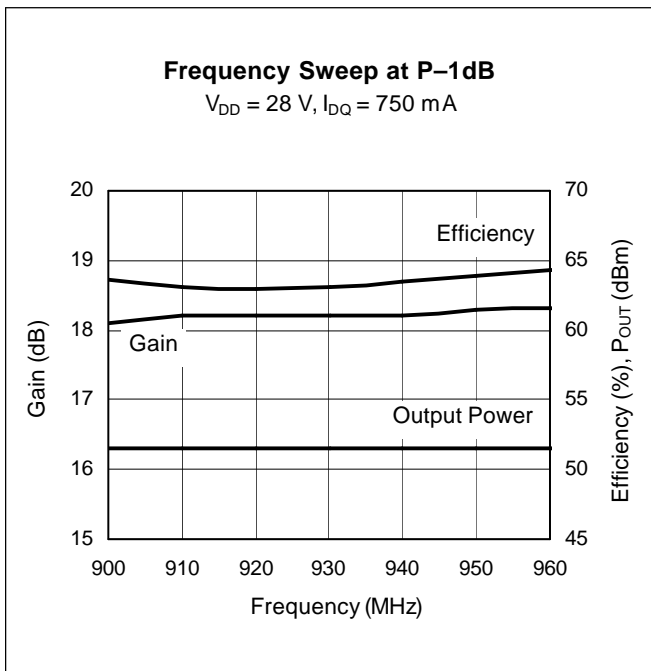
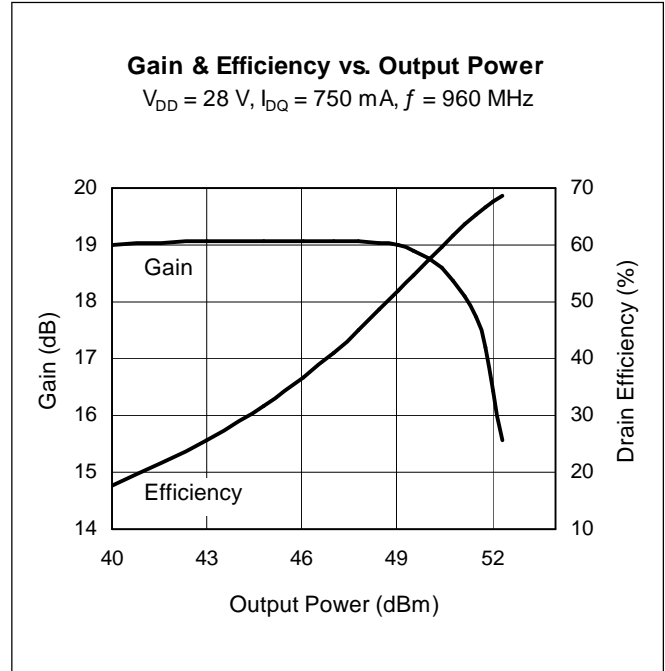
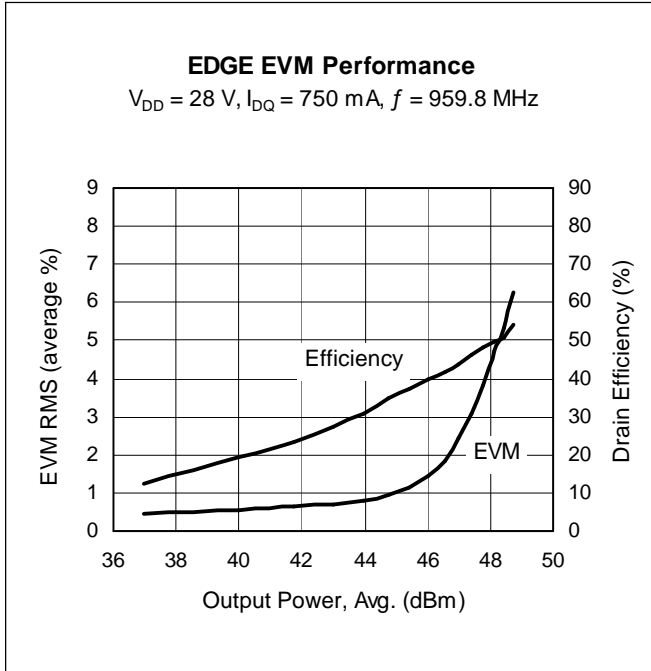
Ordering Information (see pages 9 and 10 for further information)

Type and Version	Package Type	Package Description	Marking
PTFA091201E V4	H-36248-2	Thermally-enhanced slotted flange, single-ended	PTFA091201E
PTFA091201F V4	H-37248-2	Thermally-enhanced earless flange, single-ended	PTFA091201F

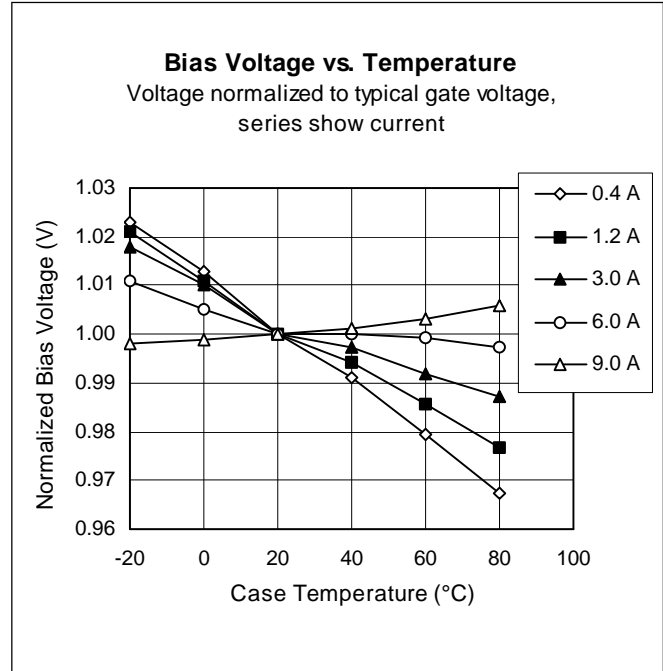
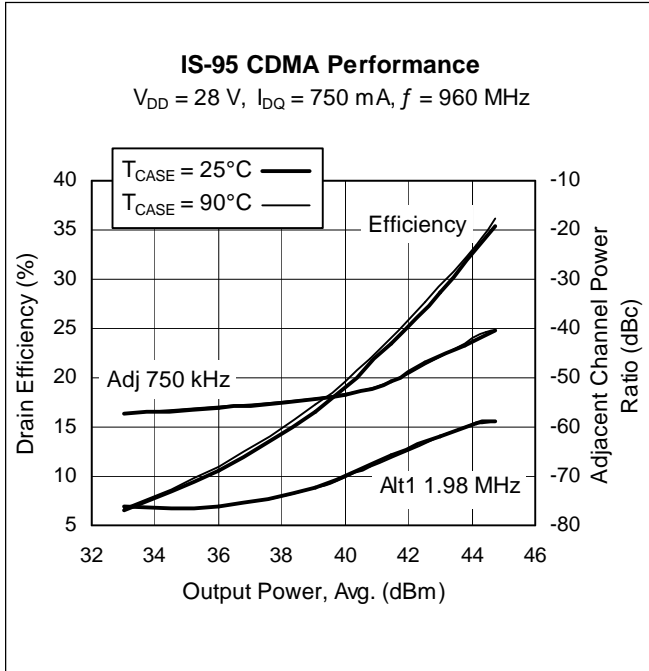
Typical Performance (data taken in a production test fixture)



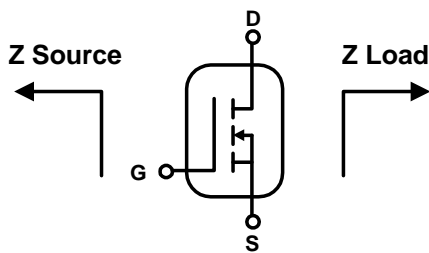
Typical Performance (cont.)



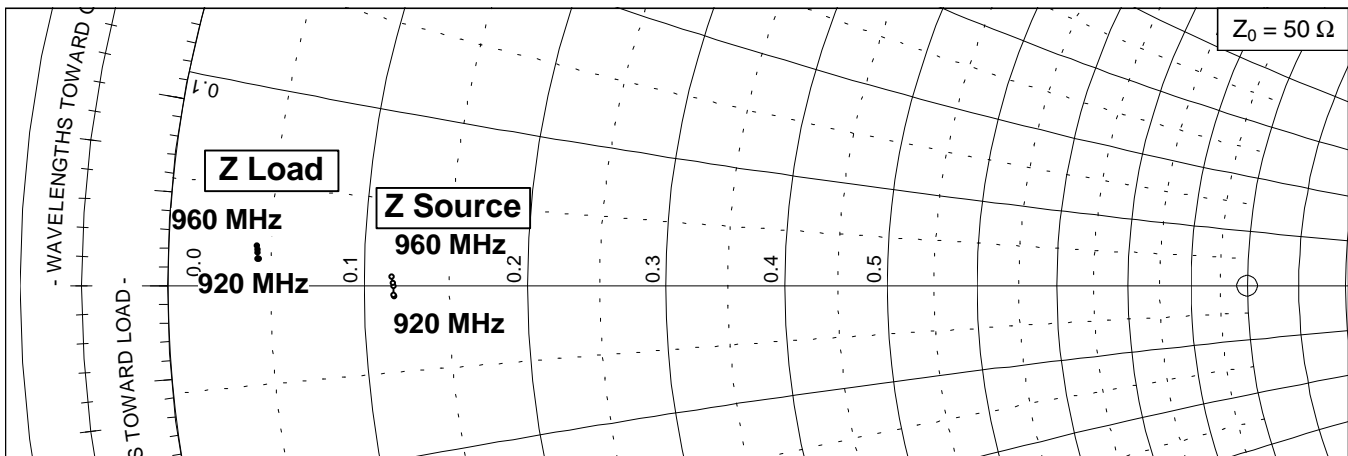
Typical Performance (cont.)



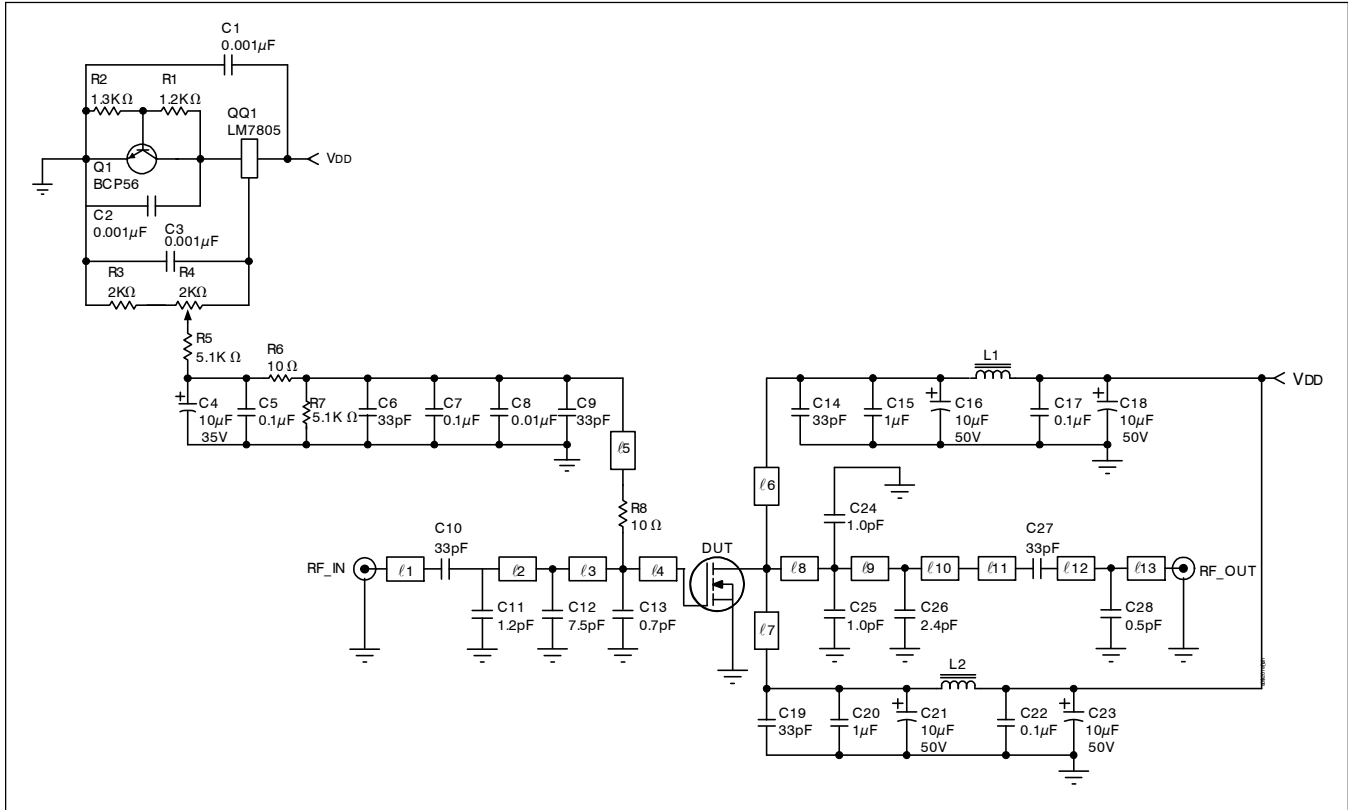
Broadband Circuit Impedance



Frequency MHz	Z Source W		Z Load W	
	R	jX	R	jX
920	5.86	-0.32	2.20	0.69
930	5.84	-0.27	2.17	0.69
940	5.85	-0.02	2.16	0.85
950	5.82	0.10	2.15	0.92
960	5.79	0.27	2.13	1.02



Reference Circuit



Reference circuit schematic for $f = 960 \text{ MHz}$

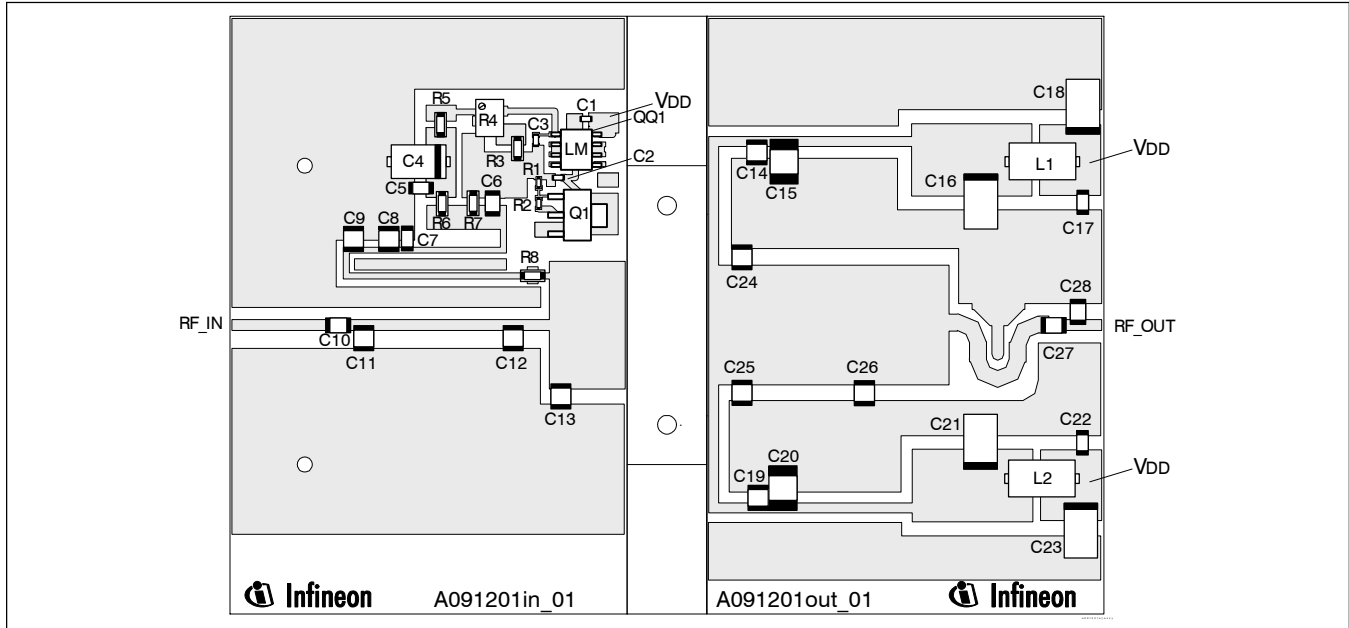
Circuit Assembly Information

DUT	PTFA091201E or PTFA091201F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, $\epsilon_r = 4.5$	Rogers TMM4	2 oz. copper

Microstrip	Electrical Characteristics at 960 MHz ¹	Dimensions: L x W (mm)	Dimensions: L x W (in.)
l_1	0.072λ , 50.0 Ω	12.27 x 1.40	0.483 x 0.055
l_2	0.115λ , 50.0 Ω	19.53 x 1.40	0.769 x 0.055
l_3	0.029λ , 50.0 Ω	5.08 x 1.40	0.200 x 0.055
l_4	0.062λ , 7.5 Ω	9.53 x 16.15	0.375 x 0.636
l_5	0.149λ , 70.0 Ω	26.31 x 0.71	1.036 x 0.028
l_6, l_7	0.122λ , 55.0 Ω	20.96 x 1.17	0.825 x 0.046
l_8	0.027λ , 7.9 Ω	4.06 x 15.24	0.160 x 0.600
l_9	0.103λ , 7.9 Ω	15.75 x 15.24	0.620 x 0.600
l_{10}	0.072λ , 7.9 Ω	11.02 x 15.24	0.434 x 0.600
l_{11}	0.155λ , 38.0 Ω	25.78 x 2.13	1.015 x 0.084
l_{12}	0.013λ , 50.0 Ω	2.24 x 1.40	0.088 x 0.055
l_{13}	0.015λ , 50.0 Ω	2.59 x 1.40	0.102 x 0.055

¹Electrical characteristics are rounded.

Reference Circuit (cont.)

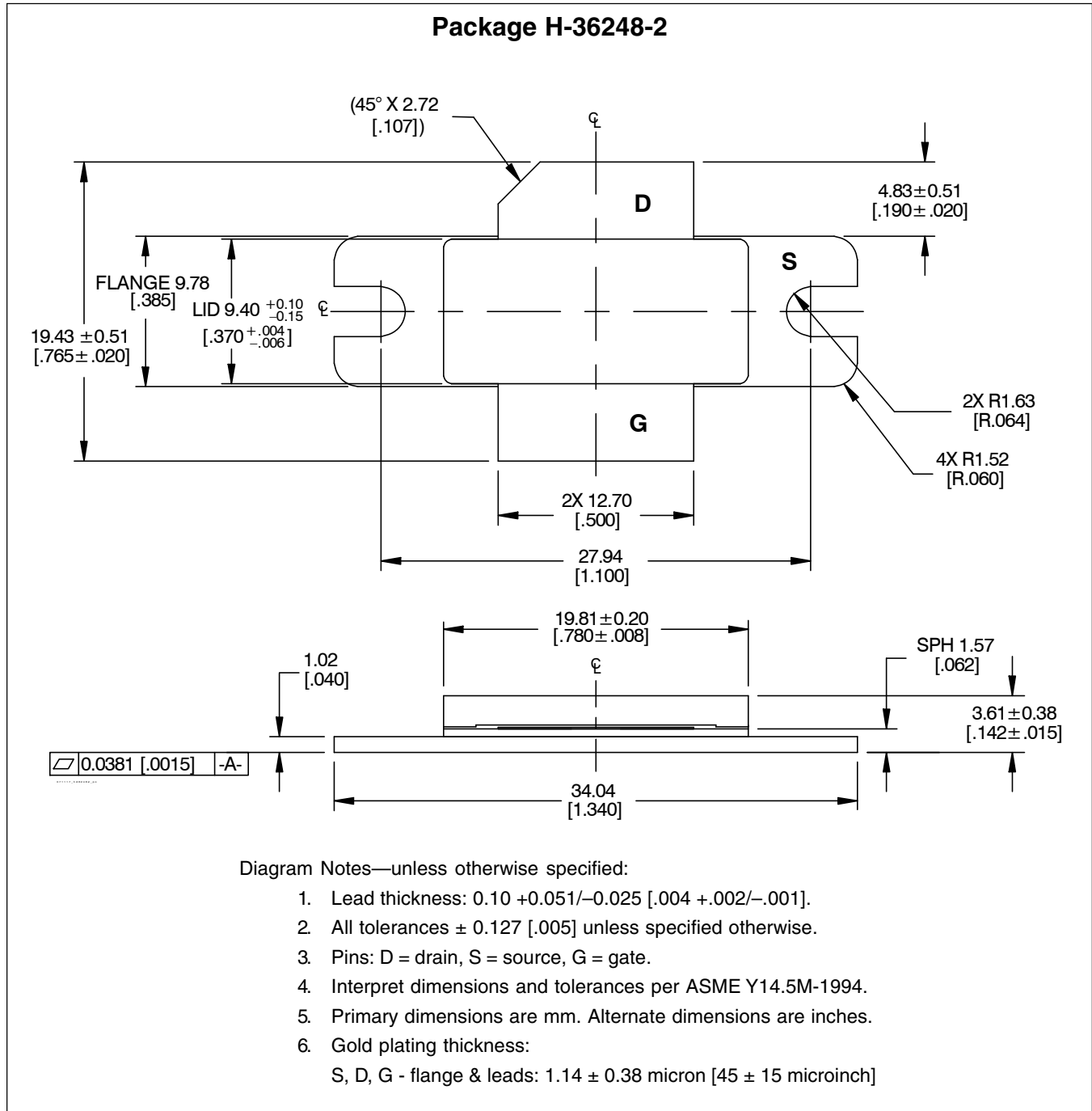


Reference circuit assembly diagram (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 μ F	Digi-Key	PCC1772CT-ND
C4	Tantalum capacitor, 10 μ F, 35 V	Digi-Key	399-1655-2-ND
C5, C7, C17, C22	Capacitor, 0.1 μ F	Digi-Key	PCC104BCT-ND
C6, C9, C10, C14, C19, C27	Ceramic capacitor, 33 pF	ATC	100B 330
C8	Capacitor, 0.01 μ F	ATC	200B 103
C11	Ceramic capacitor, 1.2 pF	ATC	100B 1R2
C12	Ceramic capacitor, 7.5 pF	ATC	100B 7R5
C13	Ceramic capacitor, 0.7 pF	ATC	100B 0R7
C15, C20	Capacitor, 1.0 μ F	ATC	920C105
C16, C18, C21, C23	Tantalum capacitor, 10 μ F, 50 V	Garrett Electronics	TPSE106K050R0400
C24, C25	Ceramic capacitor, 1.0 pF	ATC	100B 1R0
C26	Ceramic capacitor, 2.4 pF	ATC	100B 2R4
C28	Ceramic capacitor, 0.5 pF	ATC	100B 0R5
L1, L2	Ferrite, 8.9 mm	Elna Magnetics	BDS 4.6/3/8.9-4S2
Q1	Transistor	Infineon Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip Resistor 1.2 k-ohms	Digi-Key	P1.2KGCT-ND
R2	Chip Resistor 1.3 k-ohms	Digi-Key	P1.3KGCT-ND
R3	Chip Resistor 2 k-ohms	Digi-Key	P2KECT-ND
R4	Potentiometer 2 k-ohms	Digi-Key	3224W-202ETR-ND
R5, R7	Chip Resistor 5.1 k-ohms	Digi-Key	P5.1KECT-ND
R6, R8	Chip Resistor 10 ohms	Digi-Key	P10ECT-ND

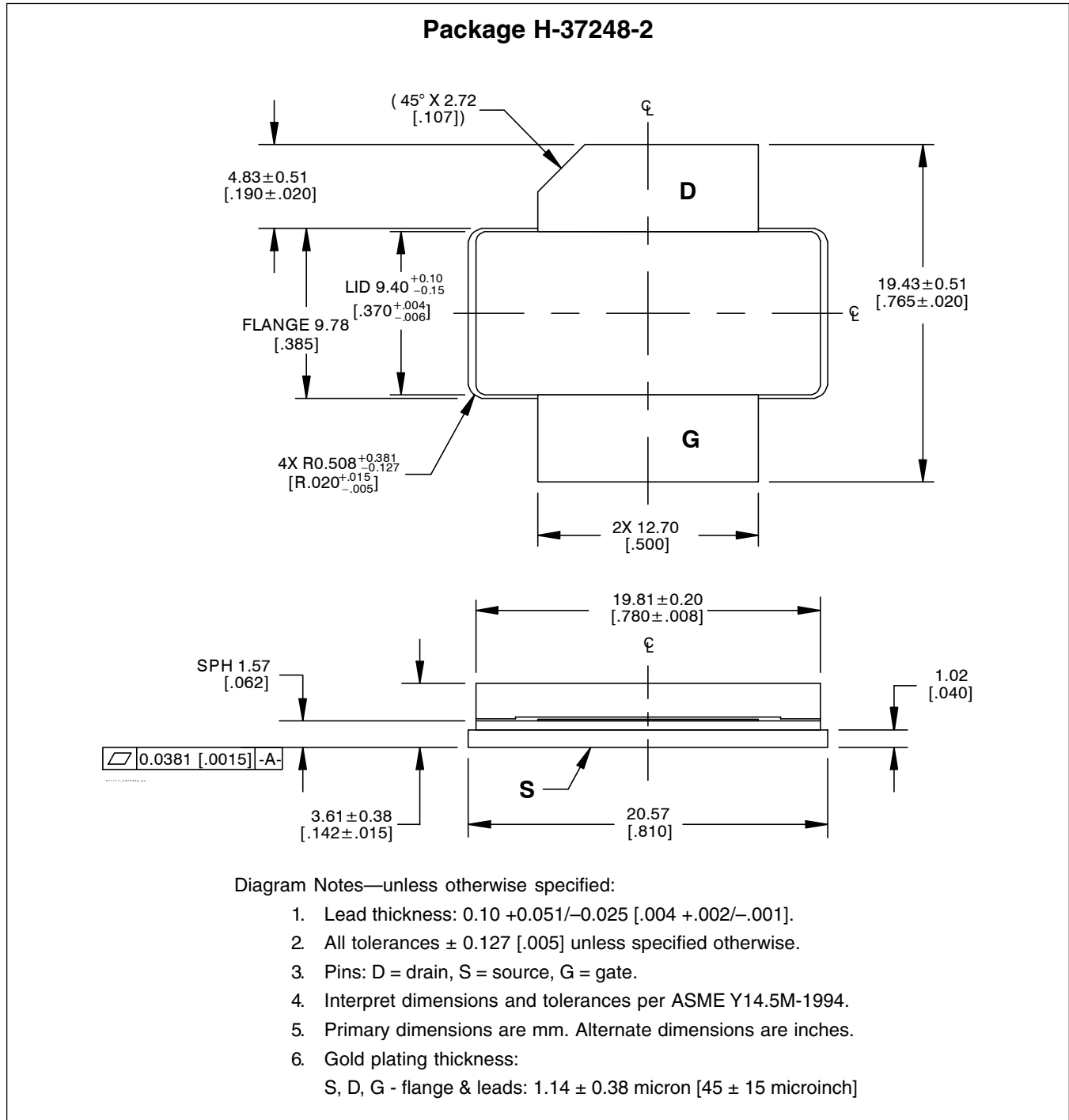
*Gerber Files for this circuit available on request

Package Outline Specifications



Find the latest and most complete information about products and packaging at the Infineon Internet page
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Package Outline Specifications (cont.)



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Revision History: 2007-11-19

Data Sheet

Previous Version: 2005-12-12, Data Sheet

Page	Subjects (major changes since last revision)
1, 10	Update company information.
1, 3, 9, 10	Update to product V4, with new package technologies. Update package outline diagrams.

We Listen to Your Comments

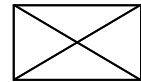
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