



PTFA181001E
PTFA181001F
 green
 Product

Thermally-Enhanced High Power RF LDMOS FETs 100 W, 1805 – 1880 MHz

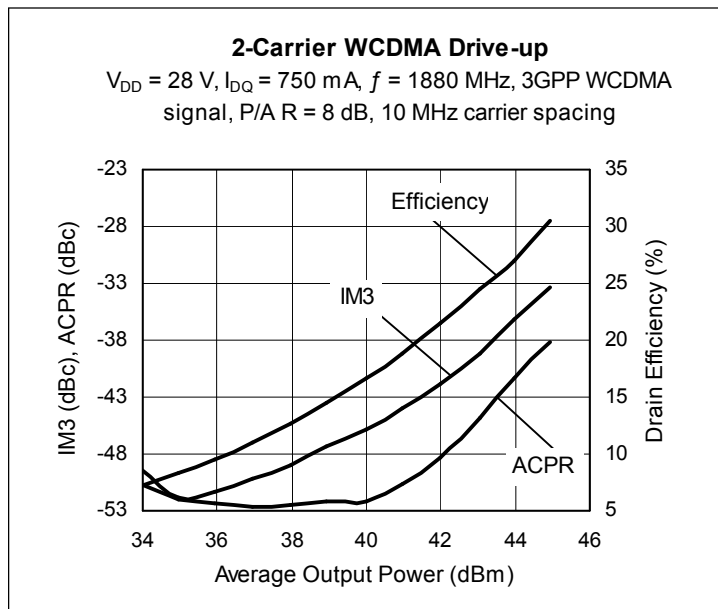
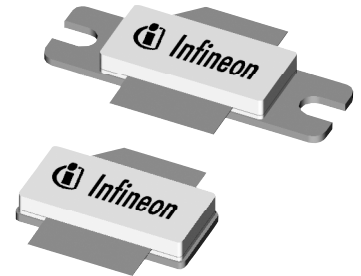
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Description

The PTFA181001E and PTFA181001F are 100-watt LDMOS FETs designed for EDGE and WCDMA power amplifier applications in the DCS band. Features include input and output matching, and thermally-enhanced packages with slotted or earless flanges. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA181001E
 Package H-36248-2

PTFA181001F
 Package H-37248-2



Features

- Thermally-enhanced packages
- Broadband internal matching
- Typical EDGE performance at 1879.8 MHz, 28 V
 - Average output power = 45 W
 - Linear Gain = 16.5 dB
 - Efficiency = 36%
 - EVM RMS = 1.8%
- Typical CW performance, 1880 MHz, 28 V
 - Output power at P-1dB = 120 W
 - Gain 15.5 dB
 - Efficiency = 52%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 28 V, 100 W (CW) output power
- Pb-free and RoHS compliant

RF Characteristics

EDGE Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ} = 750\text{ mA}$, $P_{OUT} = 45\text{ W}$, $f = 1879.8\text{ MHz}$

Characteristic	Symbol	Min	Typ	Max	Unit
Error Vector Magnitude	RMS EVM	—	1.8	—	%
Modulation Spectrum @ 400 KHz	ACPR	—	-61	—	dBc
Modulation Spectrum @ 600 KHz	ACPR	—	-73	—	dBc
Gain	G_{ps}	—	16.5	—	dB
Drain Efficiency	η_D	—	36	—	%

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (tested in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ} = 750\text{ mA}$, $P_{OUT} = 100\text{ W PEP}$, $f = 1850\text{ MHz}$, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	16	16.5	—	dB
Drain Efficiency	η_D	39	41	—	%
Intermodulation Distortion	IMD	—	-30	-28	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1.0	μA
	$V_{DS} = 63\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10.0	μA
On-State Resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.85	—	Ω
Operating Gate Voltage	$V_{DS} = 28\text{ V}$, $I_D = 750\text{ mA}$	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1.0	μA

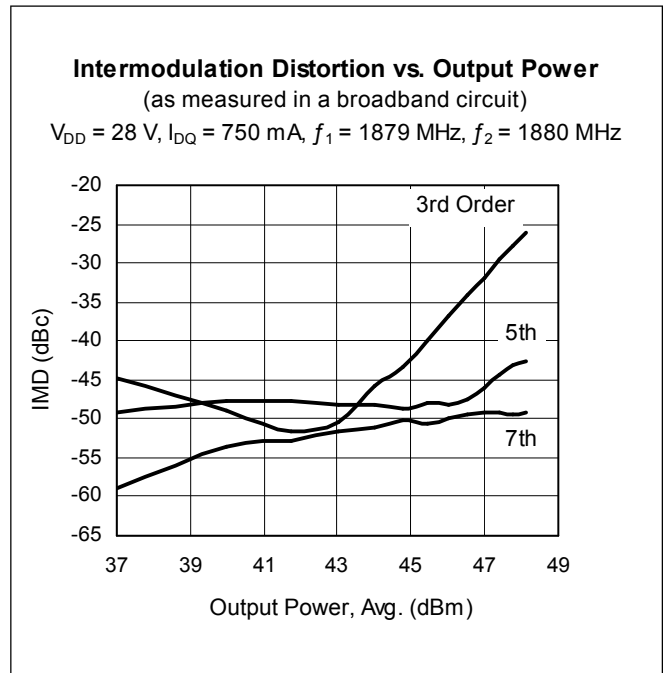
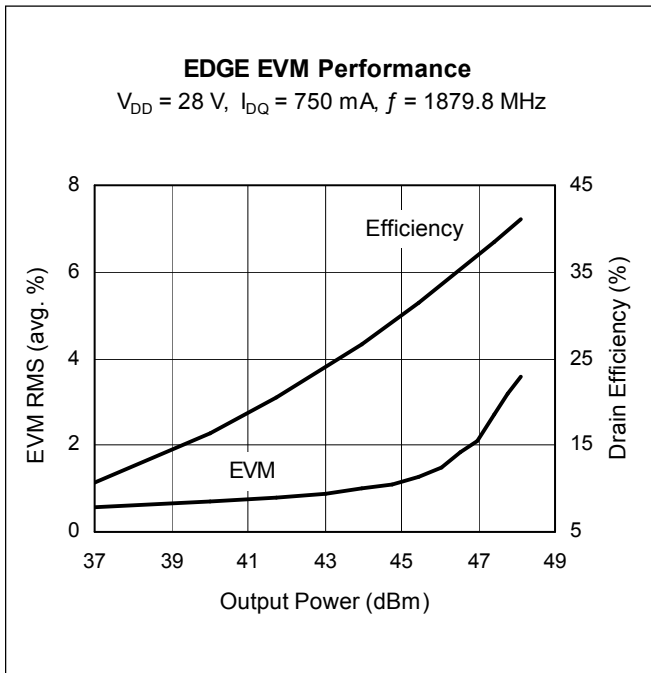
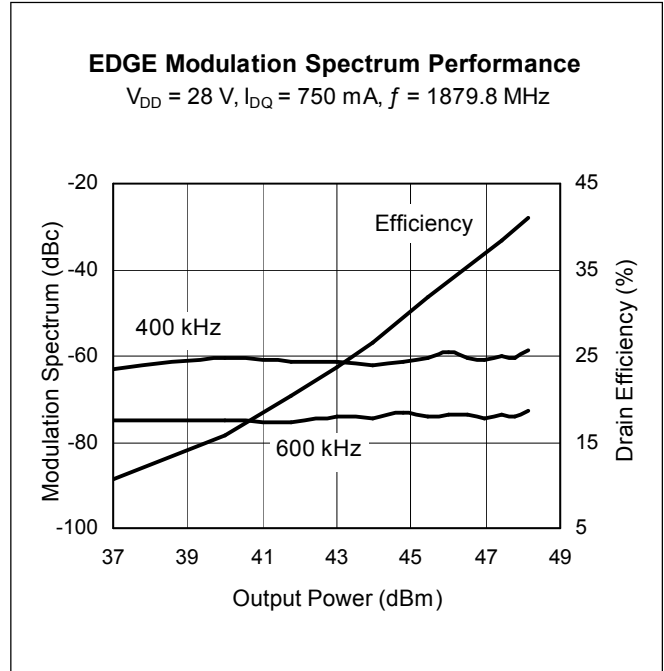
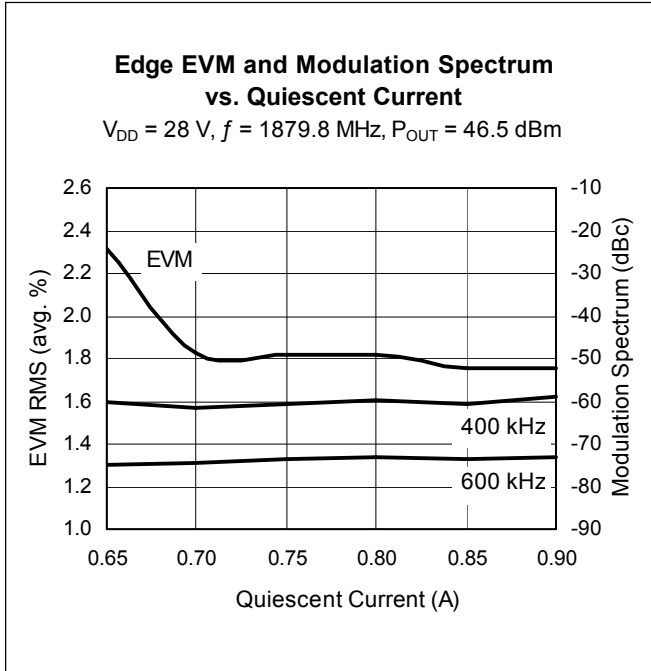
Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	-0.5 to +12	V
Junction Temperature	T_J	200	$^{\circ}\text{C}$
Total Device Dissipation Above 25 $^{\circ}\text{C}$ derate by	P_D	407	W
		2.33	W/ $^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-40 to +150	$^{\circ}\text{C}$
Thermal Resistance ($T_{CASE} = 70^{\circ}\text{C}$, 100 W CW)	$R_{\theta JC}$	0.43	$^{\circ}\text{C/W}$

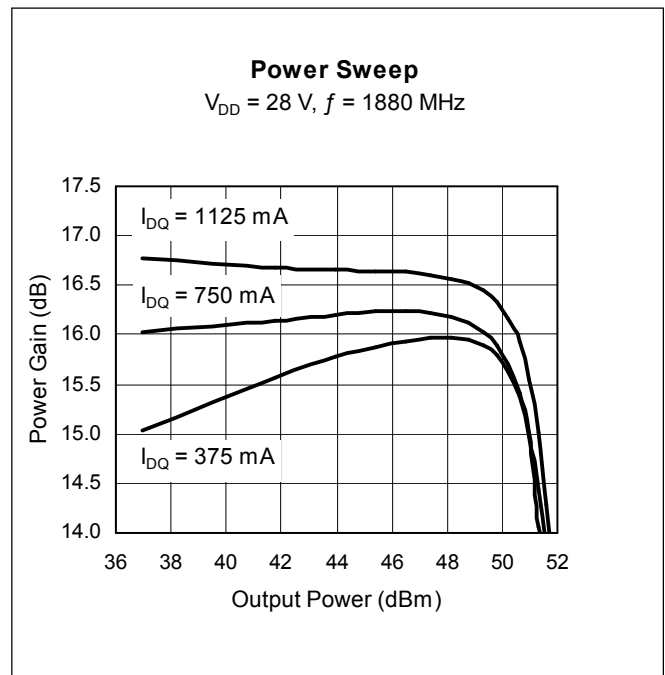
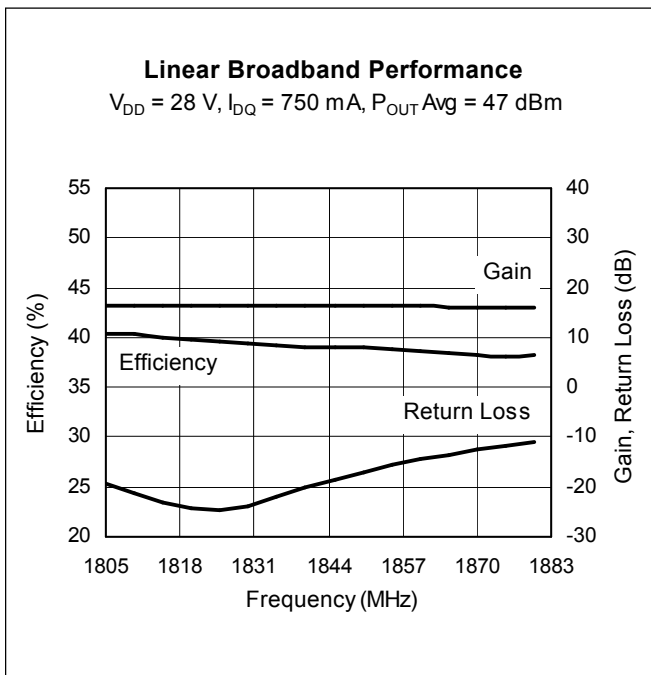
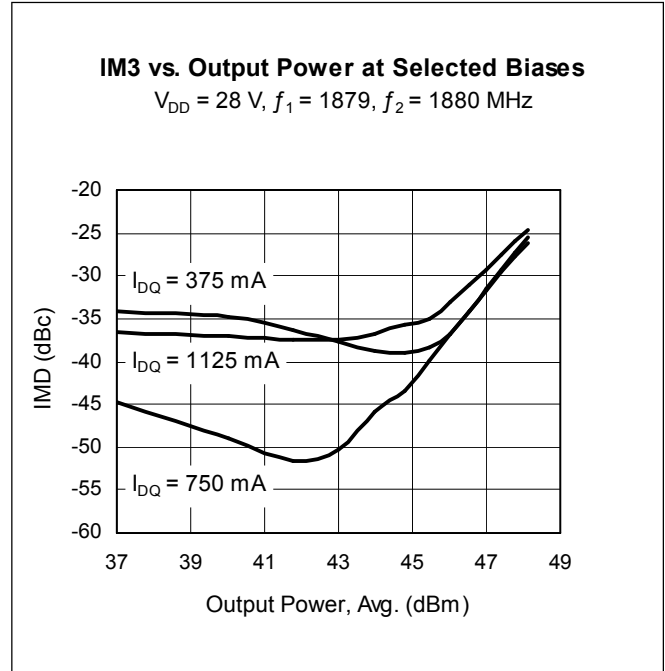
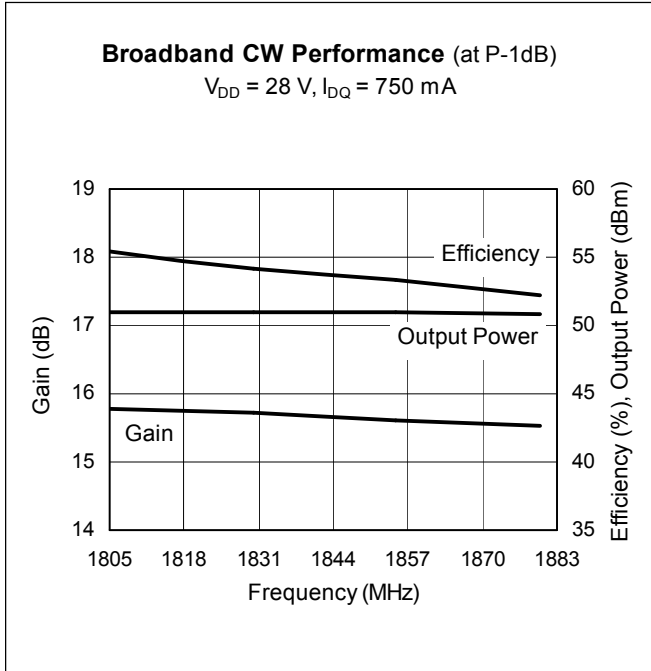
Ordering Information

Type and Version	Package Type	Package Description	Marking
PTFA181001E V4	H-36248-2	Thermally-enhanced slotted flange, single-ended	PTFA181001E
PTFA181001F V4	H-37248-2	Thermally-enhanced earless flange, single-ended	PTFA181001F

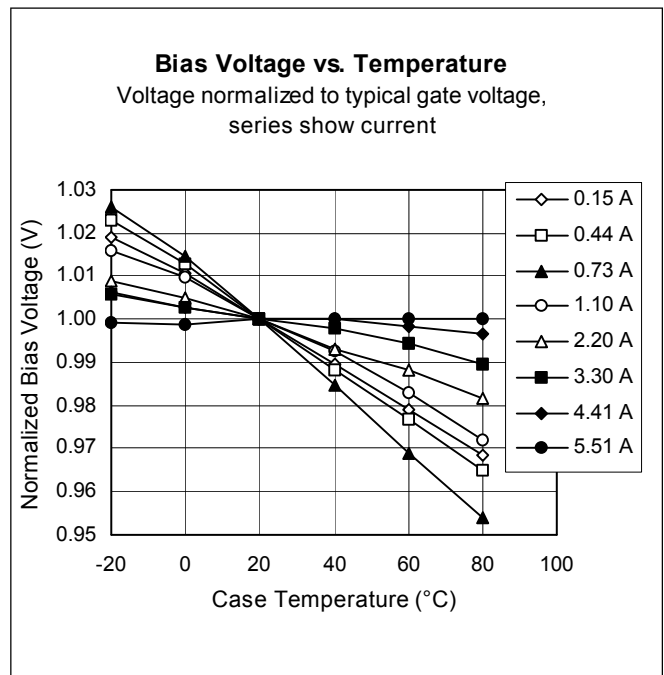
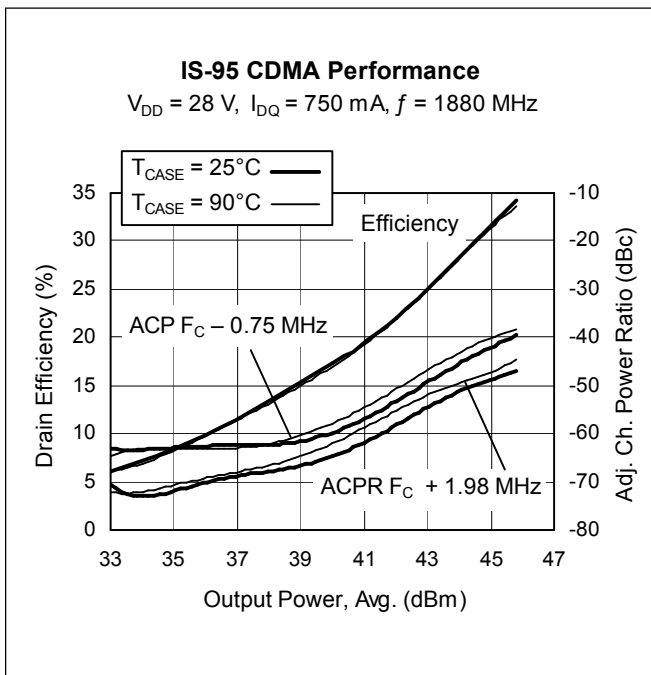
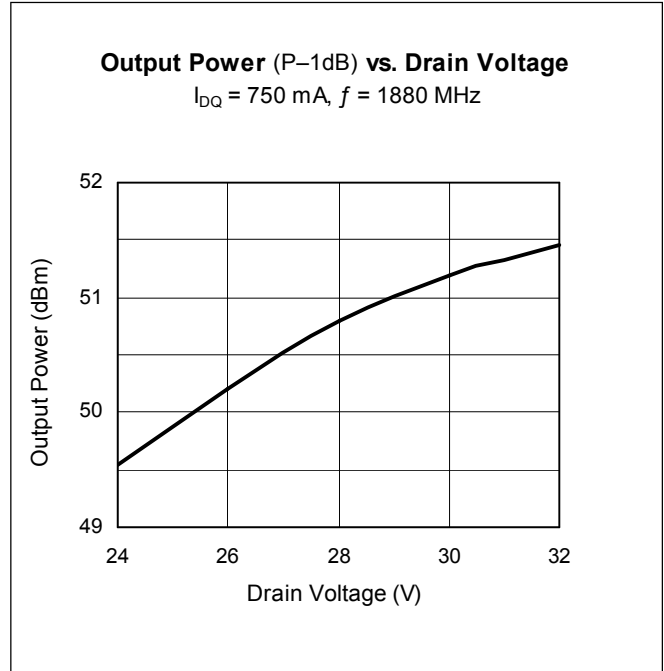
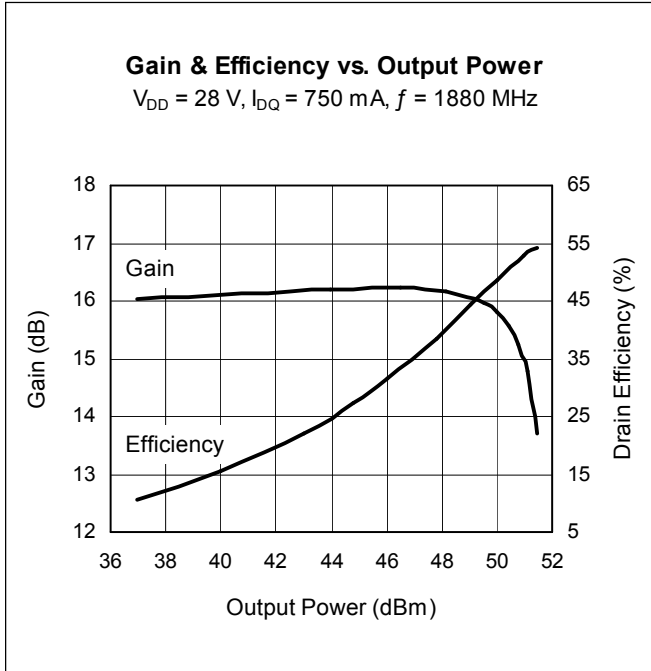
Typical Performance (data taken in a production test fixture)



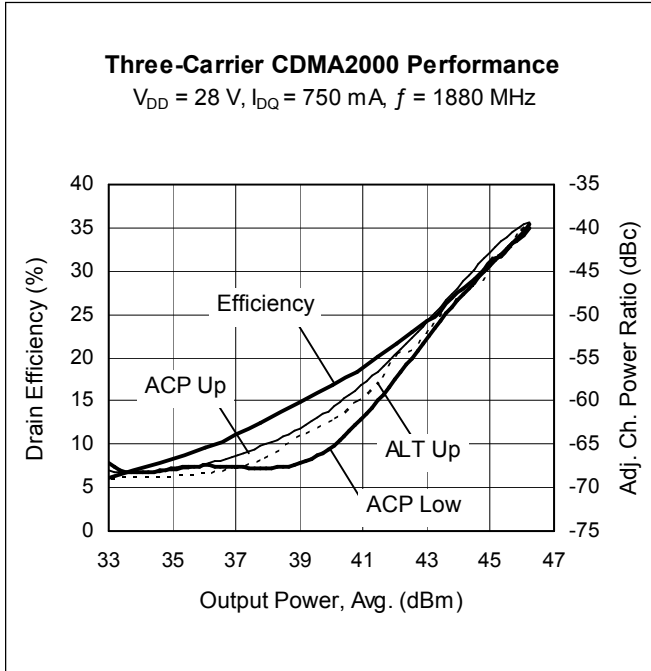
Typical Performance (cont.)



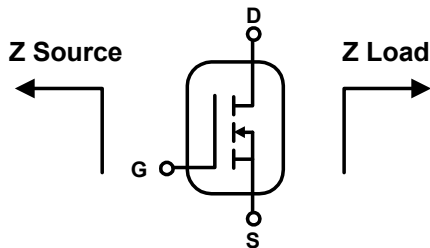
Typical Performance (cont.)



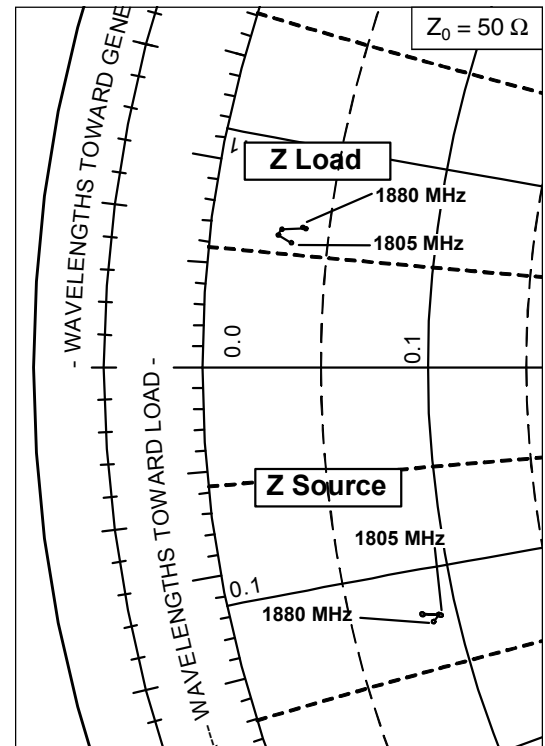
Typical Performance (cont.)



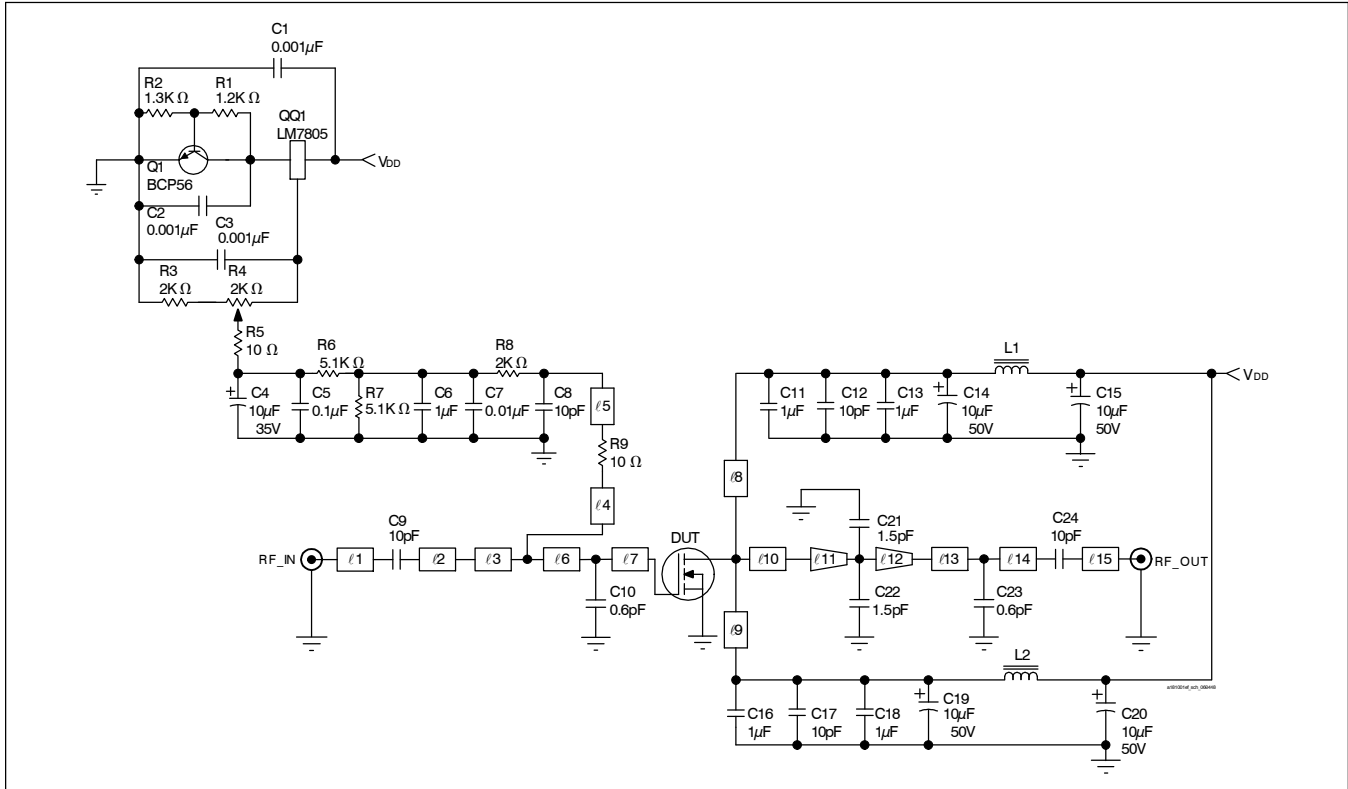
Broadband Circuit Impedance



Frequency MHz	Z Source W		Z Load W	
	R	jX	R	jX
1805	4.62	-6.23	1.71	2.79
1830	4.18	-6.10	1.41	2.92
1850	4.20	-6.13	1.47	3.05
1860	4.58	-6.20	1.99	3.13
1880	4.42	-6.36	1.91	3.16



Reference Circuit



Reference circuit schematic for $f = 1880 \text{ MHz}$

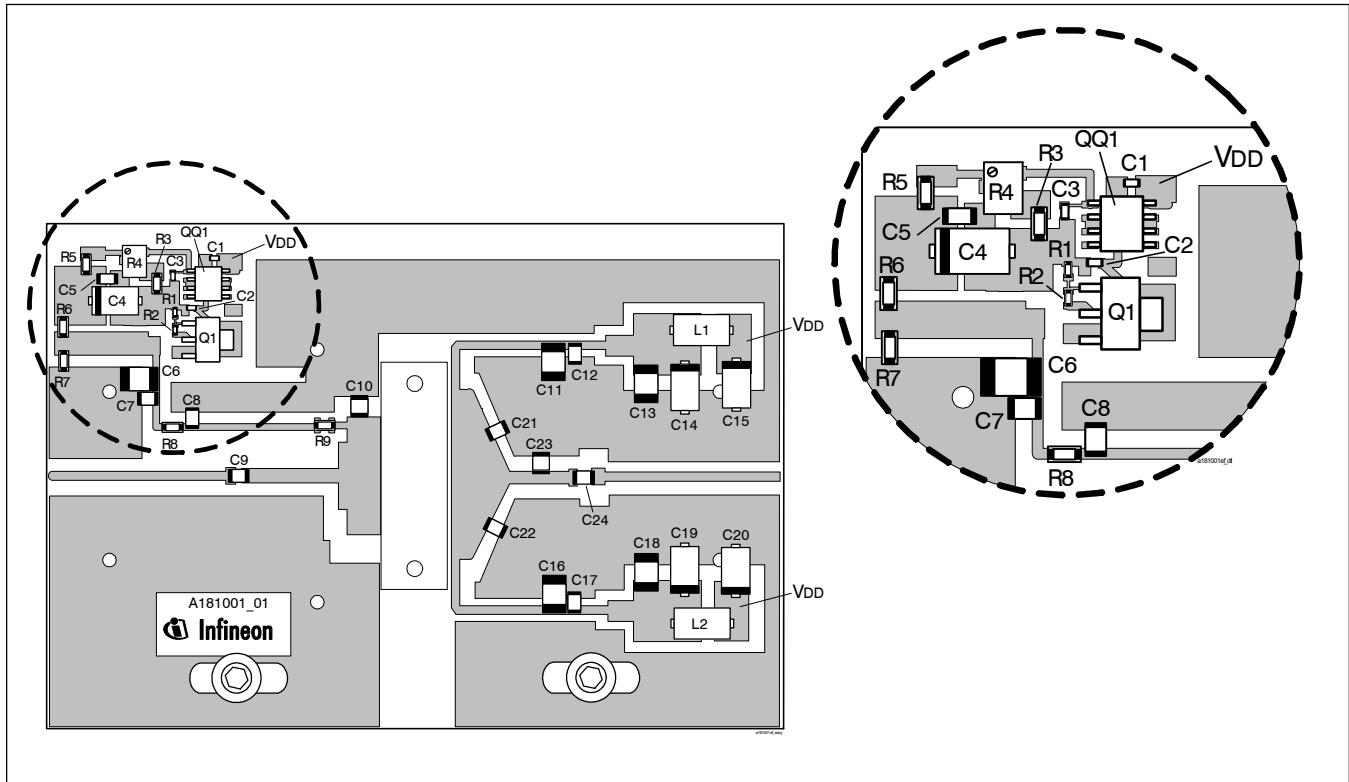
Circuit Assembly Information

DUT	PTFA181001E or PTFA181001F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, $\epsilon_r = 4.5$	Rogers TMM4	2 oz. copper

Microstrip	Electrical Characteristics at 1880 MHz ¹	Dimensions: L x W (mm)	Dimensions: L x W (in.)
l1	0.314 λ , 50.0 Ω	27.43 x 1.37	1.080 x 0.054
l2	0.172 λ , 38.0 Ω	14.73 x 2.16	0.580 x 0.085
l3	0.016 λ , 11.4 Ω	1.27 x 10.16	0.050 x 0.400
l4	0.024 λ , 60.0 Ω	2.24 x 0.99	0.088 x 0.039
l5	0.218 λ , 60.0 Ω	19.33 x 0.99	0.761 x 0.039
l6	0.019 λ , 6.9 Ω	1.52 x 17.78	0.060 x 0.700
l7	0.044 λ , 6.9 Ω	3.43 x 17.78	0.135 x 0.700
l8, l9	0.233 λ , 53.0 Ω	20.45 x 1.24	0.805 x 0.049
l10	0.039 λ , 4.9 Ω	3.10 x 25.65	0.122 x 1.010
l11 (taper)	0.037 λ , 4.9 Ω / 10.3 Ω	2.92 x 25.65 / 11.43	0.115 x 1.010 / 0.450
l12 (taper)	0.033 λ , 10.3 Ω / 41.0 Ω	2.79 x 11.43 / 1.91	0.110 x 0.450 / 0.075
l13	0.069 λ , 41.0 Ω	6.35 x 1.91	0.250 x 0.075
l14	0.038 λ , 41.0 Ω	3.25 x 1.91	0.128 x 0.075
l15	0.331 λ , 50.0 Ω	28.98 x 1.37	1.141 x 0.054

¹Electrical characteristics are rounded.

Reference Circuit (cont.)

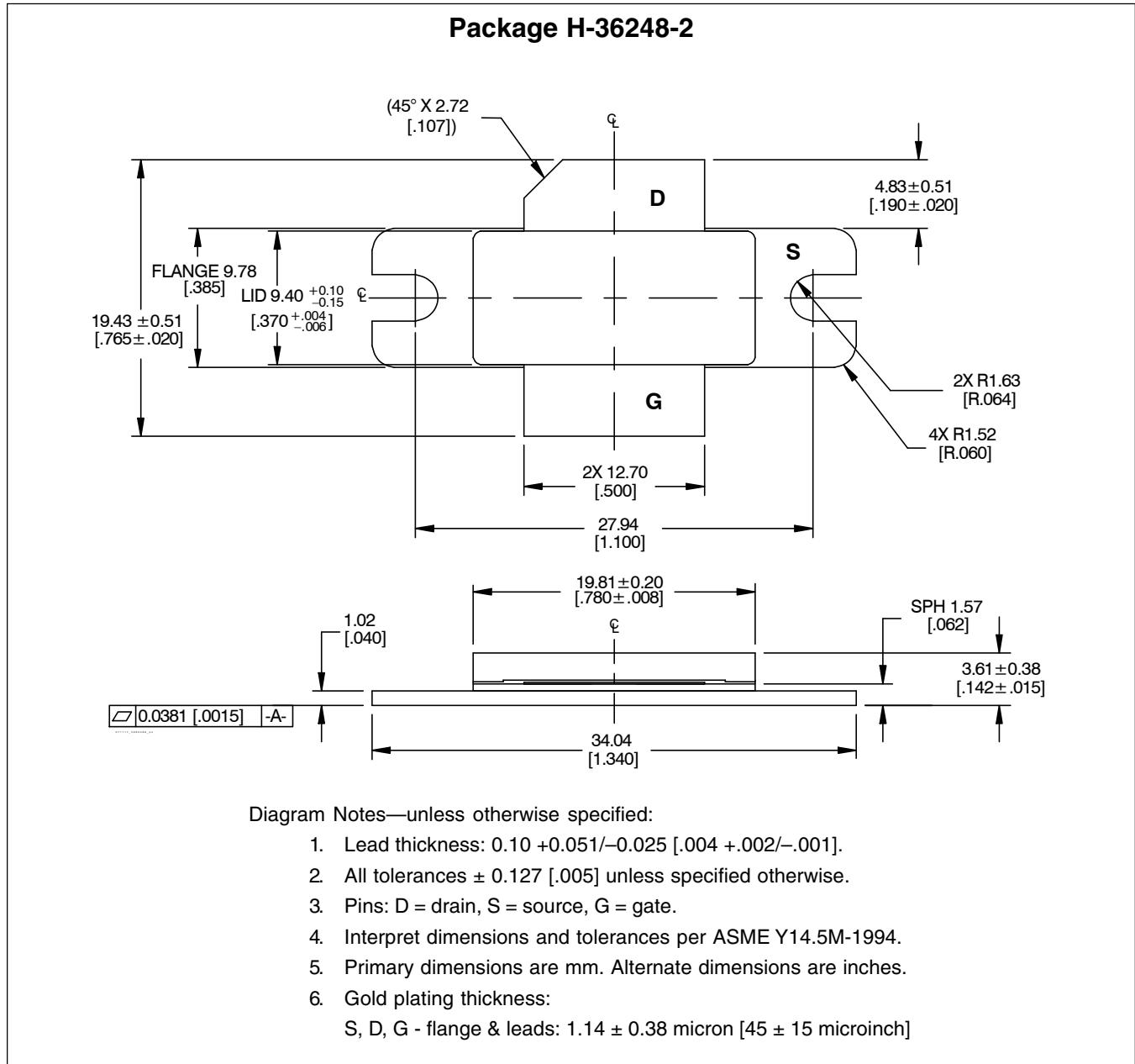


Reference circuit assembly diagram (not to scale)

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 μ F	Digi-Key	PCC1772CT-ND
C4	Tantalum capacitor, 10 μ F, 35 V	Digi-Key	399-1655-2-ND
C5	Capacitor, 0.1 μ F	Digi-Key	PCC104BCT-ND
C6, C11, C13, C16, C18	Capacitor, 1.0 μ F	ATC	920C105
C7	Capacitor, 0.01 μ F	ATC	200B 103
C8, C9, C12, C17, C24	Ceramic capacitor, 10 pF	ATC	100B 100
C10, C23	Ceramic capacitor, 0.6 pF	ATC	100B 0R6
C14, C15, C19, C20	Tantalum capacitor, 10 μ F, 50 V	Garrett Electronics	TPSE106K050R0400
C21, C22	Ceramic capacitor, 1.5 pF	ATC	100B 1R5
L1, L2	Ferrite, 8.9 mm	Elna Magnetics	BDS 4.6/3/8.9-4S2
Q1	Transistor	Infineon Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip Resistor 1.2 k-ohms	Digi-Key	P1.2KGCT-ND
R2	Chip Resistor 1.3 k-ohms	Digi-Key	P1.3KGCT-ND
R3, R8	Chip Resistor 2 k-ohms	Digi-Key	P2KECT-ND
R4	Potentiometer 2 k-ohms	Digi-Key	3224W-202ETR-ND
R5, R9	Chip Resistor 10 ohms	Digi-Key	P10ECT-ND
R6, R7	Chip Resistor 5.1 k-ohms	Digi-Key	P5.1KECT-ND

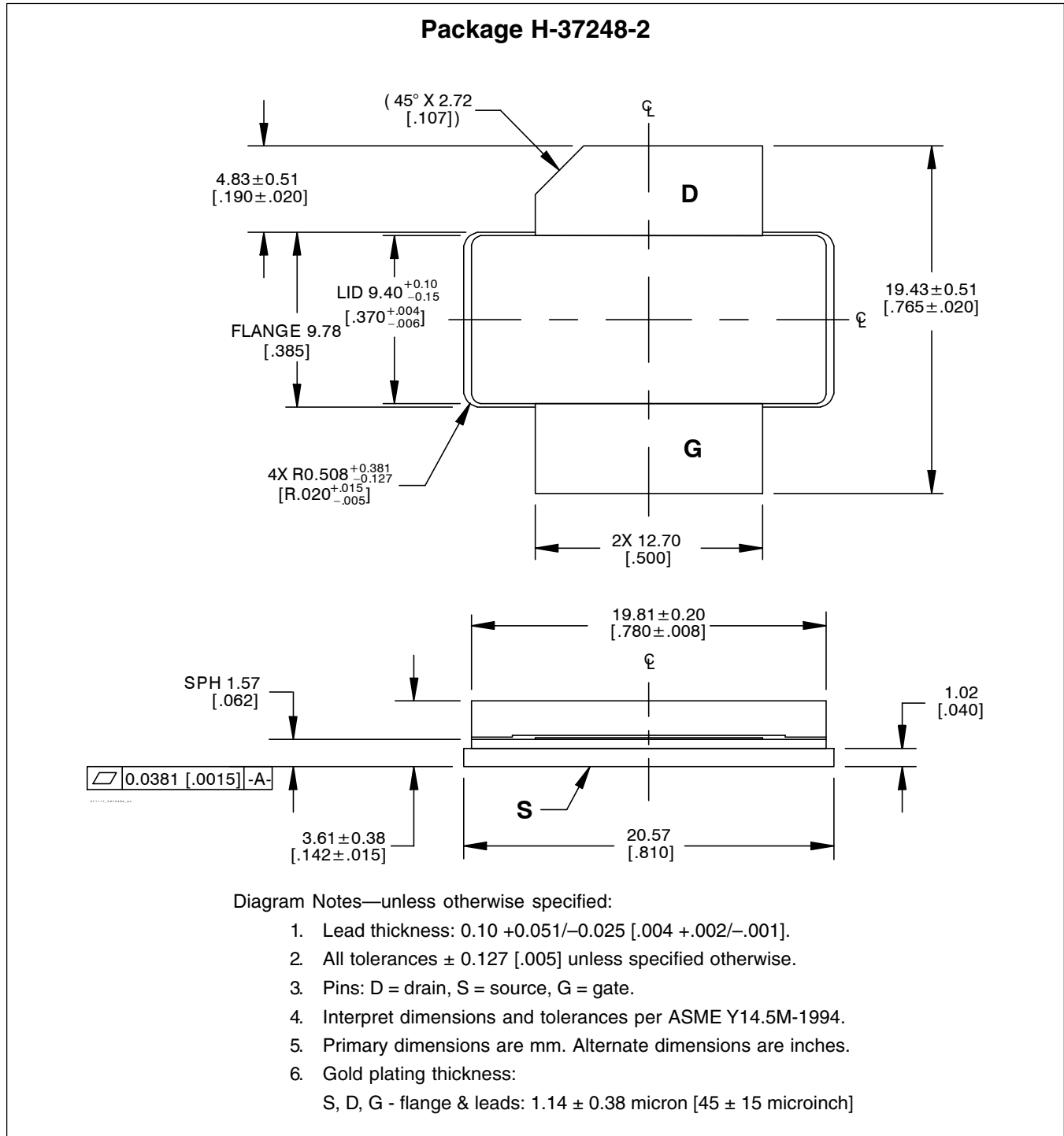
Gerber files for this circuit available on request

Package Outline Specifications



Find the latest and most complete information about products and packaging at the Infineon Internet page
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Package Outline Specifications (cont.)



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Revision History: 2009-02-20

Data Sheet

Previous Version: 2006-04-14, Data Sheet

Page	Subjects (major changes since last revision)
1, 2, 9, 10	Update to product V4, with new package technologies. Update package outline diagrams.
8	Fixed typing error

We Listen to Your Comments

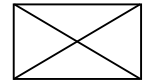
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