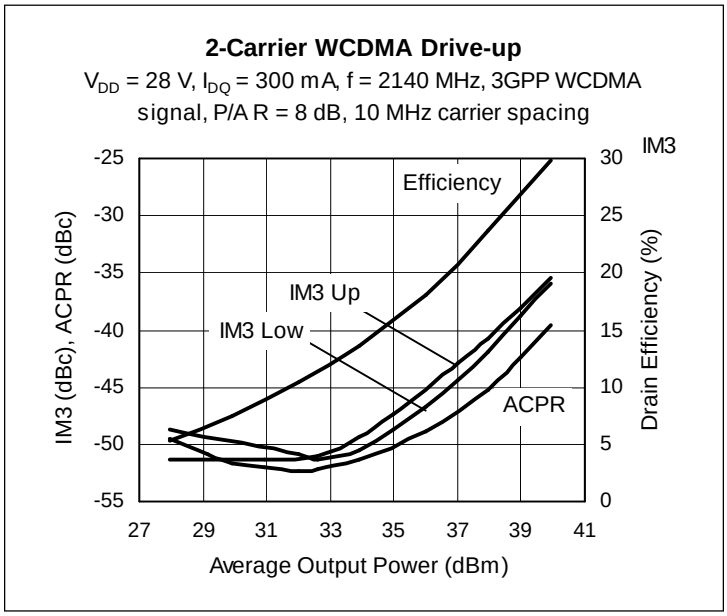
Thermally-Enhanced High Power RF LDMOS FET
30 W, 2110 – 2170 MHz

Description

The PTFA210301E is a thermally-enhanced, 30-watt, internally matched *GOLDMOS* FET intended for WCDMA applications. It is optimized for single- and two-carrier WCDMA operation from 2110 to 2170 MHz. Thermally-enhanced packaging provides the coolest operation available. Full gold metallization ensures excellent device lifetime and reliability.

PTFA210301E
Package H-30265-2



Features

- Thermally-enhanced packaging, Pb-free and RoHS-compliant
- Broadband internal matching
- Typical two-carrier WCDMA performance at 2140 MHz, 28 V
  - Average output power = 33 dBm
  - Linear Gain = 16.5 dB
  - Intermodulation distortion = –50 dBc
  - Adjacent channel power = –52 dBc
- Typical CW performance, 2170 MHz, 28 V
  - Output power at P–1dB = 40 W
  - Efficiency = 59%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 28 V, 30 W (CW) output power

RF Characteristics

2-Carrier WCDMA Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 300 mA, P_{OUT} = 8 W average

f_1 = 2135 MHz, f_2 = 2145 MHz, 3GPP signal, channel bandwidth = 3.84 MHz , peak/average = 8 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	17	—	dB
Drain Efficiency	η_D	—	27	—	%
Intermodulation Distortion	IMD	—	–38	—	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-Tone Measurements (tested in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 300 mA, P_{OUT} = 30 W PEP, f = 2170 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	16	17	—	dB
Drain Efficiency	η_D	34	36	—	%
Intermodulation Distortion	IMD	—	–32	–30	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 µA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.23	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ} = 300 mA	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	145	W
Above 25°C derate by		0.83	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 30 W CW)	$R_{\theta JC}$	1.2	°C/W

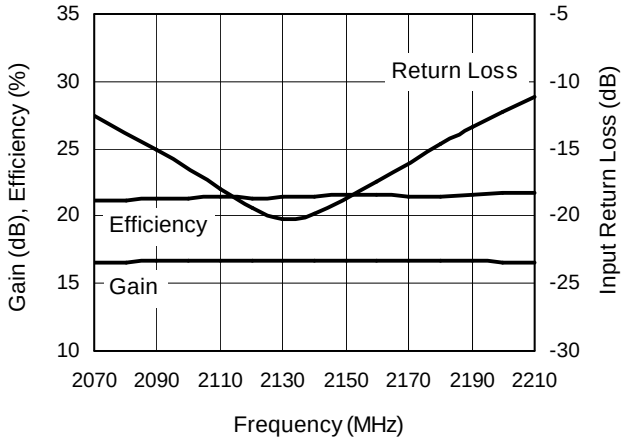
Ordering Information

Type and Version	Package Outline	Package Description	Marking
PTFA210301E V1	H-30265-2	Thermally-enhanced slotted flange, single-ended	PTFA210301E

Typical Performance (data taken in a production test fixture)

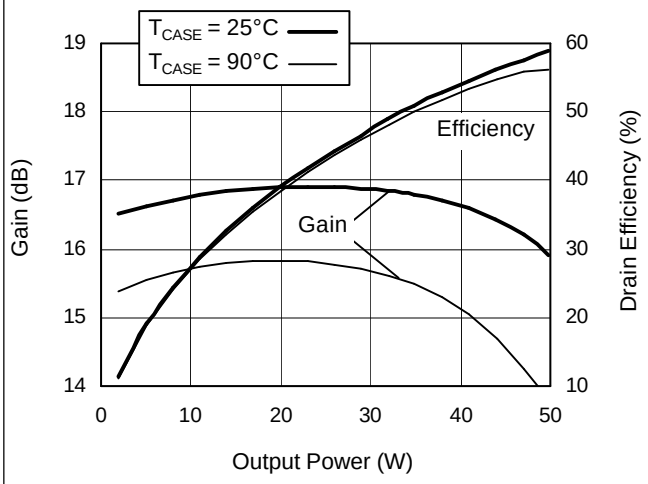
Broadband Performance

V_{DD} = 28 V, I_{DQ} = 300 mA, P_{OUT} = 38.0 dBm



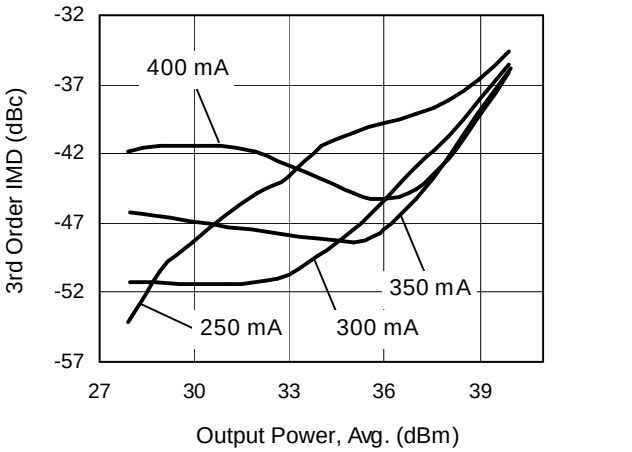
Power Sweep, CW Conditions

V_{DD} = 28 V, I_{DQ} = 300 mA, f = 2170 MHz



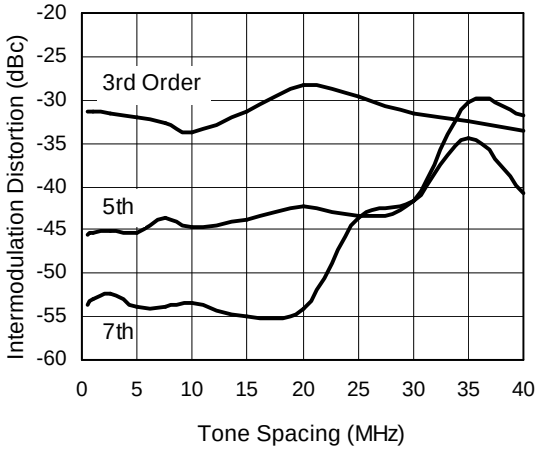
Two-carrier WCDMA at Various Biases

V_{DD} = 28 V, f = 2140 MHz, 3GPP WCDMA signal,
P/AR = 8 dB, 10 MHz carrier spacing, series show I_{DQ}



Intermodulation Distortion Products vs. Tone Spacing

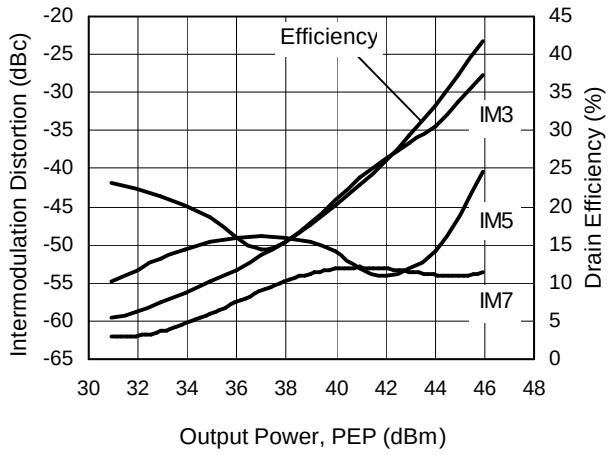
V_{DD} = 28V I_{DQ} = 300 mA, f = 2140 MHz,
P_{OUT} = 45 dBm PEP



Typical Performance (cont.)

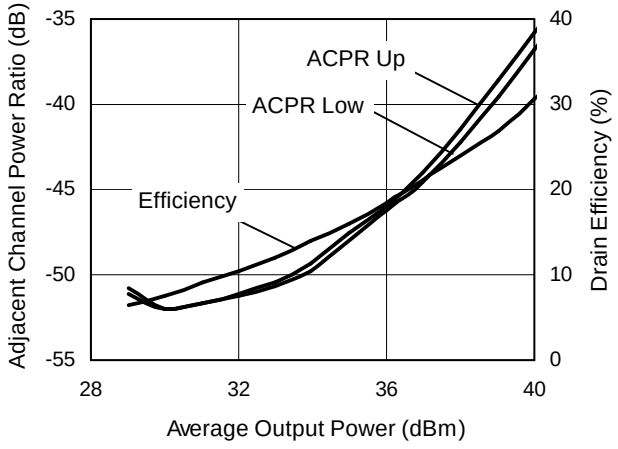
2-Tone Drive-up

V_{DD} = 28 V, I_{DQ} = 300 mA,
f = 2140 MHz, tone spacing = 1 MHz



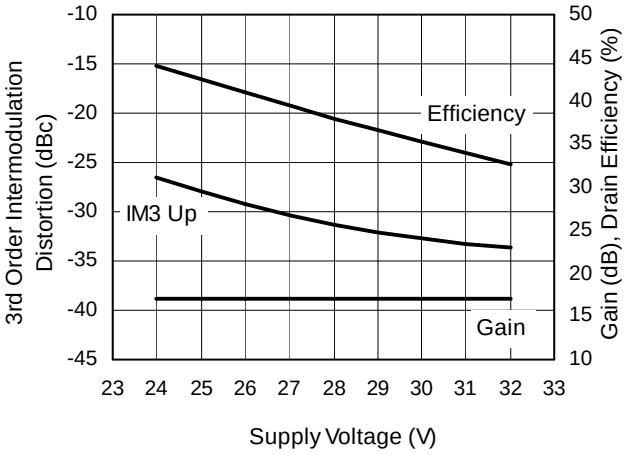
Single-carrier WCDMA Drive-up

V_{DD} = 28 V, I_{DQ} = 300 mA, f = 2140 MHz,
3GPP WCDMA signal, TM1 w/16 DPCH, 67% clipping,
P/A R = 8.5 dB, 3.84 MHz BW



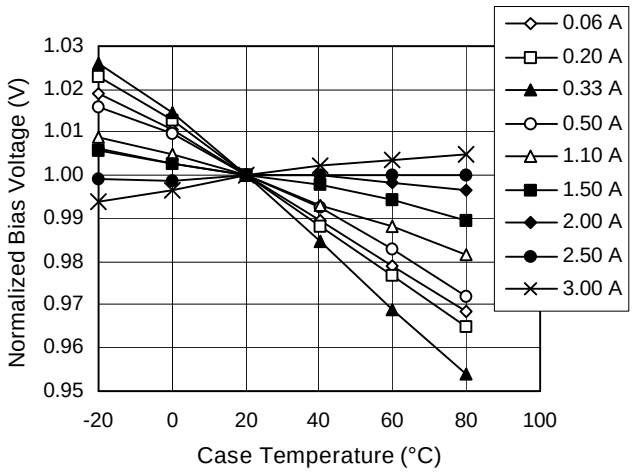
IM3, Drain Efficiency and Gain vs. Supply Voltage

I_{DQ} = 300 mA, f = 2140 MHz,
P_{OUT} (PEP) = 45 dBm, tone spacing = 1 MHz

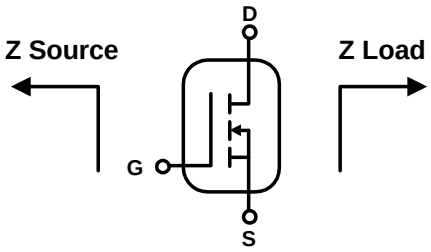


Bias Voltage vs. Temperature

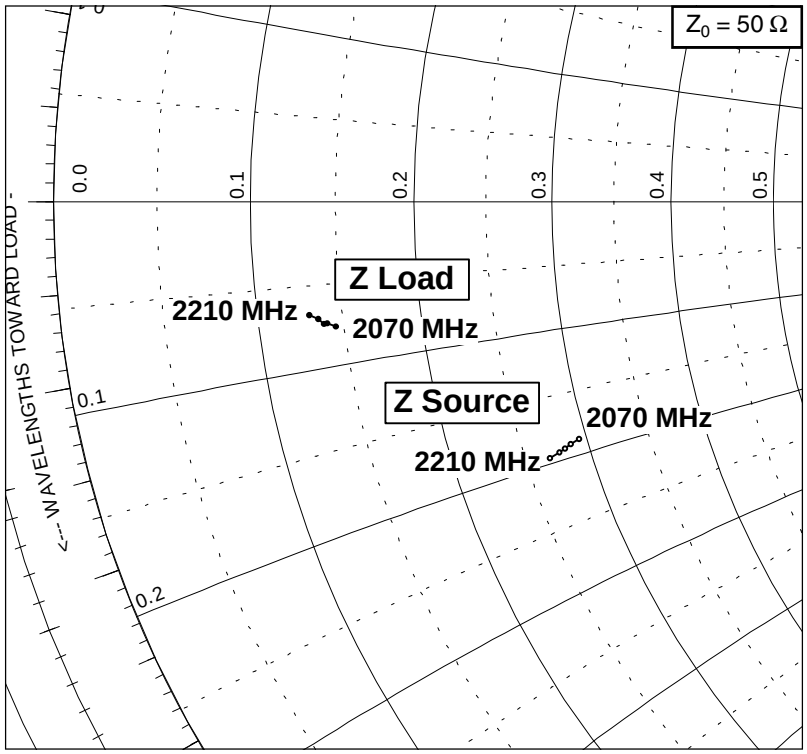
Voltage normalized to typical gate voltage,
series show current



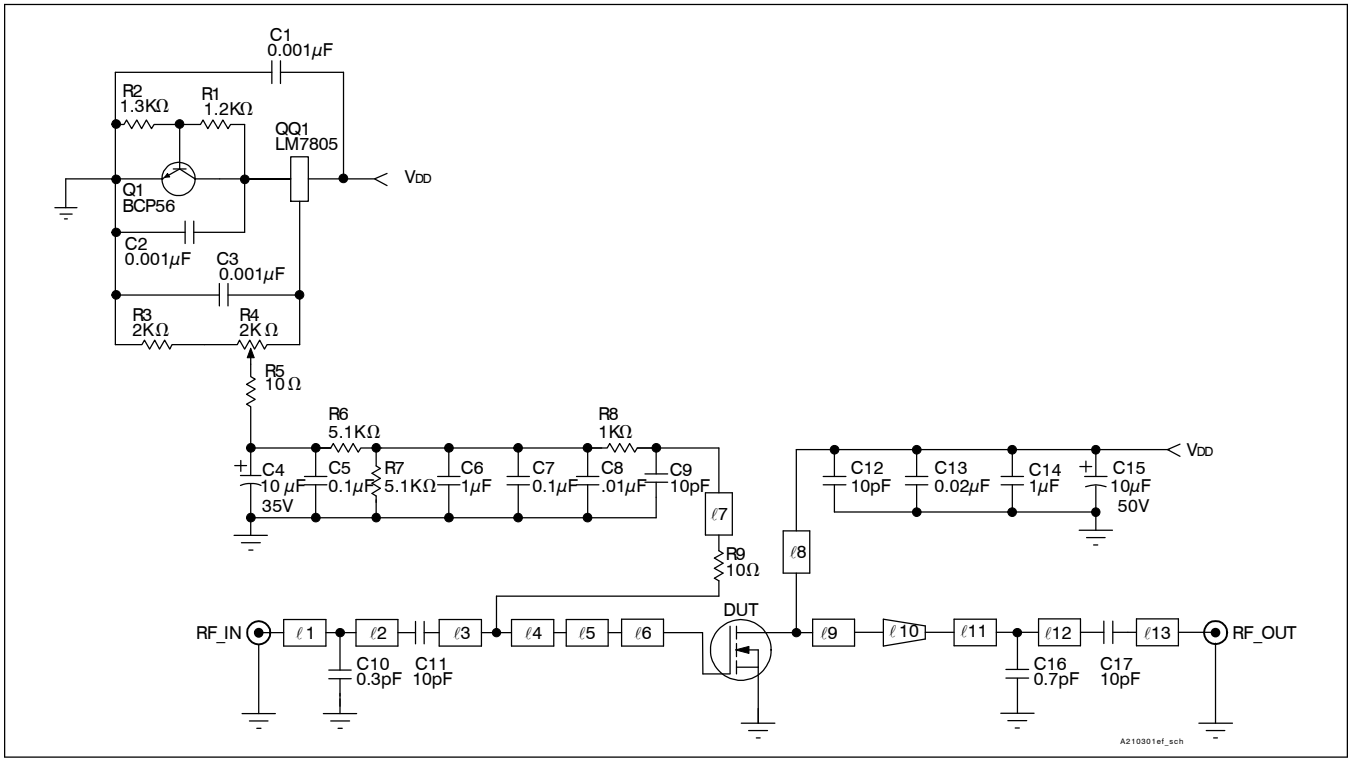
Broadband Circuit Impedance



Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
2070	14.70	-9.41	7.26	-3.82
2110	14.33	-9.52	7.01	-3.70
2140	14.07	-9.61	6.91	-3.69
2170	13.81	-9.69	6.77	-3.53
2210	13.40	-9.79	6.52	-3.39



Reference Circuit



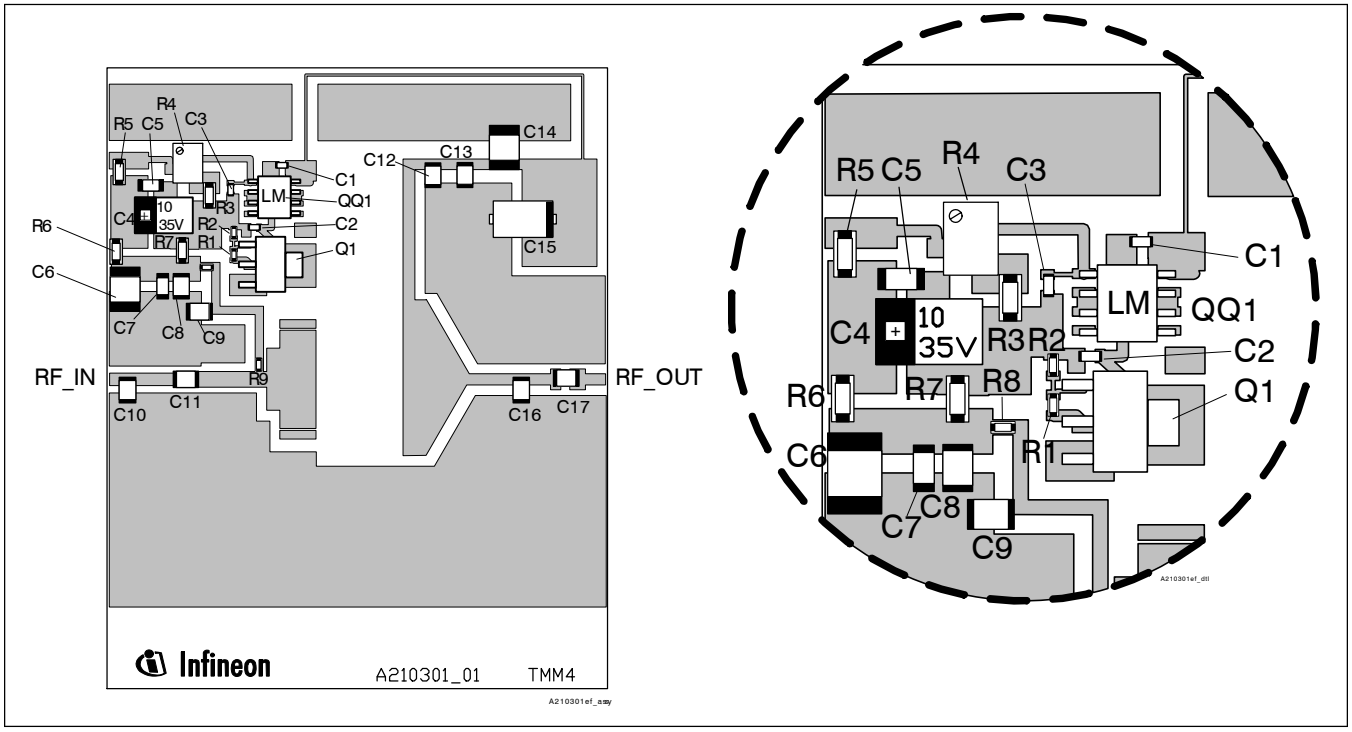
Reference Circit Schematic for f = 2140 MHz

Circuit Assembly Information			
DUT	PTFA210301E	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, ε_r = 4.5	Rogers TMM4	2 oz. copper

Microstrip	Electrical Characteristics at 2140 MHz[1]	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.013 λ, 50.0 Ω	1.02 x 1.42	0.040 x 0.056
ℓ2	0.081 λ, 50.0 Ω	6.17 x 1.42	0.243 x 0.056
ℓ3	0.108 λ, 42.0 Ω	8.23 x 1.85	0.324 x 0.073
ℓ4	0.172 λ, 61.0 Ω	13.39 x 0.94	0.527 x 0.037
ℓ5	0.013 λ, 42.0 Ω	0.94 x 1.85	0.037 x 0.073
ℓ6	0.023 λ, 15.0 Ω	1.63 x 7.57	0.064 x 0.298
ℓ7	0.063 λ, 9.9 Ω	4.29 x 12.07	0.169 x 0.475
ℓ8	0.171 λ, 53.0 Ω	13.13 x 1.22	0.517 x 0.048
ℓ9	0.039 λ, 6.5 Ω	2.64 x 19.10	0.104 x 0.752
ℓ10 (taper)	0.185 λ, 6.5 Ω / 50.0 Ω	4.70 x 19.10 / 1.37	0.185 x 0.752 / 0.054
ℓ11	0.025 λ, 50.0 Ω	1.88 x 1.42	0.074 x 0.056
ℓ12	0.128 λ, 50.0 Ω	9.78 x 1.42	0.385 x 0.056
ℓ13	0.057 λ, 50.0 Ω	4.32 x 1.42	0.170 x 0.056

[1]Electrical characteristics are rounded.

Reference Circuit (cont.)



Reference Circuit (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4	Tantalum capacitor, 10 µF, 35 V	Digi-Key	PCS6106TR-ND
C5, C7	Capacitor, 0.1 µF	Digi-Key	P4525-ND
C6, C14	Capacitor, 1 µF	Digi-Key	PCC104BCT-ND
C8	Capacitor, 0.01 µF	ATC	100B 103
C9, C11, C12, C17	Capacitor, 10 pF	ATC	100B 100
C10	Capacitor, 0.3 pF	ATC	100B 0R3
C13	Capacitor, 0.02 µF	ATC	100B 203
C15	Tantalum capacitor, 10 µF, 50 V	Garrett Electronics	TPS106K050R0400
C16	Capacitor, 0.7 pF	ATC	100B 0R7
Q1	Transistor	Infineon	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor, 1.2 k-ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor, 1.3 k-ohms	Digi-Key	P1.3KGCT-ND
R3	Chip resistor, 2 k-ohms	Digi-Key	P2KECT-ND
R4	Potentiometer, 2 k-ohms	Digi-Key	3224W-202ETR-ND
R5	Chip resistor, 10 ohms	Digi-Key	P10ECT-ND
R6, R7	Chip resistor, 5.1 k-ohms	Digi-Key	P5.1KECT-ND
R8	Chip resistor, 1 k-ohms	Digi-Key	P1.0KGCT-ND
R9	Chip resistor, 10 k-ohms	Digi-Key	P10GCT-ND

**Gerber Files for this circuit available on request*

Package Outline Specifications

Package H-30265-2

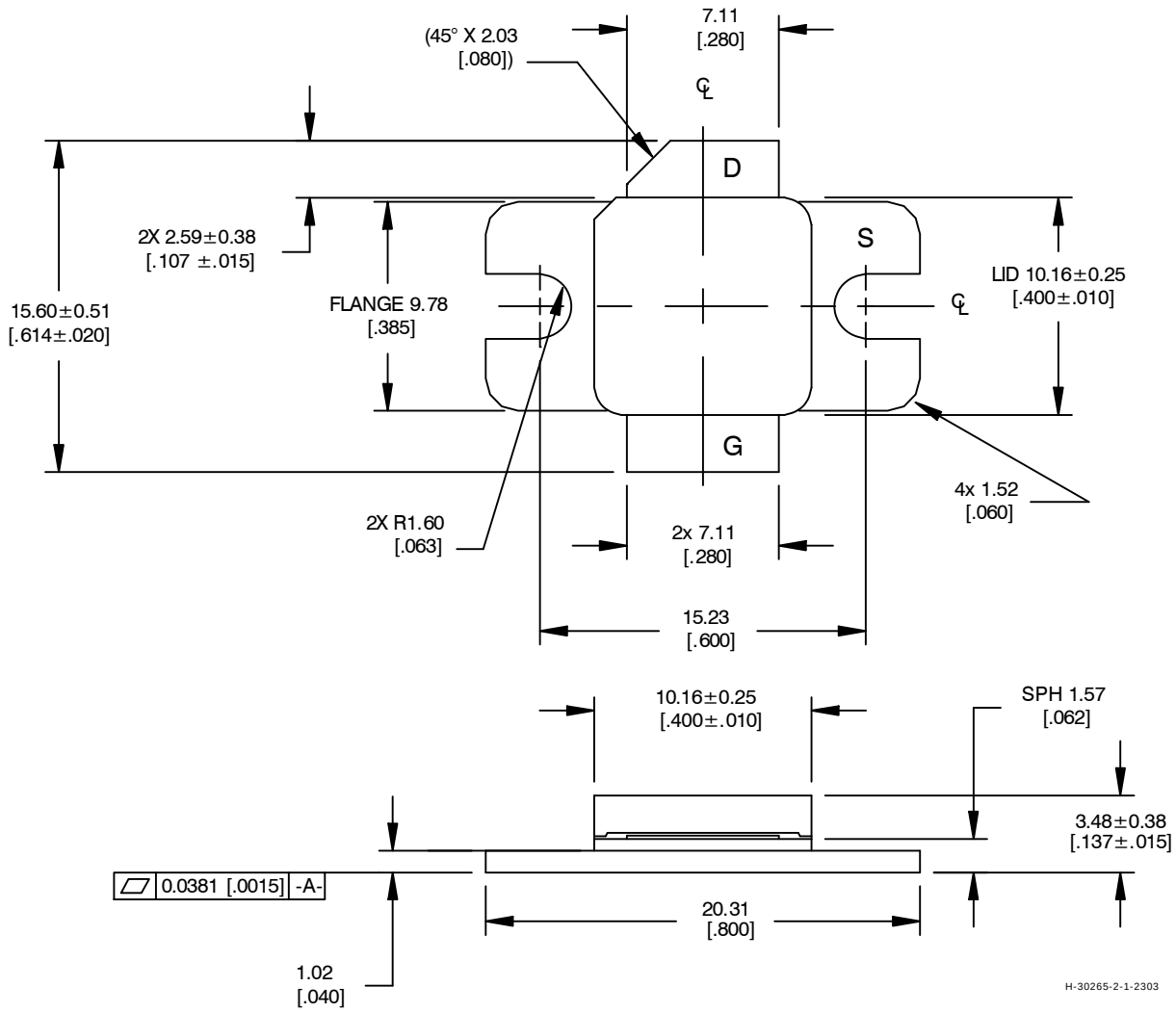


Diagram Notes:

1. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
2. All tolerances ± 0.127 [.005] unless specified otherwise.
3. Pins: D = drain, S = source, G = gate.
4. Interpret dimensions and tolerances per ASME Y14.5M-1994.
5. Primary dimensions are mm. Alternate dimensions are inches.
6. Gold plating thickness:
   S - flange: 2.54 micron [100 microinch] (min)
   D, G - leads: 1.14 ± 0.38 micron [45 ± 15 microinch]

Find the latest and most complete information about products and packaging at the Infineon Internet page ***http://www.infineon.com/rfpower***

Revision History:	2008-03-04	Data Sheet
Previous Version:	2005-06-22, Data Sheet, Rev. 02	

Page	Subjects (major changes since last revision)
All	Remove references to alternate products.

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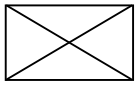

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