Thermally-Enhanced High Power RF LDMOS FET 100 W, 2110 – 2170 MHz

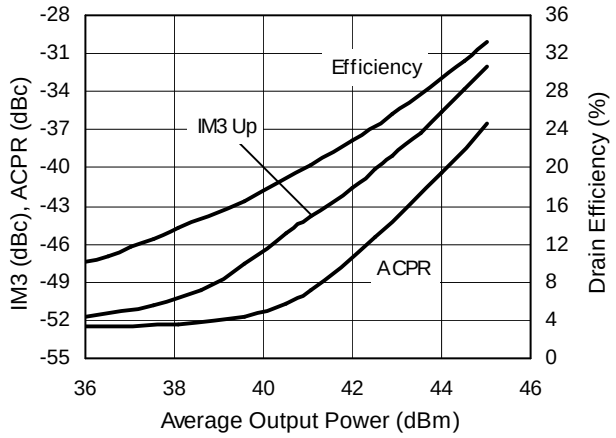
Description

The PTFA211001E is a thermally-enhanced, 100-watt, internally-matched *GOLDMOS*® FET intended for WCDMA applications. It is characaterized for single- and two-carrier WCDMA operation from 2110 to 2170 MHz. Thermally-enhanced packaging provides the coolest operation available. Full gold metallization ensures excellent device lifetime and reliability.

PTFA211001E
Package H-30248-2

Two-carrier WCDMA Drive-up

V_{DD} = 28 V, I_{DQ} = 900 mA, f = 2140 MHz, 3GPP WCDMA signal, 8 dB P/A R, 10 MHz carrier spacing



Features

- Thermally-enhanced package, Pb-free and RoHS-compliant
- Broadband internal matching
- Typical two-carrier WCDMA performance at 2140 MHz, 28 V
  - Average output power = 23 W
  - Linear Gain = 16 dB
  - Efficiency = 28.5%
  - Intermodulation distortion = –37 dBc
  - Adjacent channel power = –41 dBc
- Typical CW performance, 2170 MHz, 28 V
  - Output power at P–1dB = 125 W
  - Efficiency = 57%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 28 V, 100 W (CW) output power

RF Characteristics

WCDMA Measurements (tested in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 900 mA, P_{OUT} = 23 W average
f_1 = 2135 MHz, f_2 = 2145 MHz, 3GPP signal, channel bandwidth = 3.84 MHz , peak/average = 8 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	15	16	—	dB
Drain Efficiency	η_D	27	28.5	—	%
Intermodulation Distortion	IMD	—	–37	–36	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 µA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.08	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ} = 900 mA	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	417	W
Above 25°C derate by		2.38	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 100 W CW)	$R_{\theta JC}$	0.42	°C/W

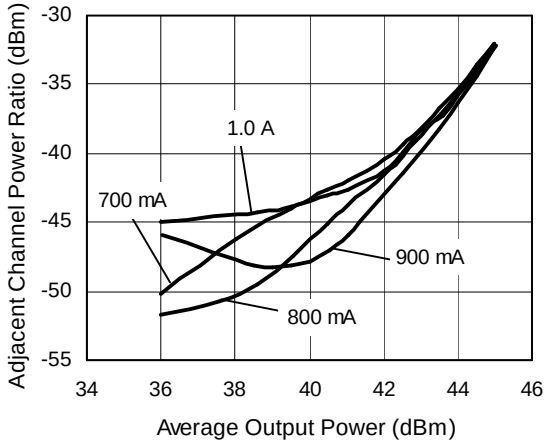
Ordering Information

Type and Version	Package Outline	Package Description	Marking
PTFA211001E V1	H-30248-2	Thermally-enhanced slotted flange, single-ended	PTFA211001E

Typical Performance (data taken in a production test fixture)

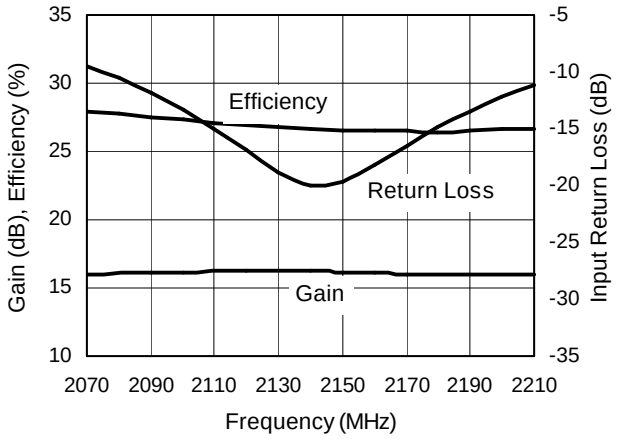
Two-carrier WCDMA at Various Biases

V_{DD} = 28 V, f = 2140 MHz, 3GPP WCDMA signal,
P/AR = 8 dB, 10 MHz carrier spacing, series show I_{DQ}



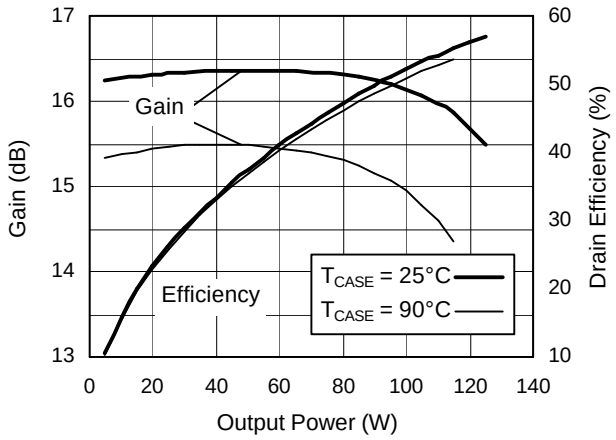
Broadband Performance

V_{DD} = 28 V, I_{DQ} = 900 mA, P_{OUT} = 44.0 dBm



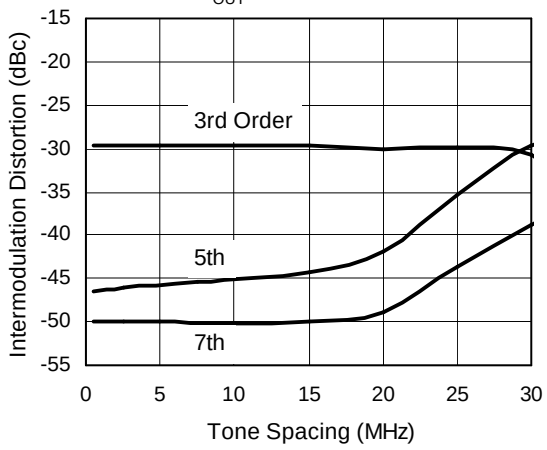
Power Sweep, CW Conditions

V_{DD} = 28 V, I_{DQ} = 900 mA, f = 2170 MHz



Intermodulation Distortion Products vs. Tone Spacing

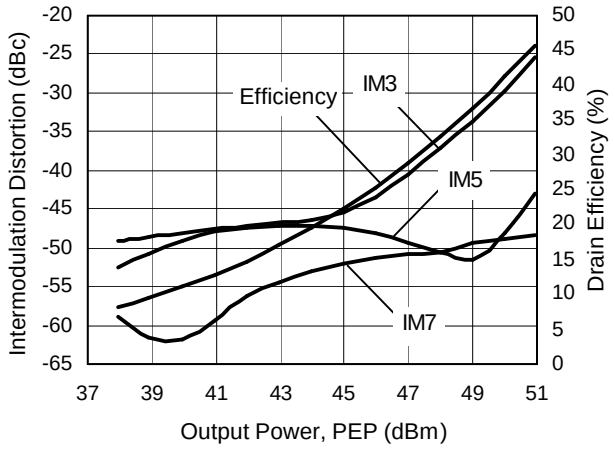
V_{DD} = 28 V I_{DQ} = 900 mA, f = 2140 MHz,
P_{OUT} = 50 dBm PEP



Typical Performance (cont.)

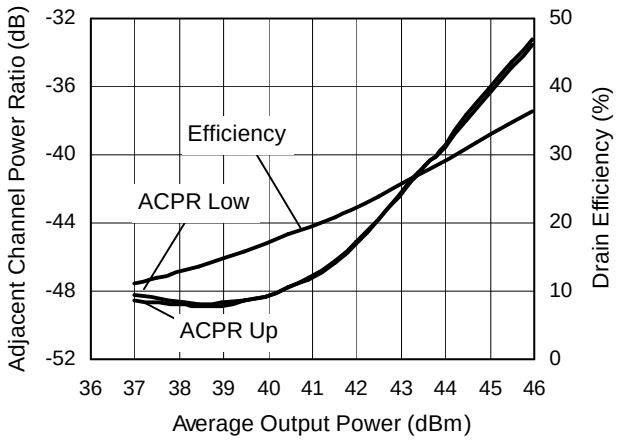
2-Tone Drive-up

V_{DD} = 28 V, I_{DQ} = 900 mA,
f = 2140 MHz, tone spacing = 1 MHz



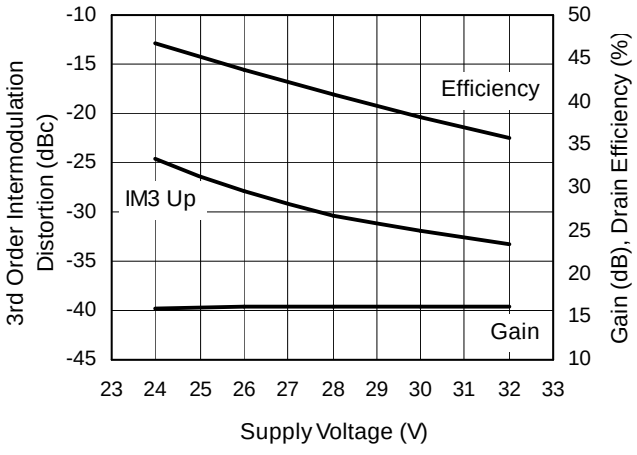
Single-carrier WCDMA Drive-up

V_{DD} = 28 V, I_{DQ} = 900mA, f = 2140 MHz,
3GPP WCDMA signal, TM1 w/16 DPCH, 67% clipping,
P/A R = 8.5 dB, 3.84 MHz BW



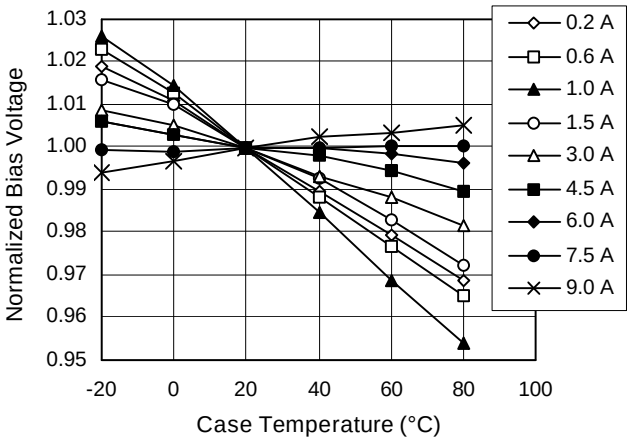
IM3, Drain Efficiency and Gain vs. Supply Voltage

I_{DQ} = 900 mA, f = 2140 MHz, tone spacing = 1 MHz,
Output Power (PEP) = 50 dBm

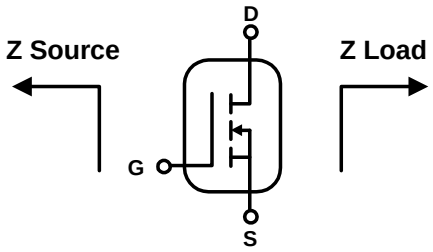


Bias Voltage vs. Temperature

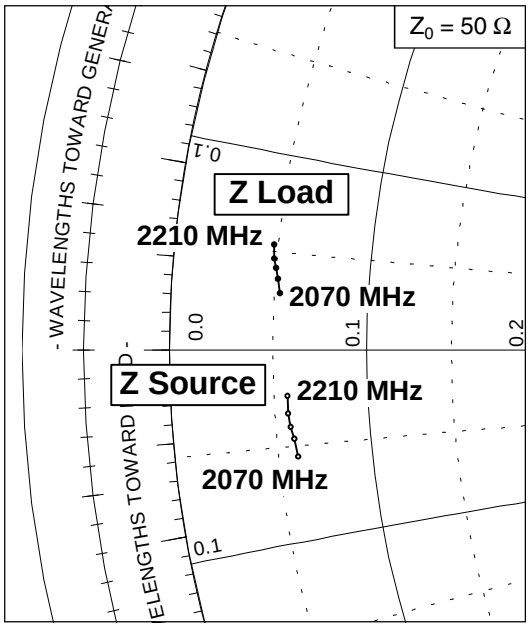
Voltage normalized to typical gate voltage,
series show current



Broadband Circuit Impedance

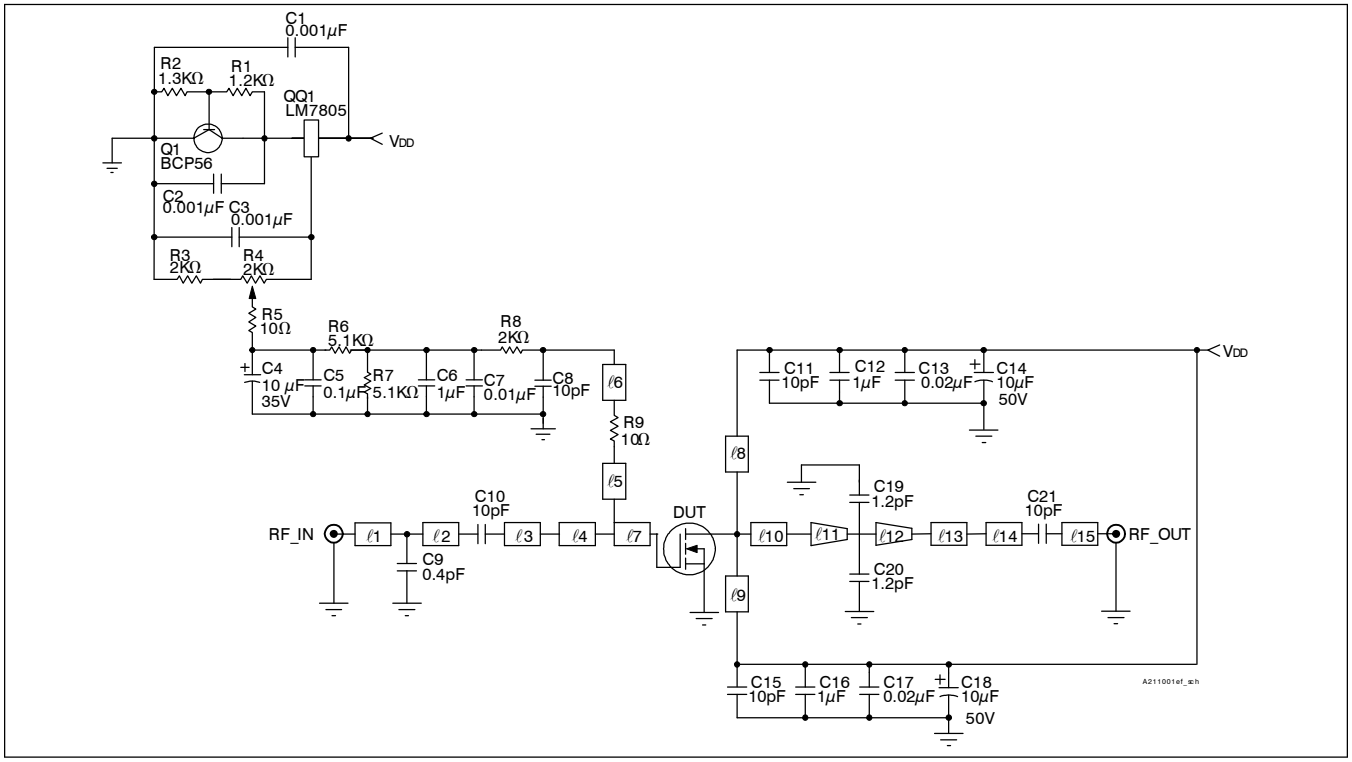


Frequency	Z Source W		Z Load W	
MHz	R	jX	R	jX
2070	3.02	–2.80	2.64	1.47
2110	2.96	–2.32	2.57	1.84
2140	2.89	–2.01	2.51	2.10
2170	2.84	–1.66	2.44	2.34
2210	2.85	–1.20	2.40	2.70



See next page for circuit information

Reference Circuit



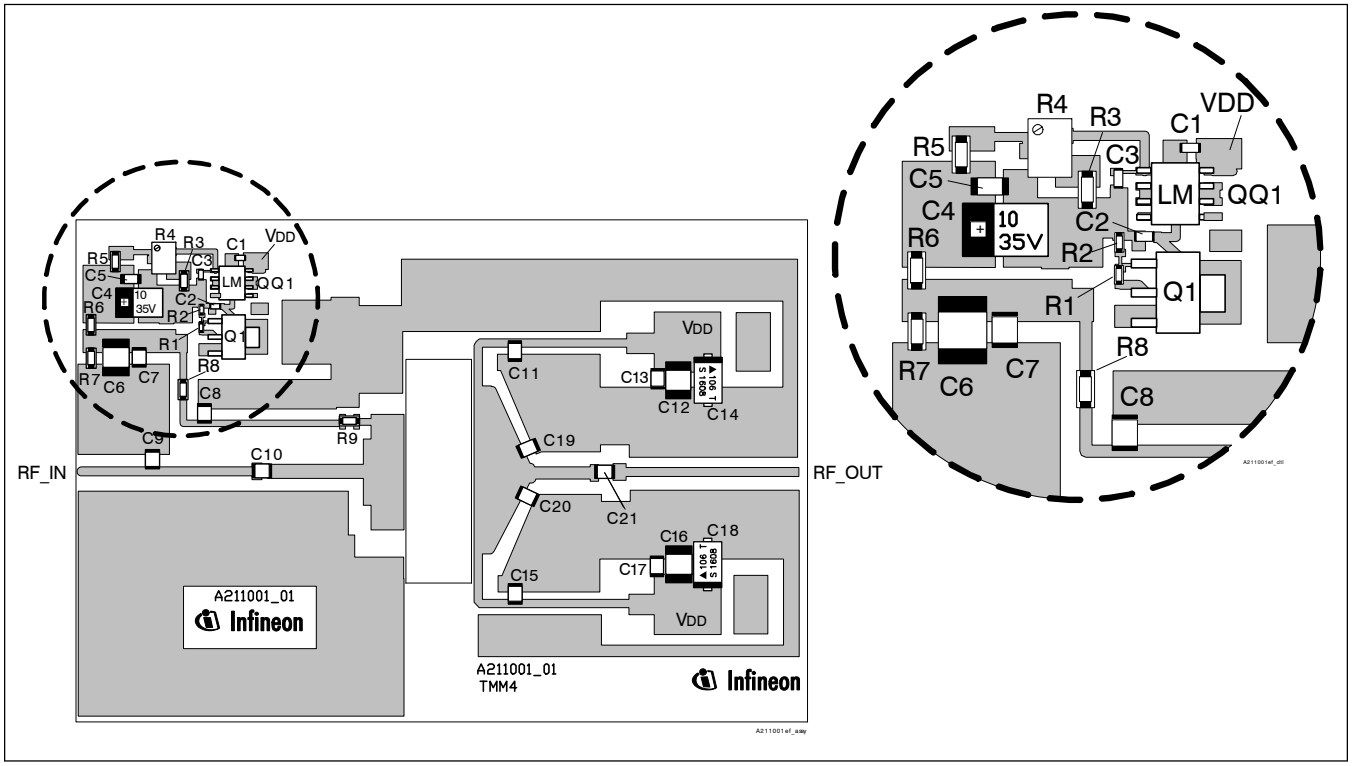
Reference circit schematic for ƒ = 2140 MHz

Circuit Assembly Information			
DUT	PTFA211001E	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, ε_r = 4.5	Rogers TMM4	2 oz. copper

Microstrip	Electrical Characteristics at 2140 MHz[1]	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.130 λ, 52.0 Ω	9.96 x 1.30	0.392 x 0.051
ℓ2	0.235 λ, 52.0 Ω	18.01 x 1.30	0.709 x 0.051
ℓ3	0.191 λ, 39.0 Ω	14.30 x 2.08	0.563 x 0.082
ℓ4	0.018 λ, 11.5 Ω	1.22 x 10.03	0.048 x 0.395
ℓ5	0.024 λ, 64.0 Ω	1.88 x 0.89	0.074 x 0.035
ℓ6	0.261 λ, 64.0 Ω	20.32 x 0.89	0.800 x 0.035
ℓ7	0.073 λ, 7.0 Ω	4.98 x 17.68	0.196 x 0.696
ℓ8, ℓ9	0.170 λ, 55.0 Ω	13.08 x 1.17	0.515 x 0.046
ℓ10	0.043 λ, 5.0 Ω	2.95 x 25.40	0.116 x 1.000
ℓ11 (taper)	0.059 λ, 5.0 Ω / 17.4 Ω	4.01 x 25.40 / 6.17	0.158 x 1.000 / 0.243
ℓ12 (taper)	0.033 λ, 17.4 Ω / 42.0 Ω	2.36 x 6.17 / 1.83	0.093 x 0.243 / 0.072
ℓ13	0.124 λ, 42.0 Ω	9.30 x 1.83	0.366 x 0.072
ℓ14	0.381 λ, 50.0 Ω	29.11 x 1.37	1.146 x 0.054

[1]Electrical characteristics are rounded.

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4	Tantalum capacitor, 10 µF, 35 V	Digi-Key	PCS6106TR-ND
C5	Capacitor, 0.1 µF	Digi-Key	PCC104BCT-ND
C6, C12, C16	Capacitor, 1 µF	ATC	920C105
C7	Capacitor, 0.01 µF	Digi-Key	200B 103
C8, C10, C11, C15, C21	Ceramic capacitor, 10 pF	ATC	100B 100
C9	Ceramic capacitor, 0.4 pF	ATC	100B 0R4
C13, C17	Capacitor, 0.02 µF	Digi-Key	200B203
C14, C18	Tantalum capacitor, 10 µF, 50 V	Gerrette Electronics	TPS106K050R0400
C19, C20	Ceramic capacitor, 1.2 pF	ATC	100B 1R2
Q1	Transistor	Infineon Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor 1.2 k-ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor 1.3 k-ohms	Digi-Key	P1.3KGCT-ND
R3, R8	Chip resistor 2 k-ohms	Digi-Key	P2KECT-ND
R4	Potentiometer, 2 k-ohms	Digi-Key	3224W-202ETR-ND
R5, R9	Chip resistor 10 ohms	Digi-Key	P10ECT-ND
R6, R7	Chip resistor 5.1 k-ohms	Digi-Key	P5.1KECT-ND

[1]*Gerber Files for this circuit available on our Web site:* ***www.infineon.com/rfpower***

Package Outline Specifications

Package H-30248-2

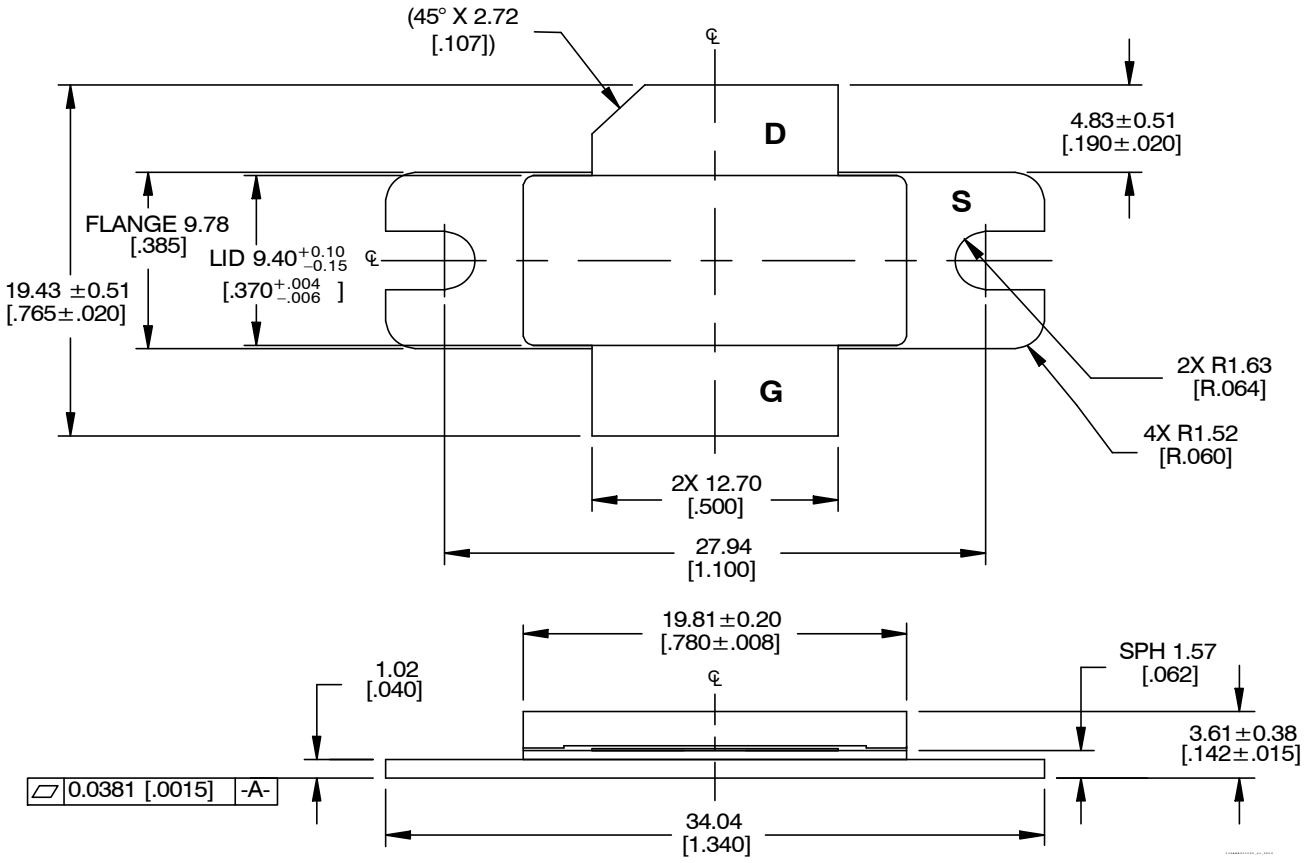


Diagram Notes:

1. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
2. All tolerances ± 0.127 [.005] unless specified otherwise.
3. Pins: D = drain, S = source, G = gate.
4. Interpret dimensions and tolerances per ASME Y14.5M-1994.
5. Primary dimensions are mm. Alternate dimensions are inches.
6. Gold plating thickness:
   S - flange: 2.54 micron [100 microinch] (min)
   D, G - leads: 1.14 ± 0.38 micron [45 ± 15 microinch]

Find the latest and most complete information about products and packaging at the Infineon Internet page ***http://www.infineon.com/rfpower***

PTFA211001E

Revision History:	**2008-03-04**	Data Sheet
Previous Version:	2005-02-04, Data Sheet	
Page	Subjects (major changes since last revision)	
All	Remove references to alternate products.	

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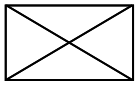

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