# PTK94N50FD

#### **500V N-Channel MOSFET**

#### **General Features**

- Proprietary New Planar Technology
- $\triangleright$  R<sub>DS(ON),typ.</sub>=47 m $\Omega$ @V<sub>GS</sub>=10V
- Low Gate Charge Minimize Switching Loss
- Fast Intrinsic Diode, Fast Recovery Body Diode

# **Applications**

- Uninterruptible Power Supply
- AC-DC Power Supply
- > SMPS

#### **Ordering Information**

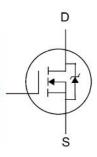
Part Number	Package	Brand
PTK94N50FD	TO-264	ľ

# **Absolute Maximum Ratings**



BV <sub>DSS</sub>	R <sub>DS(ON),typ.</sub>	ID
500V	47mΩ	94A

# G D S TO-264



G

Package Not to Scale

 $T_C {=} 25 ^{\circ} \!\! \mathrm{C}$  unless otherwise specified

Symbol	Parameter	PTK94N50FD	Unit
V <sub>DSS</sub>	Drain-to-Source Voltage <sup>[1]</sup>	500	V
V <sub>GSS</sub>	Gate-to-Source Voltage	±30	v
ID	Continuous Drain Current	94	
I <sub>D @ Tc =100</sub> ℃ Continuous Drain Current @ Tc=100℃		65	A
I <sub>DM</sub>	Pulsed Drain Current at V <sub>GS</sub> =10V <sup>[2]</sup>	376	
E <sub>AS</sub>	Single Pulse Avalanche Energy	6000	
E <sub>AR</sub>	Avalanche Energy ,Repetitive	500	— mJ
dv/dt	Peak Diode Recovery dv/dt <sup>[3]</sup>	30	V/ns
<b>D</b>	Power Dissipation	1300	W
PD	Derating Factor above 25°C	12	W/°C
T <sub>L</sub> T <sub>PAK</sub>	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	°C
T <sub>J</sub> & T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

# **Thermal Characteristics**

Symbol	Parameter	PTK94N50FD	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	0.096	
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	30	°C/W

# **Electrical Characteristics**

#### **OFF Characteristics** $T_J = 25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	500			V	$V_{GS}$ =0V, I <sub>D</sub> =250uA
	I <sub>DSS</sub> Drain-to-Source Leakage Current			10	uA	V <sub>DS</sub> =500V, V <sub>GS</sub> =0V
IDSS				1000		V <sub>DS</sub> =400V, V <sub>GS</sub> =0V, T <sub>J</sub> =125℃
I <sub>GSS</sub>	Gate-to-Source Leakage Current			+200	~ ^	V <sub>GS</sub> =+30V, V <sub>DS</sub> =0V
				-200	nA	V <sub>GS</sub> =-30V, V <sub>DS</sub> =0V

#### **ON Characteristics**

T₁ =25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
R <sub>DS(ON)</sub>	Static Drain-to-Source On-Resistance <sup>[4]</sup>		47	65	mΩ	V <sub>GS</sub> =10V, I <sub>D</sub> =20A
V <sub>GS(TH)</sub>	Gate Threshold Voltage	3.0		5.0	V	$V_{DS}=V_{GS}, I_D=250uA$
gfs	Forward Transconductance <sup>[4]</sup>		75		S	VDS=20V,ID=26A

#### **Dynamic Characteristics**

Essentially independent of operating temperature Symbol Parameter Min. Unit **Test Conditions** Тур. Max. Ciss Input Capacitance 13420 -----V<sub>GS</sub>=0V, Crss V<sub>DS</sub>=25V, **Reverse Transfer Capacitance** 58 --pF --f=1.0MHz Coss 1250 **Output Capacitance** \_\_\_ --- $\mathsf{Q}_\mathsf{g}$ **Total Gate Charge** 225 -----V<sub>DD</sub>=250V,  $\mathsf{Q}_{\mathsf{gs}}$ Gate-to-Source Charge 65 -----nC I<sub>D</sub>=47A, V<sub>GS</sub>=0 to 10V Gate-to-Drain (Miller) Charge 58  $Q_{gd}$ ------

#### **Resistive Switching Characteristics**

Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
td(ON)	Turn-on Delay Time		36			
trise	Rise Time		15		- nS	$V_{DD}=250V,$ I <sub>D</sub> =47A, V <sub>GS</sub> = 10V R <sub>G</sub> =1.0Ω
td(OFF)	Turn-Off Delay Time		75			
tfall	Fall Time		15			

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#### **Source-Drain Body Diode Characteristics**

#### $T_J=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min	Тур.	Max.	Unit	Test Conditions
I <sub>SD</sub>	Continuous Source Current <sup>[4]</sup>			96	A	Integral PN-diode in MOSFET
I <sub>SM</sub>	Pulsed Source Current <sup>[4]</sup>			376		
V <sub>SD</sub>	Diode Forward Voltage			1.5	V	I <sub>S</sub> =94A, V <sub>GS</sub> =0V
trr	Reverse recovery time		135	200	ns	V <sub>GS</sub> =0V ,I <sub>F</sub> =47A,
Qrr	Reverse recovery charge		1.3		uC	di⊧/dt=100A/µs

Note:

[1] T」=+25℃ to +150℃

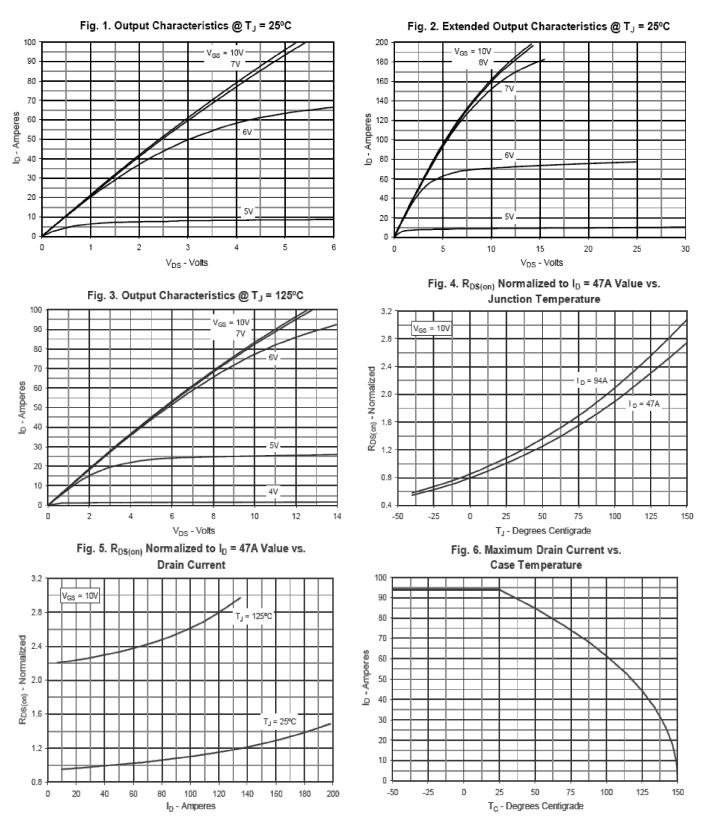
[2] Repetitive rating; pulse width limited by maximum junction temperature. [3] ISD= 47A di/dt < 100 A/ $\mu$ s, VDD < BVDss, TJ=+150 °C.

- [4] Pulse width≤380µs; duty cycle≤2%.

# PTK94N50FD

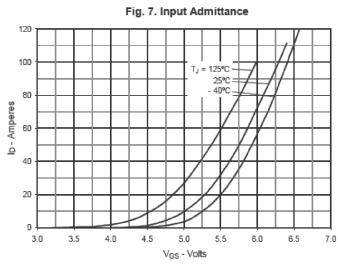
# **Typical Characteristics**

1

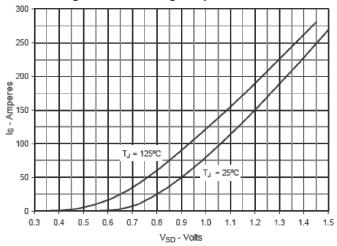


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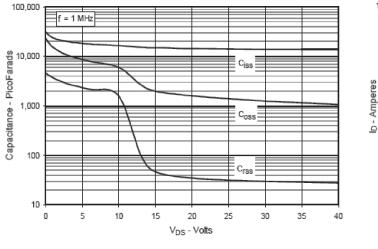
# Typical Characteristics(Cont.)











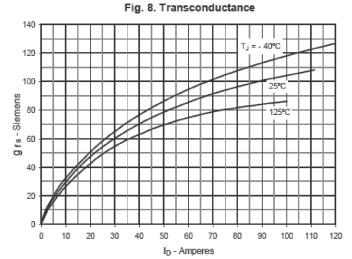
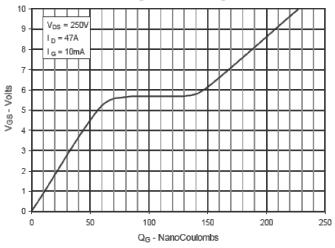
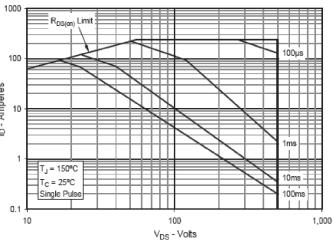


Fig. 10. Gate Charge





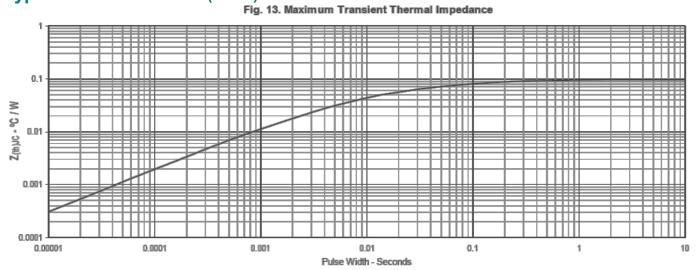


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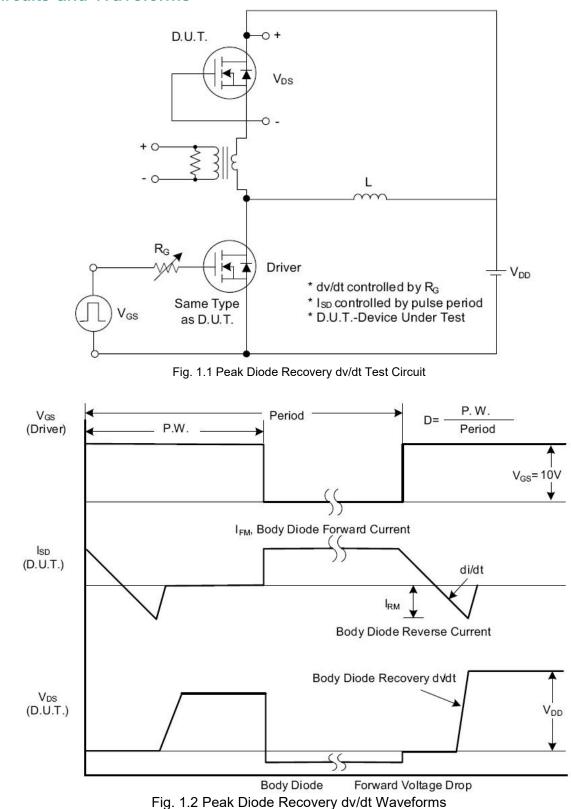
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# PTK94N50FD

# **Typical Characteristics**(Cont.)



#### **Test Circuits and Waveforms**



# PTK94N50FD

# Test Circuits and Waveforms (Cont.)

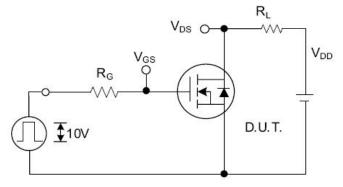


Fig. 2.1 Switching Test Circuit

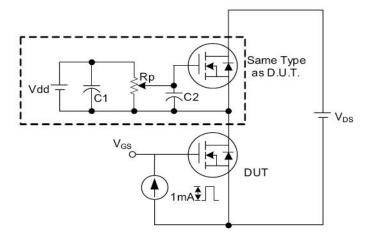


Fig. 3 . 1 Gate Charge Test Circuit

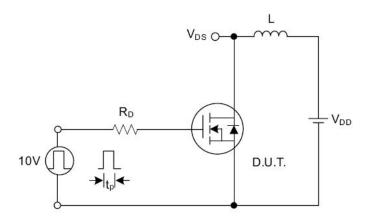


Fig. 4.1 Unclamped Inductive Switching Test Circuit

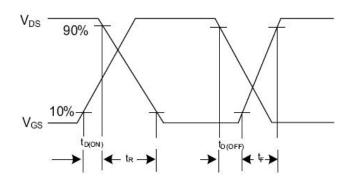


Fig. 2.2 Switching Waveforms

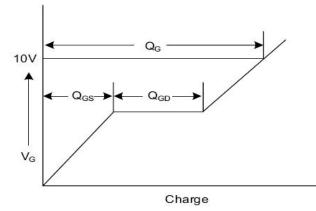
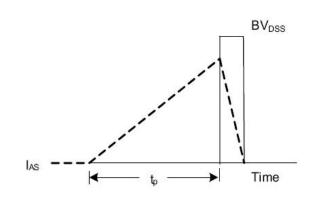
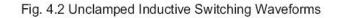


Fig. 3.2 Gate Charge Waveform





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