



# PUSB3AB4

ESD protection for ultra high-speed interfaces

Rev. 1 — 25 August 2015

Objective data sheet

## 1. Product profile

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### 1.1 General description

The device is designed to protect high-speed interfaces such as SuperSpeed USB 3.1 at 10 Gbps, High-Definition Multimedia Interface (HDMI), DisplayPort, external Serial Advanced Technology Attachment (eSATA) and Low Voltage Differential Signaling (LVDS) interfaces against ElectroStatic Discharge (ESD).

The device includes a high-level ESD protection diode structure protecting sensitive transmitters and receivers for ultra high-speed signal lines. The device is encapsulated in a leadless small DFN2510A-10 (SOT1176-1) plastic package.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of only 0.2 pF maximum. These diodes utilize a snapback structure in order to provide protection to downstream components from ESD voltages up to  $\pm 15$  kV contact exceeding IEC 61000-4-2, level 4.

### 1.2 Features and benefits

- System-level ESD protection for USB 2.0 and SuperSpeed USB 3.1 at 10 Gbps, HDMI, DisplayPort, eSATA and LVDS
- Line capacitance of only 0.2 pF maximum for each channel
- Outstanding system protection: extremely deep snapback combined with dynamic resistance of only 0.4  $\Omega$ .
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of  $\pm 15$  kV exceeding IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Signal lines with  $\leq 0.05$  pF matching capacitance between signal pairs
- Design-friendly 'pass-through' signal routing

### 1.3 Applications

The device is designed for high-speed receiver and transmitter port protection:

- Smartphones, tablet computers, Mobile Internet Devices (MID) and portable devices
- TVs and monitors
- DVD recorders and players
- Notebooks, main board graphic cards and ports
- Set-top boxes and game consoles



## 2. Pinning information

Table 1. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CH1	channel 1 ESD protection	<p>Transparent top view</p>	<p>aaa-019396</p>
2	CH2	channel 2 ESD protection		
3	GND	ground		
4	CH3	channel 3 ESD protection		
5	CH4	channel 4 ESD protection		
6	n.c.	not connected		
7	n.c.	not connected		
8	GND	ground		
9	n.c.	not connected		
10	n.c.	not connected		

## 3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PUSB3AB4	DFN2510A-10	plastic extremely thin small outline package; no leads; 10 terminals; body 1 × 2.5 × 0.5 mm	SOT1176-1

## 4. Marking

Table 3. Marking codes

Type number	Marking code
PUSB3AB4	AB

## 5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_I$	input voltage		-0.5	+3.3	V
$V_{ESD}$	electrostatic discharge voltage	IEC 61000-4-2, level 4 [1]			
		contact discharge	-15	+15	kV
		air discharge	-15	+15	kV
$I_{PPM}$	rated peak pulse current	$t_p = 8/20 \mu s$	-7	7	A
$T_{amb}$	ambient temperature		-40	+85	°C
$T_{stg}$	storage temperature		-55	+125	°C

[1] All pins to ground.

## 6. Characteristics

**Table 5. Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{BR}$	breakdown voltage	$I_I = 1\text{ mA}$	5.5	9	-	V
$I_{LR}$	reverse leakage current	per channel; $V_I = 5\text{ V}$	-	<1	100	nA
$V_F$	forward voltage	$I_I = 1\text{ mA}$	-	0.7	-	V
$C_{line}$	line capacitance		[1]	0.17	0.2	pF
$r_{dyn}$	dynamic resistance	TLP	[2]			
		positive transient	-	0.4	-	$\Omega$
		negative transient	-	0.4	-	$\Omega$
$V_{sbck}$	snapback voltage	$I_I = 1\text{ A}$ ; TLP 100/10 ns	-	3.3	-	V
$V_{CL}$	clamping voltage	$I_{PP} = 5\text{ A}$ ; positive transient	[3]	4.5	-	V
		$I_{PP} = -5\text{ A}$ ; negative transient	[3]	-4.5	-	V

[1] This parameter is guaranteed by design.

[2] 100 ns Transmission Line Pulse (TLP); 50  $\Omega$ ; pulser at 80 ns.

[3] According to IEC 61000-4-5 (8/20  $\mu\text{s}$  current waveform).

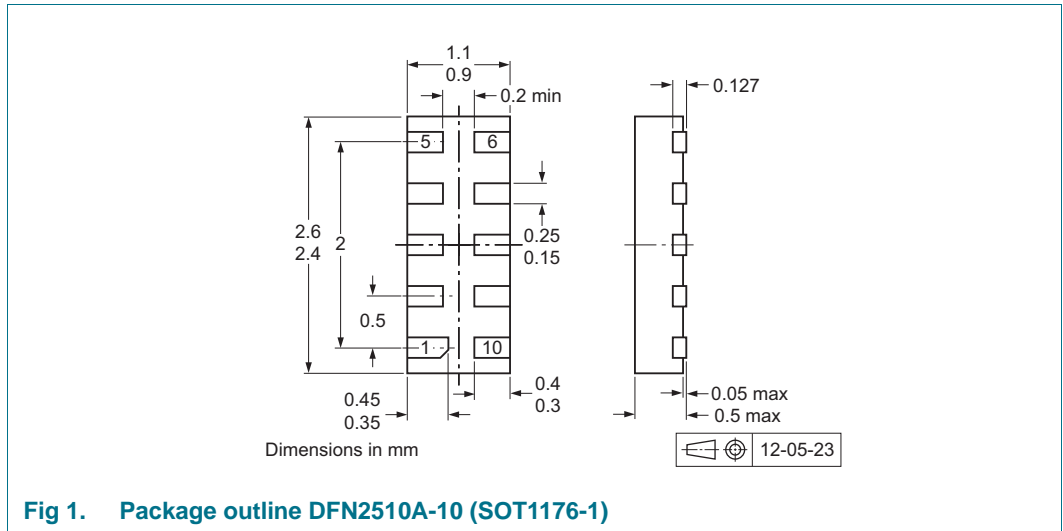
The device uses an advanced clamping structure showing a negative dynamic resistance. This snapback behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

## 7. Application information

The device is designed to provide high-level ESD protection for high-speed serial data buses such as HDMI, DisplayPort, eSATA and LVDS data lines.

When designing the PCB, give careful consideration to impedance matching and signal coupling. Do not connect the signal lines to unlimited current sources like, for example, a battery.

## 8. Package outline



9. Soldering

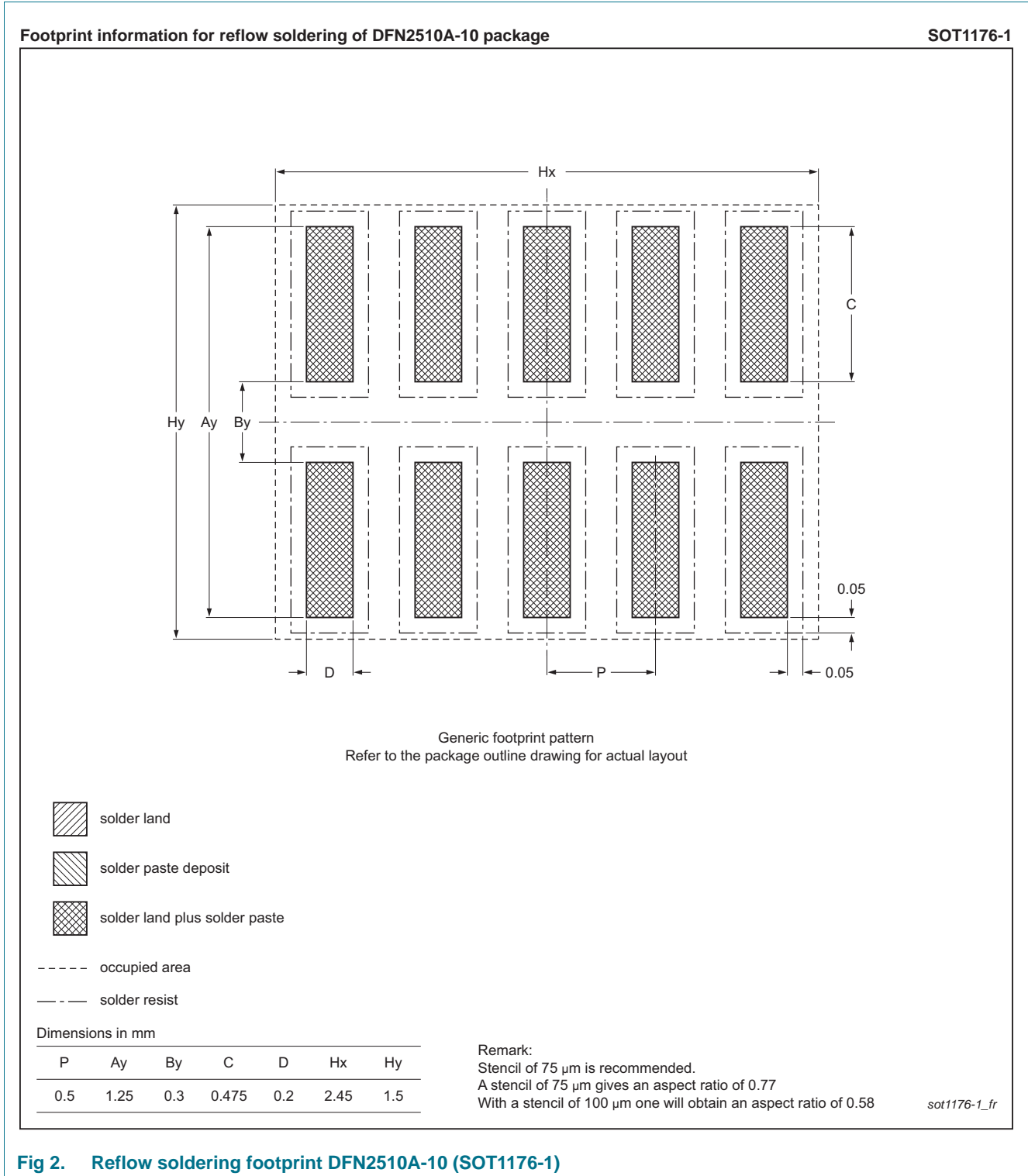


Fig 2. Reflow soldering footprint DFN2510A-10 (SOT1176-1)

## 10. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PUSB3AB4 v.1	20150825	Objective data sheet	-	-

## 11. Legal information

### 11.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 25 August 2015

Document identifier: PUSB3AB4