

ESD protection for ultra high-speed interfaces Rev. 1 — 10 May 2017

**Product data sheet** 

#### **Product profile** 1.

### **1.1 General description**

The device is designed to protect high-speed interfaces such as SuperSpeed USB, High-Definition Multimedia Interface (HDMI), DisplayPort, external Serial Advanced Technology Attachment (eSATA) and Low Voltage Differential Signaling (LVDS) interfaces against ElectroStatic Discharge (ESD).

The device includes four high-level ESD protection diode structures for ultra high-speed signal lines and is encapsulated in a leadless small DFN2510A-10 (SOT1176-1) plastic package.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of only 0.5 pF. These diodes utilize a unique snap-back structure in order to provide protection to downstream components from ESD voltages up to ±10 kV contact exceeding IEC 61000-4-2, level 4.

#### 1.2 Features and benefits

- System ESD protection for USB 2.0 and SuperSpeed USB 3.1, HDMI 2.0, DisplayPort, eSATA and LVDS
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±10 kV exceeding IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Signal lines with ≤ 0.05 pF matching capacitance between signal pairs
- Line capacitance of only 0.5 pF for each channel
- Design-friendly 'pass-through' signal routing

### 1.3 Applications

The device is designed for high-speed receiver and transmitter port protection:

- TVs and monitors
- DVD recorders and players
- Notebooks, main board graphic cards and ports
- Set-top boxes and game consoles



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### 2. Pinning information

Table	Table 1. Pinning						
Pin	Symbol	Description	Simplified outline	Graphic symbol			
1	CH1	channel 1 ESD protection					
2	CH2	channel 2 ESD protection					
3	GND	ground					
4	СНЗ	channel 3 ESD protection					
5	CH4	channel 4 ESD protection	Transparent top view	本本   本本			
6	n.c.	not connected		3.8			
7	n.c.	not connected		3, o 018aaa001			
8	GND	ground					
9	n.c.	not connected					
10	n.c.	not connected					

# 3. Ordering information

#### Table 2.Ordering information

Type number	Package		
	Name	Description	Version
PUSB3F97	DFN2510A-10	plastic extremely thin small outline package; no leads; 10 terminals; body $1 \times 2.5 \times 0.5$ mm	SOT1176-1

### 4. Marking

Table 3. Marking codes	Marking codes				
Type number	Marking code				
PUSB3F97	96				

### 5. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
VI	input voltage			-0.5	+5.5	V
V <sub>ESD</sub>	electrostatic discharge voltage	IEC 61000-4-2, level 4	[1]			
		contact discharge		-10	+10	kV
		air discharge		–15	+15	kV
T <sub>amb</sub>	ambient temperature			-40	+85	°C
T <sub>stg</sub>	storage temperature			-55	+125	°C

[1] All pins to ground.

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## 6. Characteristics

#### Table 5. Characteristics

 $T_{amb} = 25 \ ^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>BR</sub>	breakdown voltage	l <sub>l</sub> = 1 mA		6	-	-	V
I <sub>LR</sub>	reverse leakage current	per channel; V <sub>I</sub> = 3 V		-	-	1	μA
V <sub>F</sub>	forward voltage	l <sub>l</sub> = 1 mA		-	0.7	-	V
Cline	line capacitance	f = 1 MHz; V <sub>I</sub> = 3.3 V	[1]	-	0.5	0.6	pF
$\Delta C_{line}$	line capacitance difference	f = 1 MHz; V <sub>I</sub> = 3.3 V	[1]	-	0.05	-	pF
r <sub>dyn</sub>	dynamic resistance	surge	[2]				
		positive transient		-	0.41	-	Ω
		negative transient		-	0.26	-	Ω
		TLP	[3]				
		positive transient		-	0.43	-	Ω
		negative transient		-	0.28	-	Ω
V <sub>CL</sub>	clamping voltage	I <sub>PP</sub> = 5.2 A	[2]				
		positive transient		-	4.6	-	V
		I <sub>PP</sub> = -4.4 A	[2]				
		negative transient		-	-2.2	-	V

[1] This parameter is guaranteed by design.

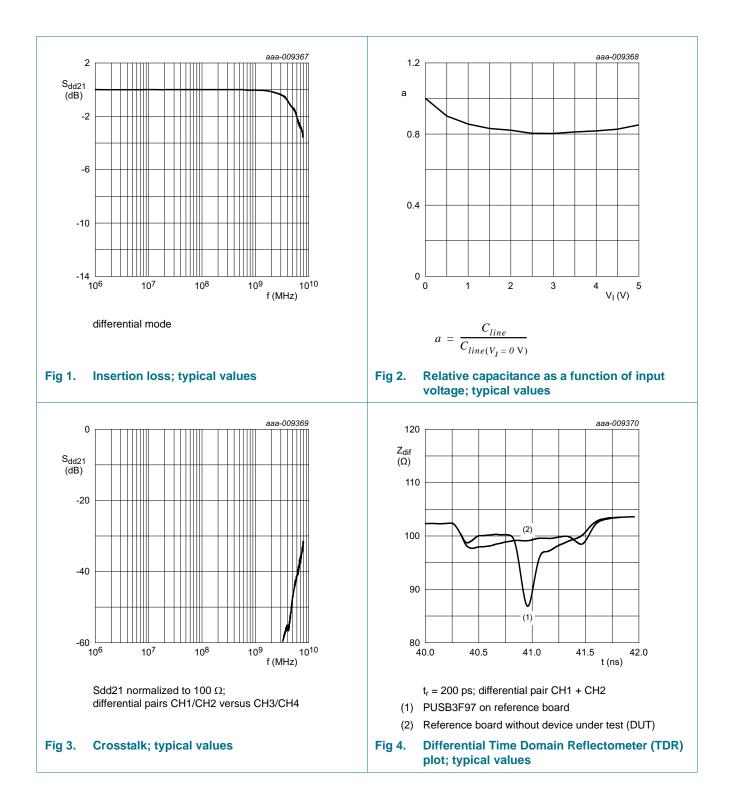
[2] According to IEC 61000-4-5 (8/20  $\mu s$  current waveform).

[3] 100 ns Transmission Line Pulse (TLP); 50  $\Omega$ ; pulser at 80 ns.

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# PUSB3F97

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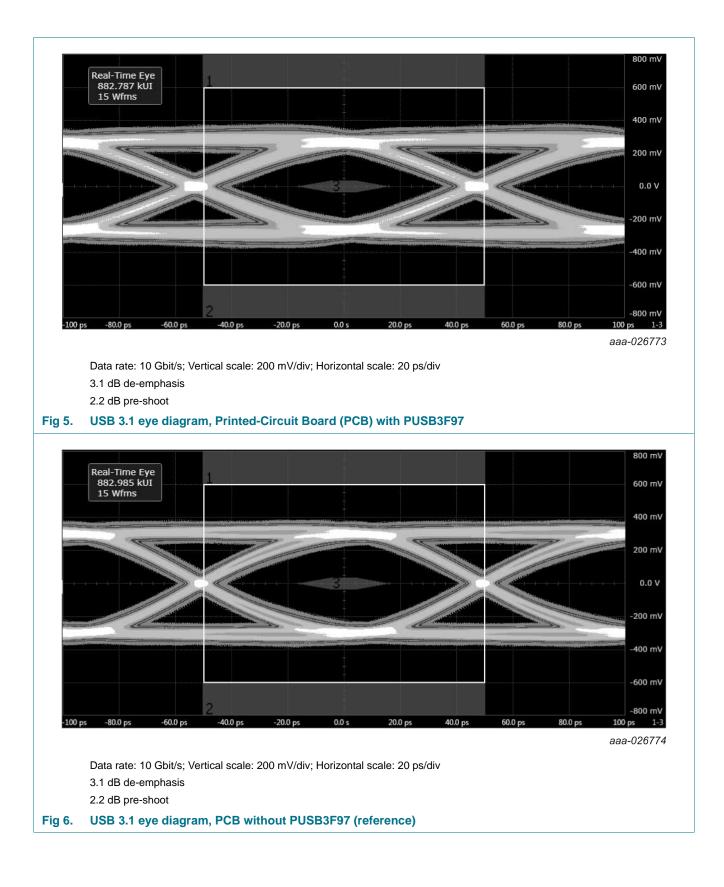


Product data sheet

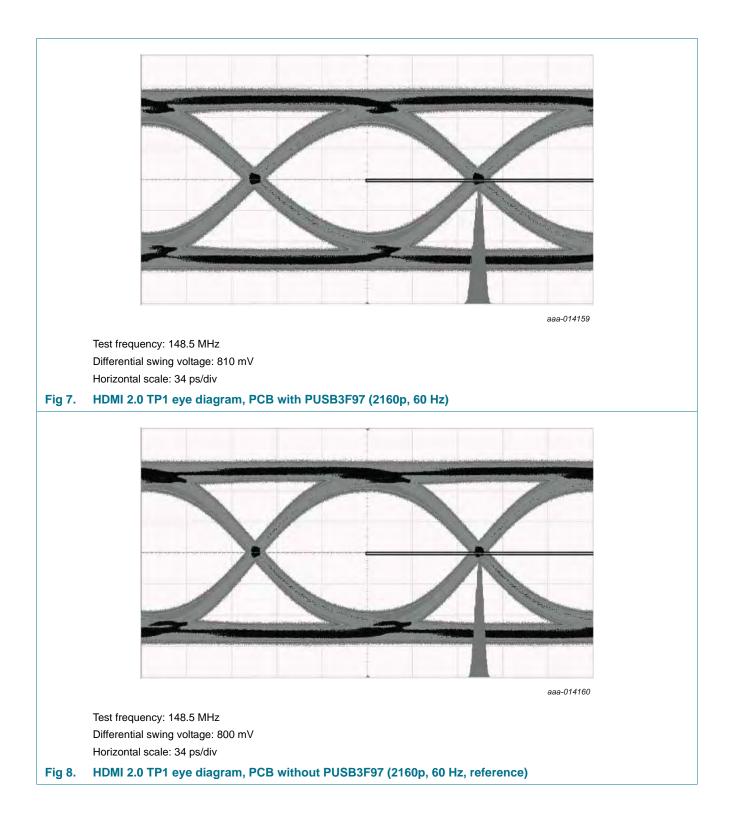
PUSB3F97

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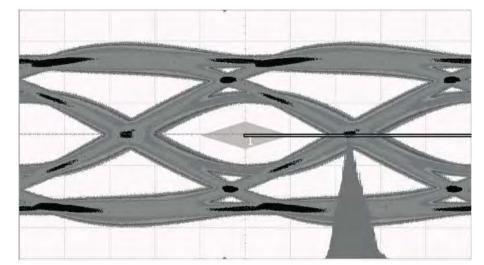
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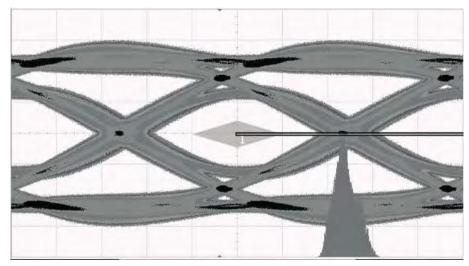
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aaa-014161

Test frequency: 148.5 MHz Differential swing voltage: 809 mV Horizontal scale: 34 ps/div Remark: Measured at Test Point 2 (TP2) worst cable emulator, reference cable equalizer and worst case positive skew.

#### HDMI 2.0 TP2 eye diagram, PCB with PUSB3F97 (2160p, 60 Hz) Fig 9.



aaa-014162

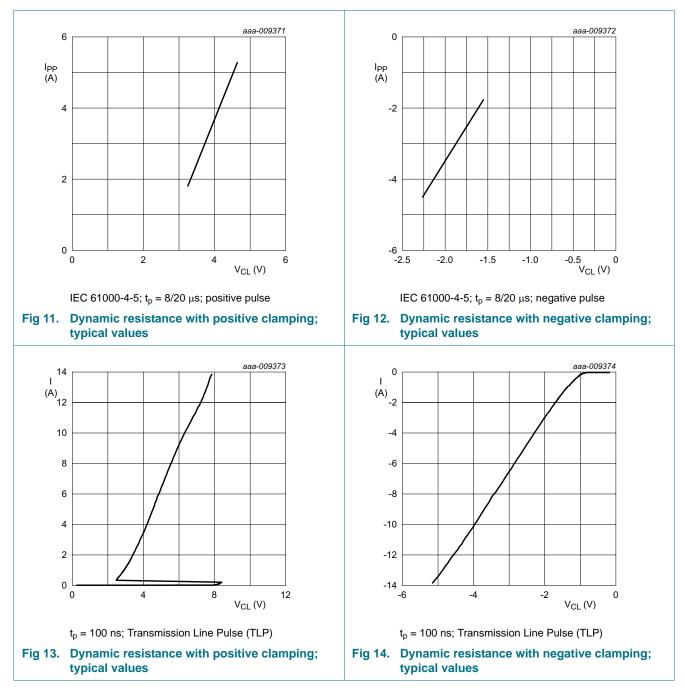
Test frequency: 148.5 MHz Differential swing voltage: 820 mV Horizontal scale: 34 ps/div Remark: Measured at Test Point 2 (TP2) worst cable emulator, reference cable equalizer and worst case positive skew. Fig 10. HDMI 2.0 TP2 eye diagram, PCB without PUSB3F97 (2160p, 60 Hz, reference)

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The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

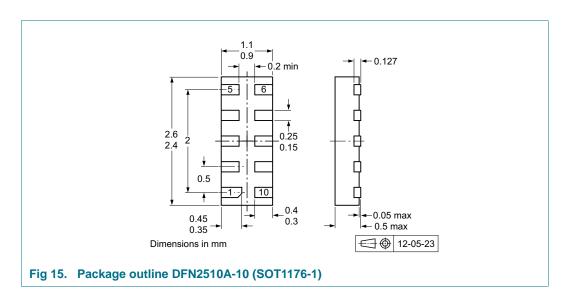
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## 7. Application information

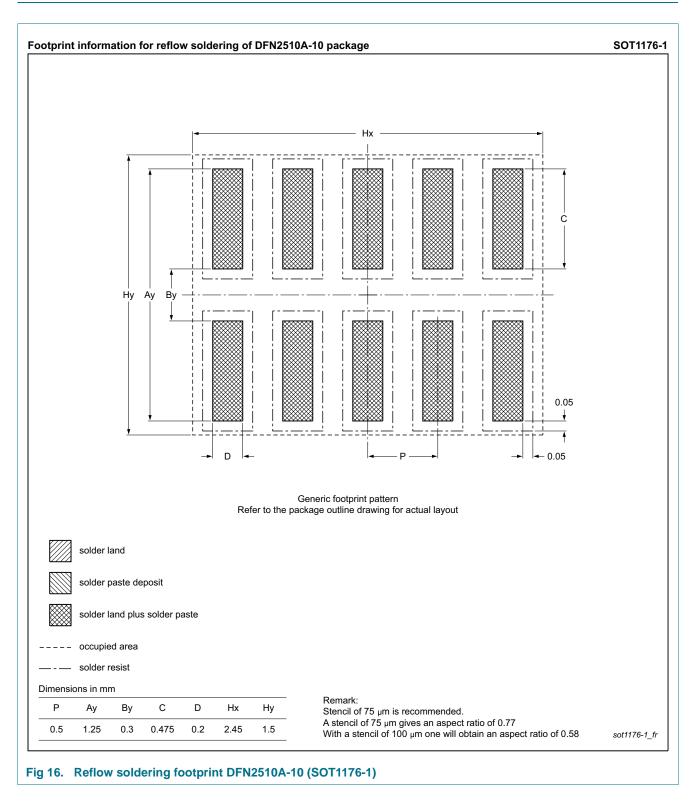
The device is designed to provide high-level ESD protection for high-speed serial data buses such as USB3.1, HDMI, DisplayPort, eSATA and LVDS data lines.

When designing the Printed-Circuit Board (PCB), give careful consideration to impedance matching and signal coupling. Do not connect the signal lines to unlimited current sources like, for example, a battery.

### 8. Package outline



### 9. Soldering



# **10. Revision history**

Table 6.   Revision history						
Document ID	Release date	Data sheet status	Change notice	Supersedes		
PUSB3F97 v.1	20170510	Product data sheet	-	-		

### **11. Legal information**

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Document status[1][2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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