

PUSB3FR6

ESD protection for ultra high-speed interfaces

Rev. 1 — 25 February 2015

Product data sheet

1. Product profile

1.1 General description

The device is designed to protect high-speed interfaces such as SuperSpeed and Hi-Speed USB combination, SD-memory card 3.0 and thunderbolt interfaces against ElectroStatic Discharge (ESD).

The device includes six high-level ESD protection diode structures for ultra high-speed signal lines. The device is encapsulated in a leadless ultra small DFN2111-7 (SOT1358-1) Surface-Mounted Device (SMD) plastic package.

All signal lines are protected by a special diode structure offering ultra low line capacitance of only 0.35 pF. These diodes utilize a snap-back structure in order to provide protection to downstream components from ESD voltages up to ± 15 kV contact exceeding IEC 61000-4-2, level 4.

1.2 Features and benefits

- System-level ESD protection for USB 2.0 and USB 3.1 combination, SD-memory card and thunderbolt interfaces
- Supports SuperSpeed USB 3.1 at 10 Gbps
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ± 15 kV exceeding IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Line capacitance of only 0.35 pF for each channel
- Design-friendly 'pass-through' signal routing

1.3 Applications

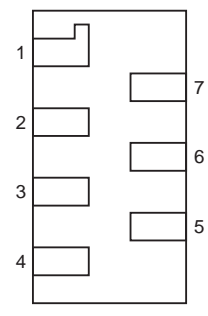
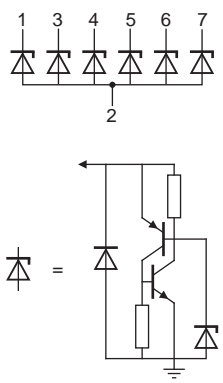
The device is designed for high-speed receiver and transmitter port protection:

- Portable and wearable devices
- Smartphones and tablet PCs
- TVs and monitors
- DVD recorders and players
- Notebooks, main board graphic cards and ports
- Set-top boxes and game consoles



2. Pinning information

Table 1. Pinning

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|--------------------------|--|---|
| 1 | CH1 | channel 1 ESD protection |  <p>Transparent top view</p> |  <p>aaa-016877</p> |
| 2 | GND | ground | | |
| 3 | CH2 | channel 2 ESD protection | | |
| 4 | CH3 | channel 3 ESD protection | | |
| 5 | CH4 | channel 4 ESD protection | | |
| 6 | CH5 | channel 5 ESD protection | | |
| 7 | CH6 | channel 6 ESD protection | | |

3. Ordering information

Table 2. Ordering information

| Type number | Package | | |
|-------------|-----------|--|-----------|
| | Name | Description | Version |
| PUSB3FR6 | DFN2111-7 | plastic extremely thin small outline package; no leads; 7 terminals; body 1.1 × 2.1 × 0.5 mm | SOT1358-1 |

4. Marking

Table 3. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PUSB3FR6 | FR |

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|---------------------------------|----------------------------|------|------|------|
| V_I | input voltage | | -0.5 | +3.3 | V |
| V_{ESD} | electrostatic discharge voltage | IEC 61000-4-2, level 4 [1] | | | |
| | | contact discharge | -15 | +15 | kV |
| | | air discharge | -15 | +15 | kV |
| I_{PPM} | rated peak pulse current | $t_p = 8/20 \mu s$ | -7 | 7 | A |
| T_{amb} | ambient temperature | | -40 | +85 | °C |
| T_{stg} | storage temperature | | -55 | +125 | °C |

[1] All pins to ground.

6. Characteristics

Table 5. Characteristics

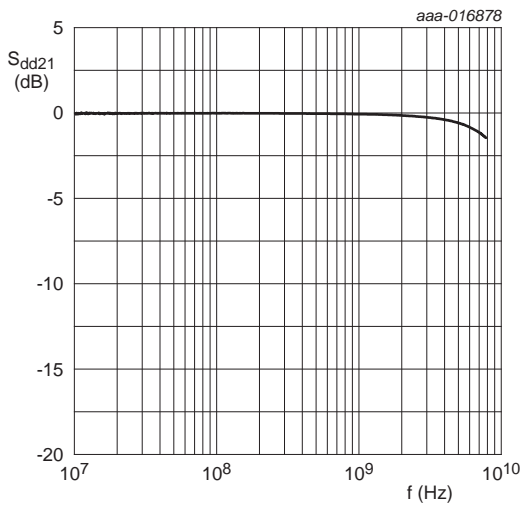
$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|-------------------------|--|-----|------|------|----------|
| V_{BR} | breakdown voltage | $I_I = 1\text{ mA}$ | 6 | - | - | V |
| I_{LR} | reverse leakage current | per channel; $V_I = 3\text{ V}$ | - | 1 | 100 | nA |
| V_F | forward voltage | $I_I = 1\text{ mA}$ | - | 0.7 | - | V |
| C_{iine} | line capacitance | $f = 1\text{ MHz}$; $V_I = 1.5\text{ V}$ | [1] | 0.35 | 0.40 | pF |
| r_{dyn} | dynamic resistance | TLP | [3] | | | |
| | | positive transient | - | 0.29 | - | Ω |
| | | negative transient | - | 0.29 | - | Ω |
| V_{sbck} | snapback voltage | $I_I = 1\text{ A}$; TLP 100/10 ns | - | 1.6 | - | V |
| V_{CL} | clamping voltage | $I_{PP} = 5\text{ A}$; positive transient | [2] | 3 | - | V |
| | | $I_{PP} = -5\text{ A}$; negative transient | [2] | -3 | - | V |

[1] This parameter is guaranteed by design.

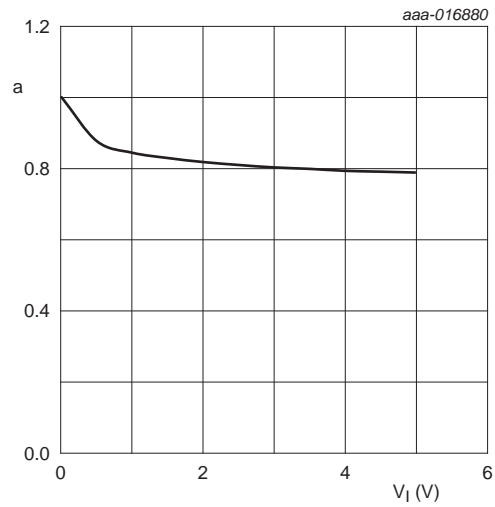
[2] According to IEC 61000-4-5 (8/20 μs current waveform).

[3] 100 ns Transmission Line Pulse (TLP); 50 Ω ; pulser at 80 ns.



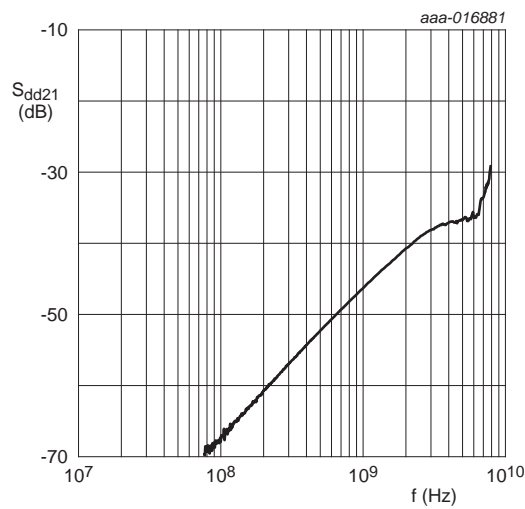
differential mode

Fig 1. Insertion loss; typical values



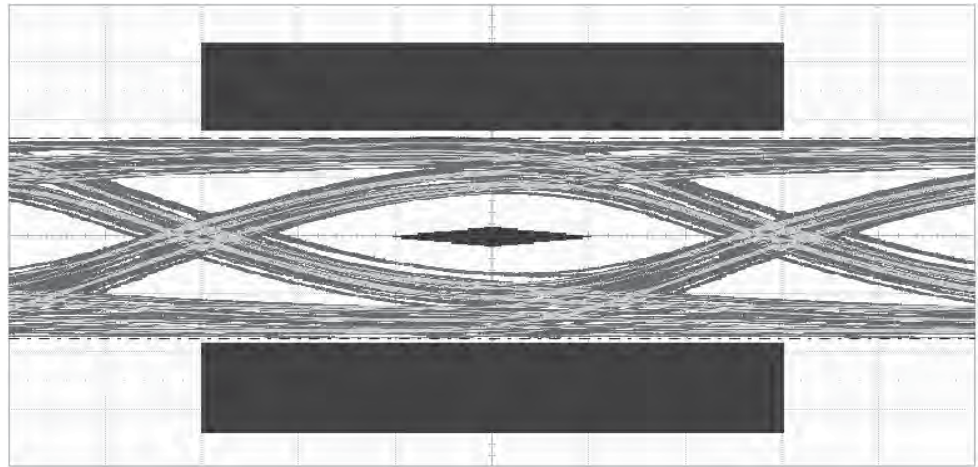
$$a = \frac{C_{line}}{C_{line}(V_I = 0 \text{ V})}$$

Fig 2. Relative capacitance as a function of input voltage; typical values



normalized to 100 Ω

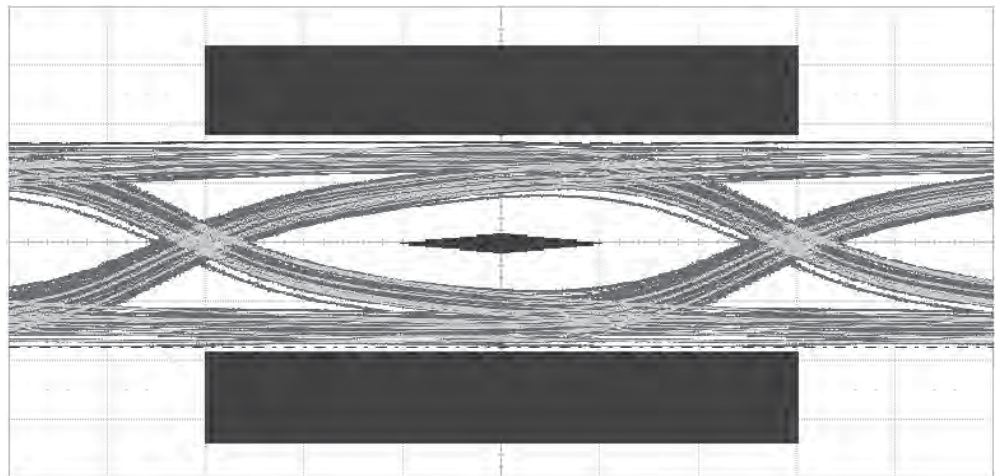
Fig 3. Crosstalk; typical values



aaa-016882

Data rate: 10 Gbit/s
Vertical scale: 325 mV/div
Horizontal scale: 16.7 ps/div

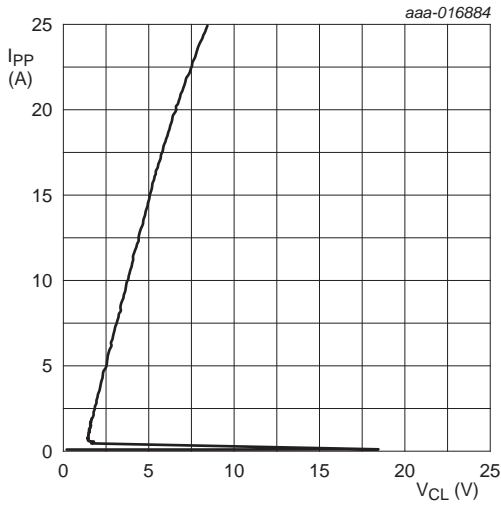
Fig 4. USB 3.1 eye diagram, Printed-Circuit Board (PCB) with PUSB3FR6



aaa-016883

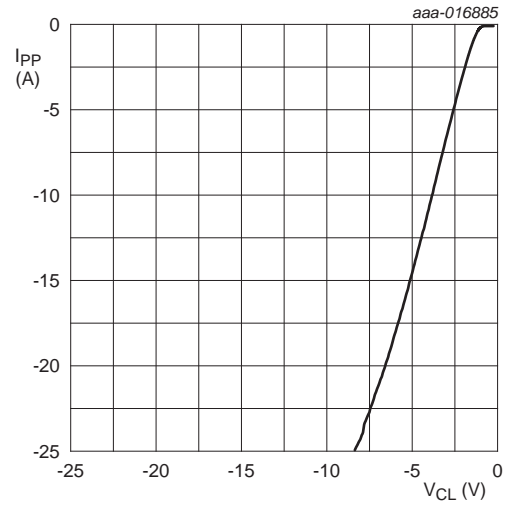
Data rate: 10 Gbit/s
Vertical scale: 325 mV/div
Horizontal scale: 16.7 ps/div

Fig 5. USB 3.1 eye diagram, PCB without PUSB3FR6 (reference)



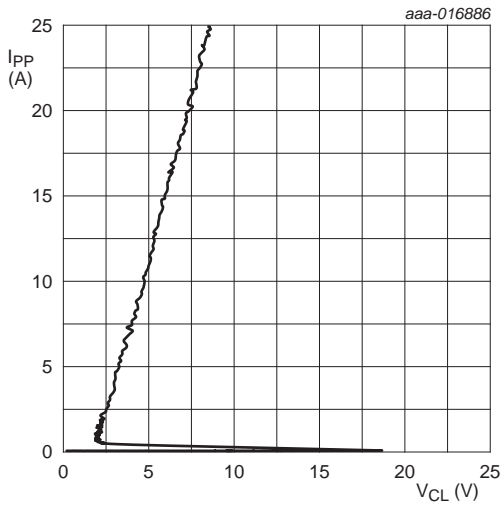
$t_p = 100$ ns; Transmission Line Pulse (TLP)

Fig 6. Dynamic resistance with positive clamping; typical values



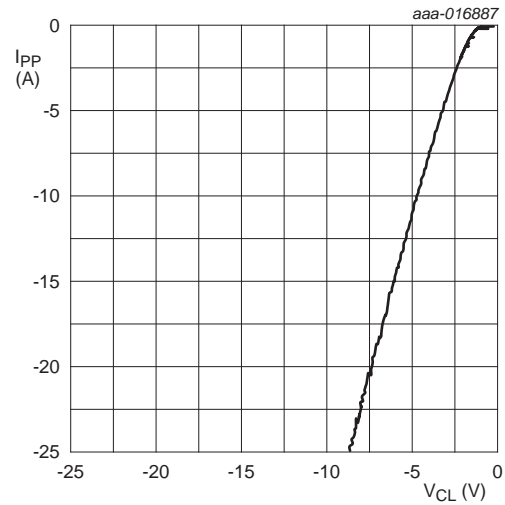
$t_p = 100$ ns; Transmission Line Pulse (TLP)

Fig 7. Dynamic resistance with negative clamping; typical values



$t_p = 5$ ns; Very-Fast TLP (VF-TLP)

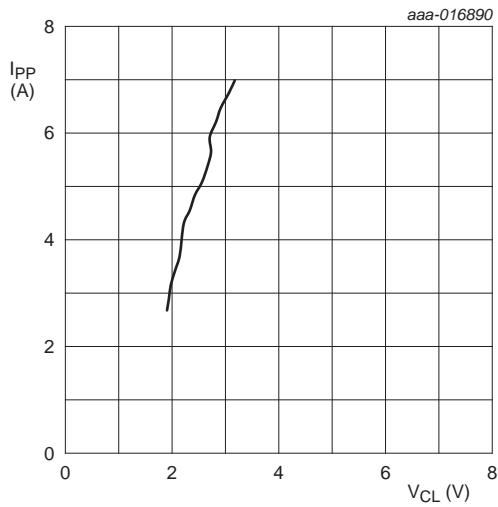
Fig 8. Dynamic resistance with positive clamping; typical values



$t_p = 5$ ns; Very-Fast TLP (VF-TLP)

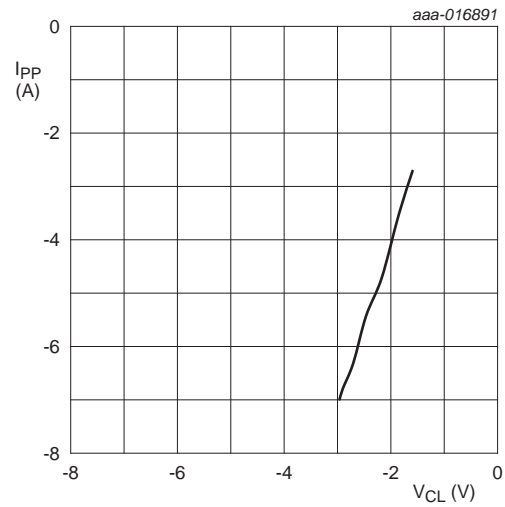
Fig 9. Dynamic resistance with negative clamping; typical values

The device uses an advanced clamping structure showing a negative dynamic resistance. This snapback behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).



IEC 61000-4-5; $t_p = 8/20 \mu s$; positive pulse

Fig 10. Dynamic resistance with positive clamping; typical values



IEC 61000-4-5; $t_p = 8/20 \mu s$; negative pulse

Fig 11. Dynamic resistance with negative clamping; typical values

7. Package outline

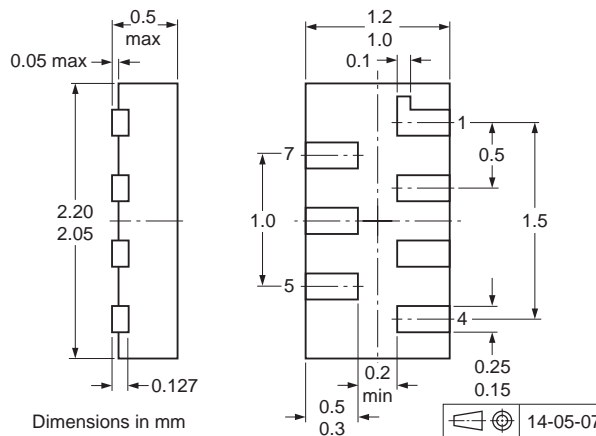


Fig 12. Package outline DFN2111-7 (SOT1358-1)

8. Soldering

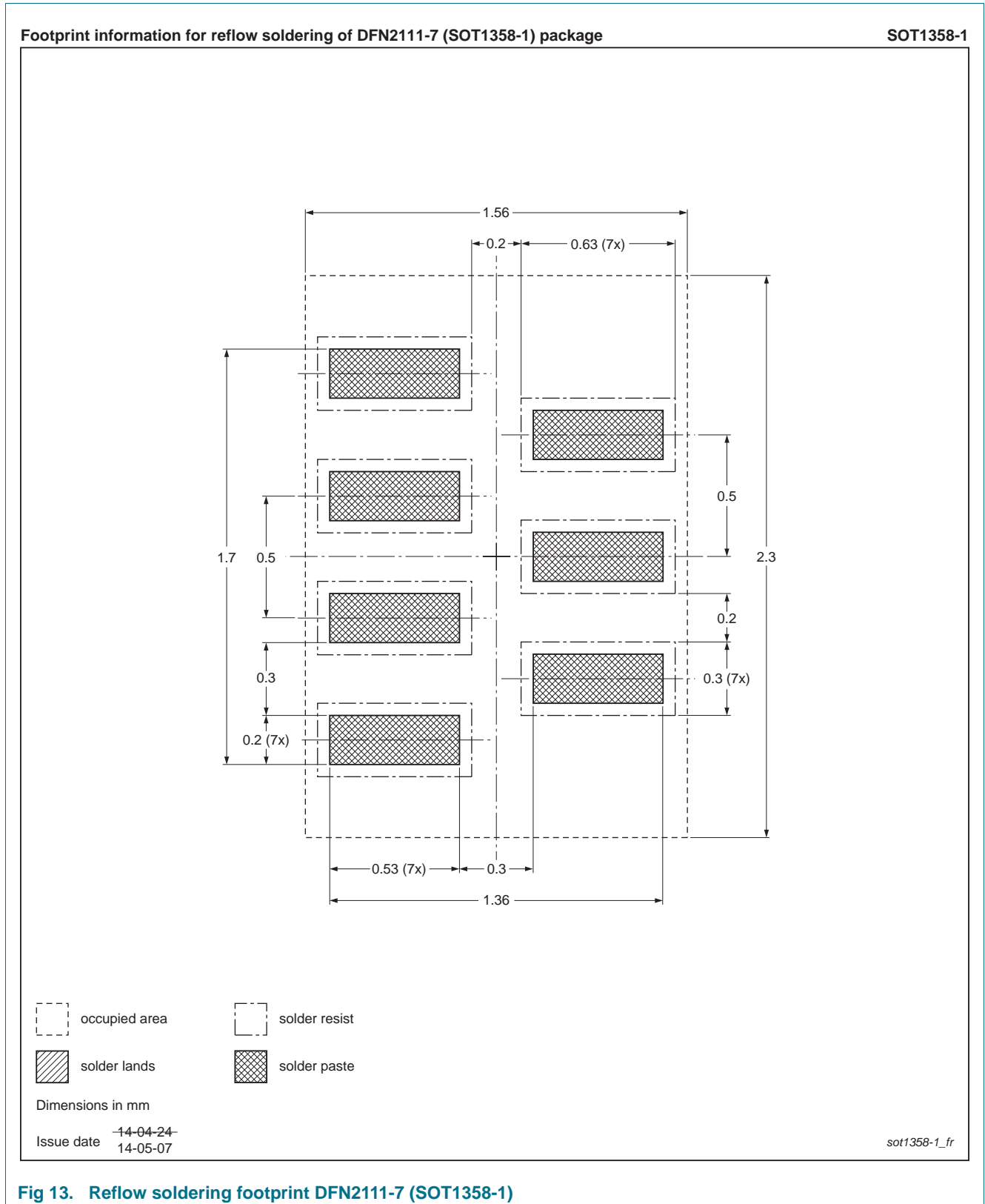


Fig 13. Reflow soldering footprint DFN2111-7 (SOT1358-1)

9. Revision history

Table 6. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------|--------------|--------------------|---------------|------------|
| PUSB3FR6 v.1 | 20150225 | Product data sheet | - | - |

10. Legal information

10.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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