承認書
APPROVAL SHEET

客　戶		APPROVE DATE
CUSTOMER		

產品型號 TYPE NO.	電路功能 CIRCUIT FUNCTION
PVG120602EGE	128 × 64 DOTS MATRIX LCD MODULE TYPE : STN LCD DUTY RATIO : 1/ 64 DOT COLOR /BACKGROUND COLOR DARK BLUE / GRAY
REMARKS :	

ORG BY:	CONCURRED:	APPROVED:	QC:
FINAL APPROVE BY CUSTOMER :			

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NO. 12, LANE 468, SEC. 2,
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HSIN-CHU TAIWAN, R.O.C.

GRAPHIC TYPE LCD MODULE

PRODUCT SPECIFICATION

PVG120602EGE

NOTICE

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE IN THE INTEREST OF PRODUCT IMPROVEMENT.

如 上 述 規 格 因 改 良 產 品 而 有 變 更, 恕 不 另 行 通 知.

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1.0 INTRODUCTION

THIS USER'S MANUAL IS INTRODUCED THE OUTSIDE DIMENSIONS, OPTICAL CHARACTERISTICS, ELECTRICAL CHARACTERISTICS, INTERFACE SPECIFICATIONS, INSTRUCTIONS, ETC. OF THE STANDARD PRODUCT.

PICVUE'S DOT MATRIX LCD MODULES, CONSIST OF A NEWLY DEVELOPED STN/FSTN TYPE LIQUID CRYSTAL DISPLAY WITH HIGH CONTRAST AND WIDE VIEWING ANGLE, CMOS LCD DRIVER (AND CONTROLLER). THE COMBINATION OF LCD AND SEMICONDUCTOR TECHNOLOGY FEATURES HIGH RELIABILITY AND LOW POWER CONSUMPTION.

1.1 FEATURE

(1) COMPACT, INTEGRATED DISPLAY MODULE.
(2) HIGH CONTRAST & CLEAR DISPLAY WITH FSTN LCD MODULE.
(3) LOW VOLTAGE.
(4) WIDE OPERATING TEMPERATURE RANGE.
(5) BUILT-IN EL BACK LIGHT.

2.0 CLASSIFICATION OF MODULE

PV G 1206 02 E G E

BACKLIGHT —
N : NO BACKLIGHT (REFLECTIVE)
E : EL BACKLIGHT
L : LED BACKLIGHT
C : CCFL BACKLIGHT

BACKGROUND COLOR —
T : TN TYPE LCD
W : (FSTN) BLACK & WHITE
G : (STN) GRAY
Y : (STN) YELLOW
B : (STN) BLUE
C : COLOR

VERSION NO (A TO O : SMT ; P TO Z : COB
1 TO 9 : TAB)

DEVELOPING SEQUENCE NO.

CHARACTER LINE OR ROW DOTS AND COLUMN DOTS

S : SEGMENT TYPE
C : CHARACTER TYPE
G : GRAPHIC TYPE

SYMBOL OF PICVUE'S STANDARD LCD MODULE

PICVUE			
LCM NO: PVG120602EGE	REF.NO:	REV.:	/

3.0 MECHANICAL SPECIFICATIONS

ITEM	NORMINAL DIMENSIONS	UNIT
NUMBER OF DOTS	128 (W) × 64 (H)	DOTS
MODULE DIMENSION	93.0 (W) × 70.0 (H) × 8.5 (D)	mm
EFFECTIVE DISPLAY AREA	70.7 (W) × 38.8 (H)	mm
DOT SIZE	0.48 (W) × 0.48 (H)	mm
DOT PITCH	0.52 (W) × 0.52 (H)	mm
DUTY	1/64	
LCD	GRAY	
VIEWING DIRECTION	6 O'CLOCK	
BACK LIGHT	COOL WHITE (EL)	

4.0 MAX RATING ABSOLUTE

ITEM	SYMBOL	MIN.	MAX.	UNIT
OPERATING TEMPERATURE	Top	0	+50	℃
STORAGE TEMPERATURE	Tst	-20	+60	℃
SUPPLY VOLTAGE FOR LOGIC	VDD-VSS	0	6.0	V
SUPPLY VOLTAGE FOR LCD	VDD-VO	0	19.0	V
INPUT VOLTAGE	Vi	VSS	VDD	V
STATIC ELECTRICITY	BE SURE THAT USER ARE GROUNDED WHEN HANDING LCM			

5.0 ELECTRICAL CHARACTERISTICS :

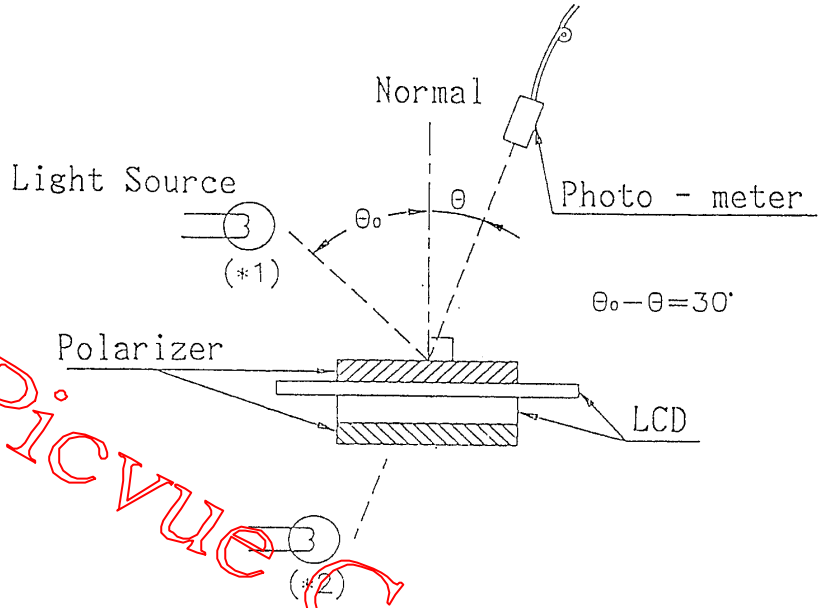
ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SUPPLY VOLTAGE FOR LOGIC	VDD-VSS	———	4.75	5.0	5.25	V
INPUT VOLTAGE	VI	H LEVEL	0.8VDD	——	VDD	V
		L LEVEL	0	——	0.2VDD	V
POWER SUPPLY FOR LCM	IDD	VCC = 5V FR = 70Hz	——	3.6	——	mA
FRAME FREQUENCY	FR	——	——	70	85	Hz

6.0 OPTICAL CHARACTERISTICS :

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
VIEW ANGLE (H)	θX	CR≧2.0	-25	——	25	DEG
VIEW ANGLE (V)	θY		-30	——	30	DEG
CONTRAST RATIO	CR	θX = 0° θY = 0°	——	6	—	—
RESPONSE TIME (RISE)	TON		——	130	230	ms
RESPONSE TIME (FALL)	TOFF		——	150	250	ms

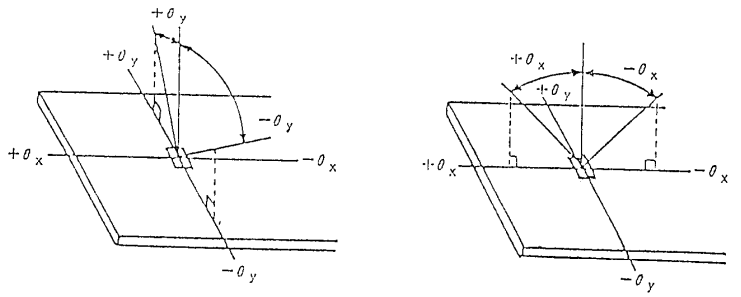
6-1 OPTICAL MEASUREMENT SYSTEM :

MEASURING INSTRUMENTS FOR ELECTRO-OPTICAL CHARACTERISTICS



* 1 : LIGHT SOURCE POSITION FOR MEASURING OF REFLECTIVE TYPE LCD
* 2 : LIGHT SOURCE POSITION FOR MEASURING OF TRANSPARENT/TRANSFLECTIVE TYPE LCD

6-2 DEFINITION OF θx AND θy :



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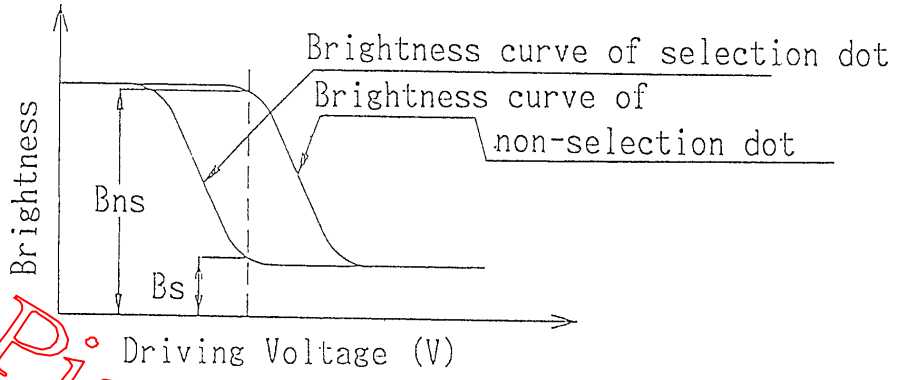
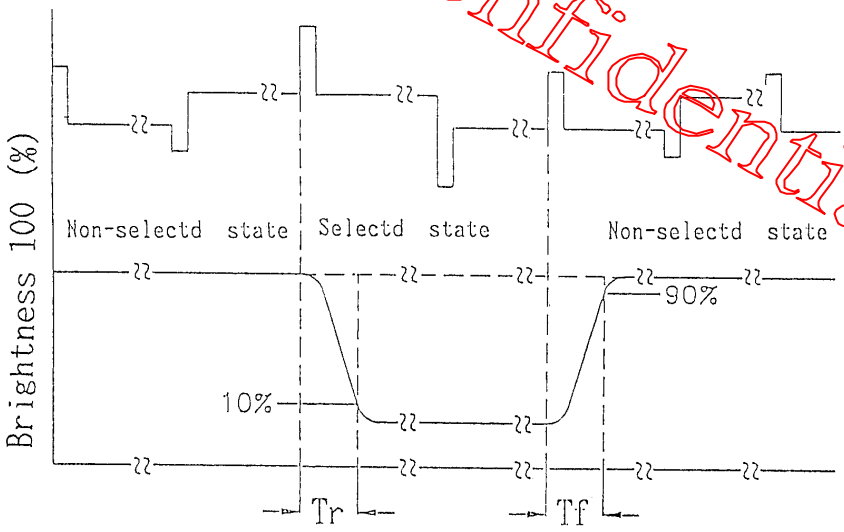
6-3 DEFINITION OF CONTRAST RATIO CR :

$$CR = \frac{\text{Bringhtness of non-selected segment(B2)}}{\text{Bringhtness of selected segment(B1)}}$$



6-4 DEFINITION OF OPTICAL RESPONSE TIME :



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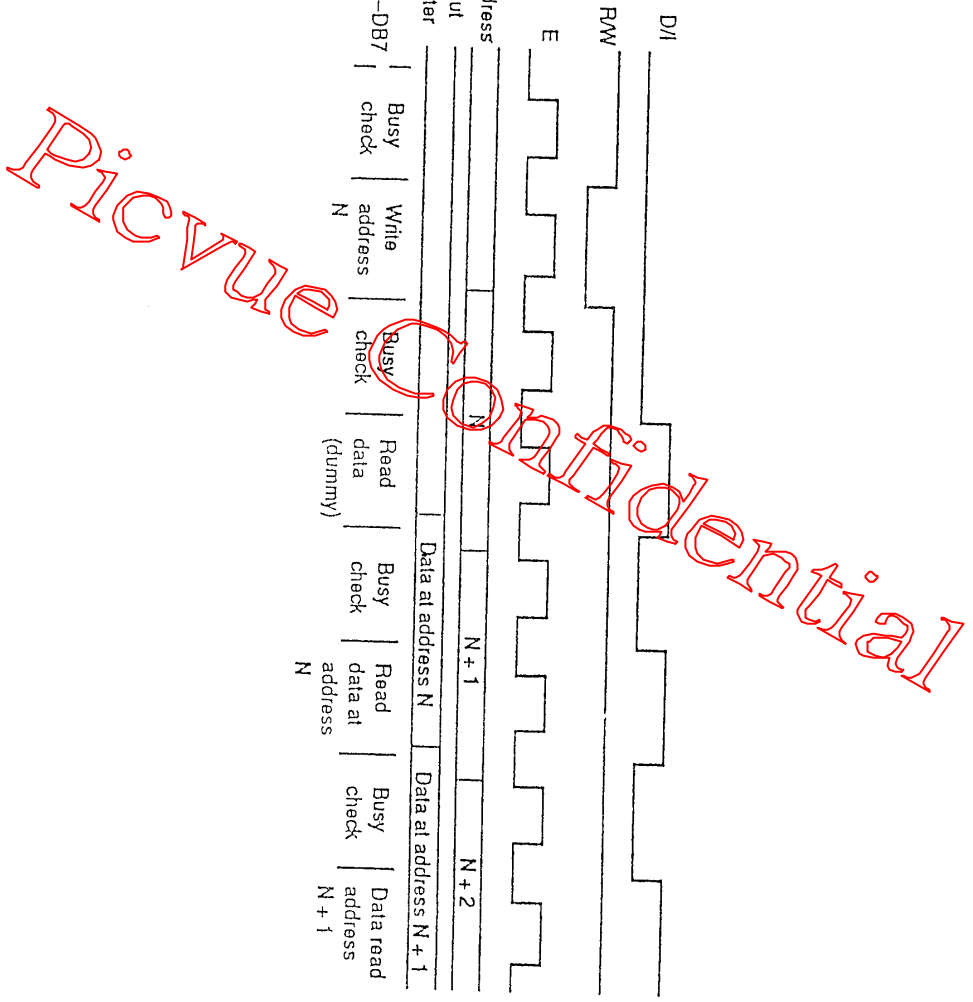
LCM NO	PVG120602EGE	REF.NO:	REV	/

7. INTERFACE TIMING CHART :

7-1. TIMING CHART :



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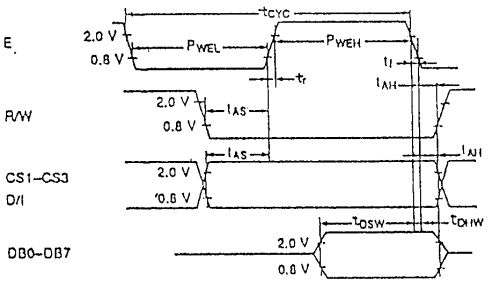
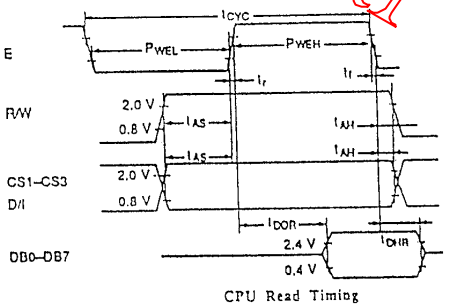
LCM NO	PVG120602EGE	REF.NO:	REV /

7-2 TIMING CHARACTERISTICS :

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
E cycle time	tCYC	1000	—	—	nS
E high level width	pWEH	450	—	—	nS
E low level width	pWEL	450	—	—	nS
E rise time	tr	—	—	25	nS
E fall time	tf	—	—	25	nS
Address set-up time	tAS	140	—	—	nS
Address hold time	tAH	10	—	—	nS
Data set-up time	tDSW	200	—	—	nS
Data delay time	tDDR	—	—	320	nS
Data hold time(Write)	tDHW	10	—	—	nS
Data hold time(Read)	tDHR	20	—	—	—



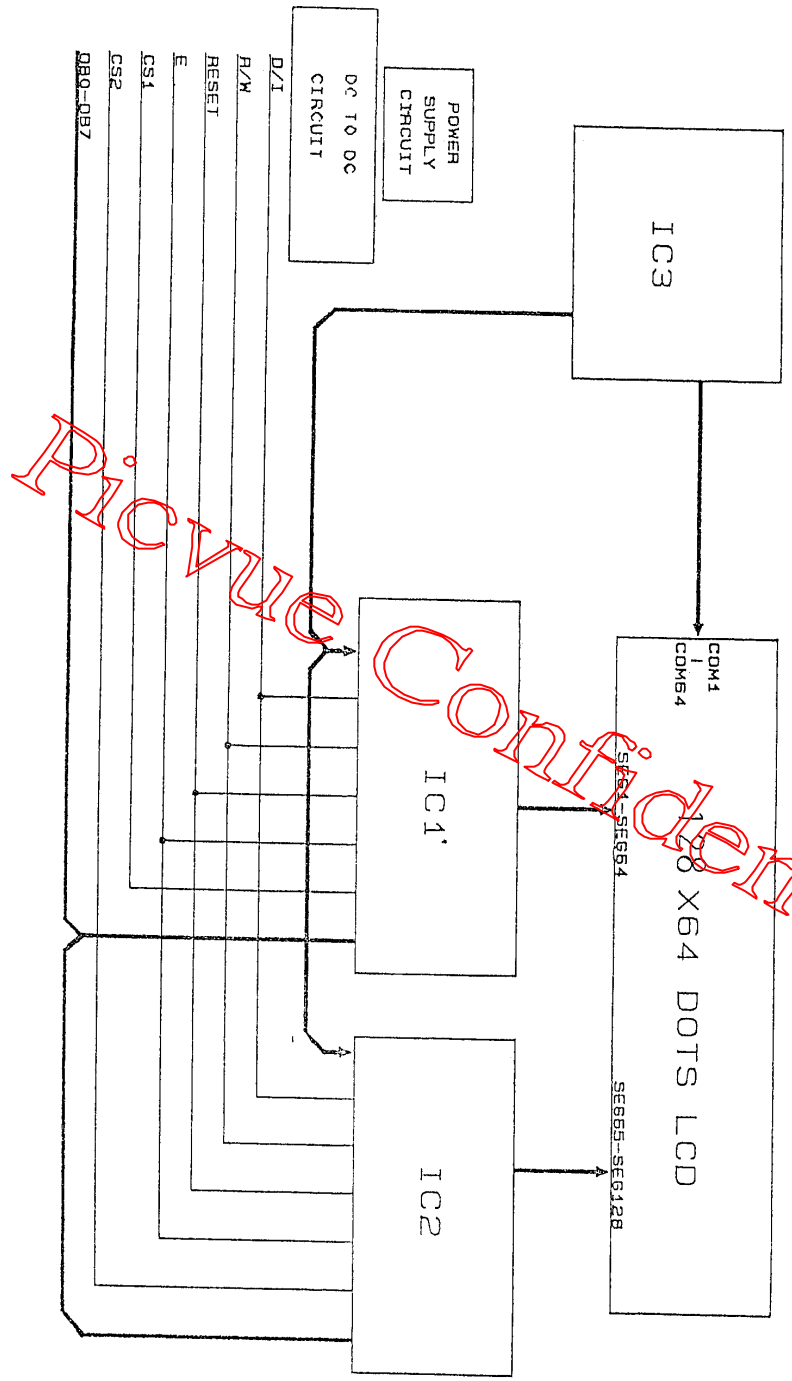
CPU Write Timing



CPU Read Timing

PICVUE	PICVUE ELECTRONICS CO.,LTD.		
LCM NO: PVG120602EGE	REF.NO:	REV :	/

8. BLOCK DIAGRAM :



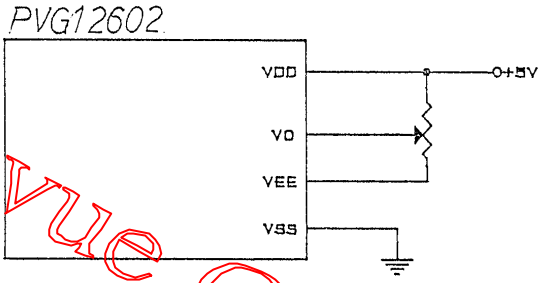
PICVUE	PICVUE ELECTRONICS CO.,LTD.		
LCM NO: PVG120602EGE	REF.NO:	REV. :	/

9. I/O TERMINAL

9.1 INTERFACE PIN CONNECTIONS

PIN NO	SYMBOL	LEVEL	FUNCTIONS
1	VSS	—	GROUND.
2	VDD	—	POWER SUPPLY FOR LOGIC CIRCUIT
3	VO	—	OPERATING VOLTAGE FOR LCD DRINING
4	D/I	H/L	H:DATA INPUT L:INSTRUCTION CODE INPUT
5	R/W	H/L	H:DATA READ L:DATA WRITE
6	E	H,H->L	ENABLE
7-14	DB0-DB7	H/L	DATA BUS LINE
15	CS1	H	CHIP SELECT FOR IC1
16	CS2	H	CHIP SELECT FOR IC2
17	RST	L	RESET
18	VEE	—	POWER SUPPLY FOR LCD DRIVING
19	EL1	—	POWER SUPPLY FOR EL DRIVING
20	EL2	—	POWER SUPPLY FOR EL DRIVING

9-2. POWER SUPPLY CIRCUIT DIAGRAM



PICVUE	PICVUE ELECTRONICS CO.,LTD.		
LCM NO PVG120602EGE	REF.NO:	REV. :	/

10. APPLICATION OF LCD MODULE

10-1. INTERFACE BETWEEN LCM AND MPU

1. Example of connection with HD6800

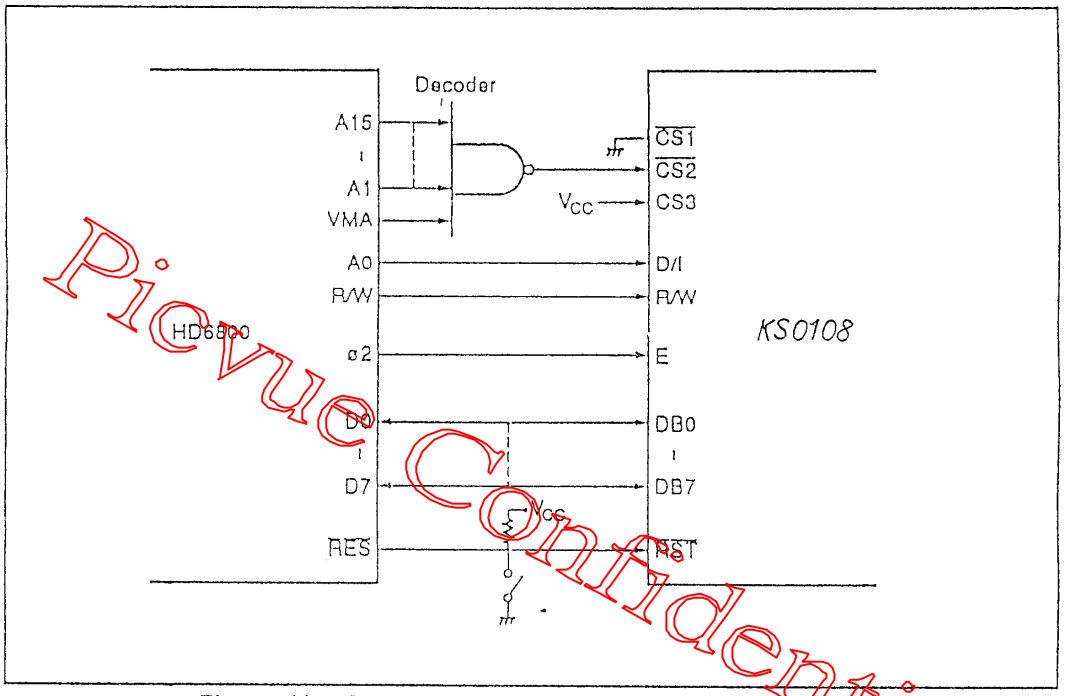


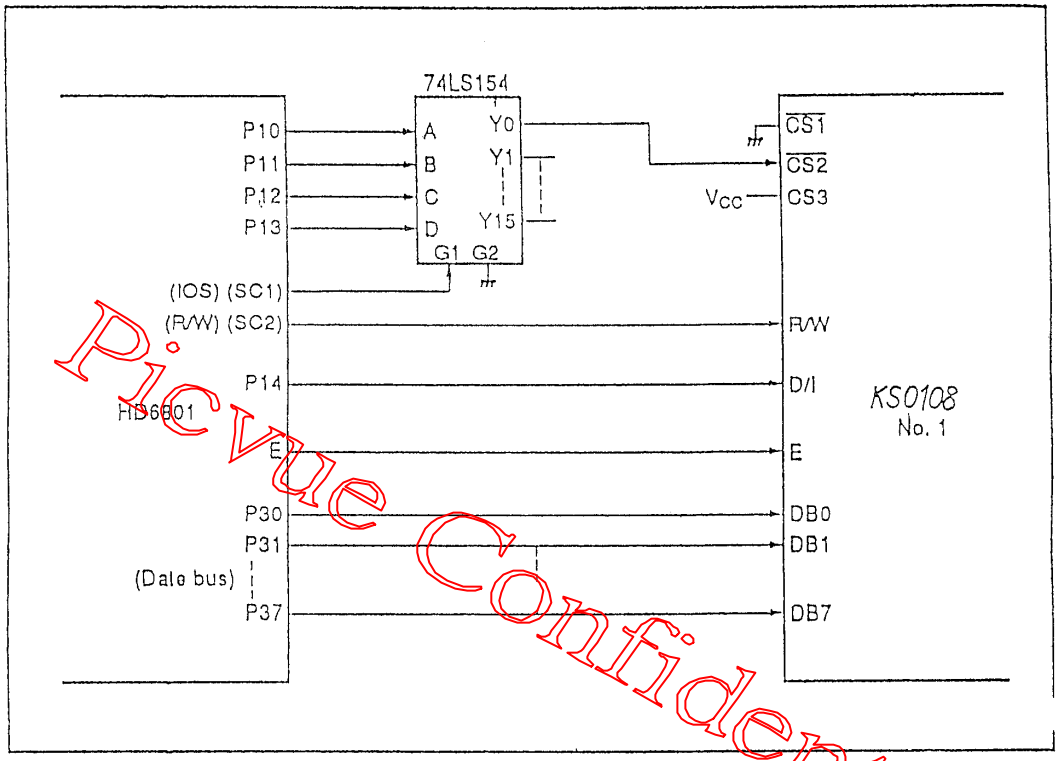
Figure 11 Example of Connection with HD6800 Series

In this decoder, addresses of KS0108 in the address area of HD6800 are:

Read/write of the display data	$FFFF
write of display instruction	$FFFE
Read out of status	$FFFE

Therefore, you can control KS0108 by reading/writing the data at these addresses.

2. Example of connection with HD6801



Set HD6801 to mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus.
74LS154 4-to-16 decoder generates chip select signal to make specified KS0108 active after decoding 4 bits of P10 to P13.

Therefore, after enabling the operation by P10 to P13 and specifying D/I signal by P14, read/write from/to the external memory area ($0100 to $01FE) to control KS0108. In this case, IOS signal is output from SC1 and R/W signal from SC2.
For details of HD6800 and HD6801, refer to their manuals.

10-2. CONTROL INSTRUCTION

Function of Each Block

Interface Control

1. I/O buffer

Data is transferred through 8 data bus lines (DB0–DB7).

DB7: MSB (Most significant bit)

DB0: LSB (Least significant bit)

Data can neither be input nor output unless $\overline{CS1}$ to CS3 are in the active mode. Therefore, when $\overline{CS1}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{RST}$ and ADC; that is namely, the internal state is maintained and no instruction excutes. Besides, pay attention to $\overline{RST}$ and ADC which operate irrespectively of $\overline{CS1}$ to CS3.

2. Register

Both input register and output register are provided to interface to an MPU whose speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals (table 1).

a. Input register

The input register is used to store data temporarily before writing it into display data RAM.

The data from MPU is written into the input register, then into display data RAM automatically by internal operation. When $\overline{CS1}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in table 1, data is latched at the fall of the E signal.

b. Output register

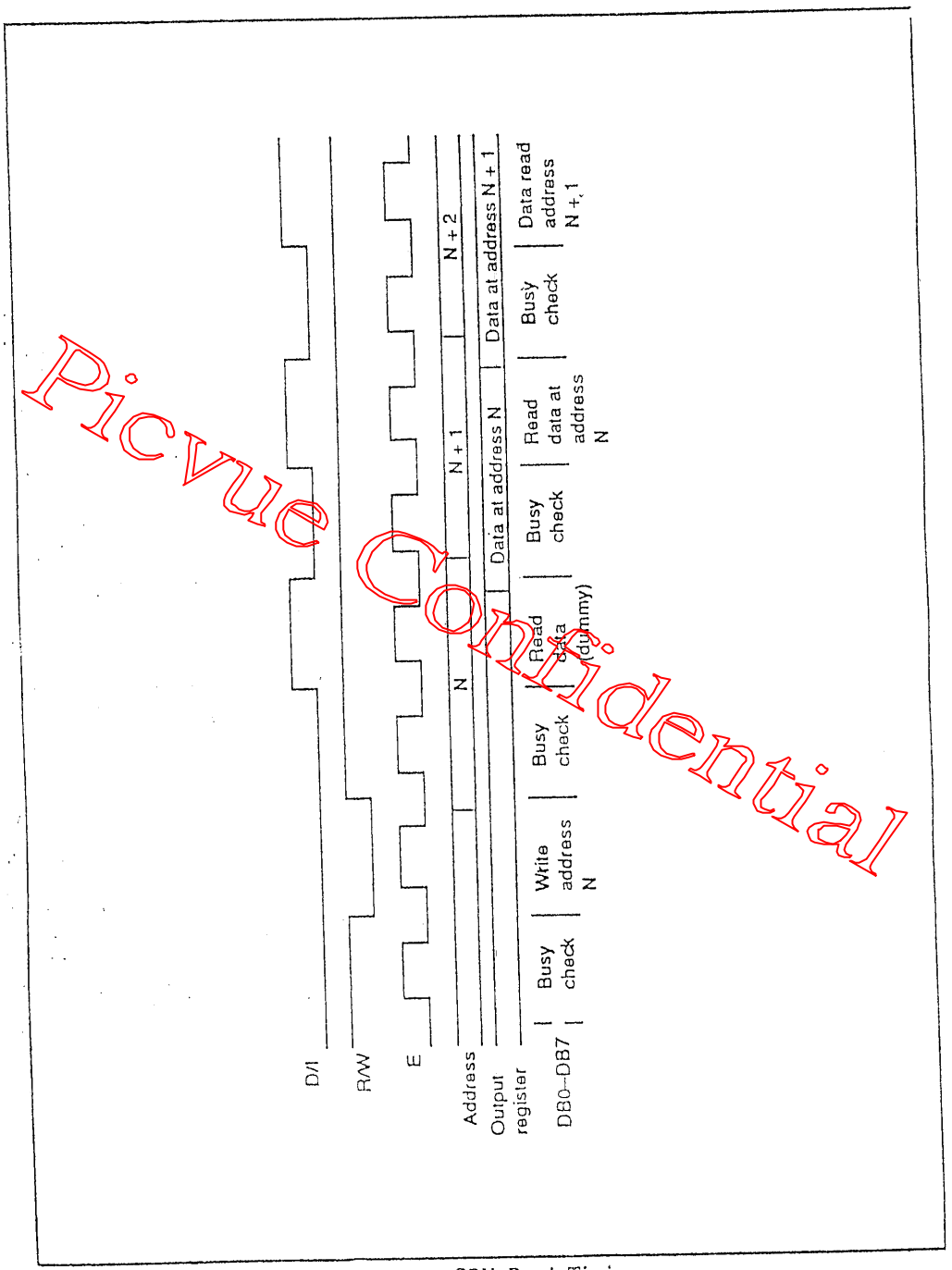
The output register is used to store data temporarily that is read from display data RAM. To read out the data from output register, $\overline{CS1}$ to CS3 should be in the active mode and both D/I and R/W should be 1. With the read display data instruction, data stored in the output register is output while E is high level. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1.

The contents in the output register are rewritten by the read display data instruction, but are held by address set instruction, etc.

Therefore, the data of the specified address cannot be output with the read display data instruction right after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Figure 5 shows the CPU read timing.

Table 1 Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register)
1	0	Writes data into input register as internal operation (input register → display data RAM)
0	1	Busy check. Read of status data.
0	0	Instruction



CPU Read Timing

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LCM NO: PVG120602EGE	REF.NO:	REV. :	/

Busy Flag

Busy flag = 1 indicates that KS0108 is operating and no instructions except status read instruction can be accepted. The value of the busy flag is read out on DB7 by the status read instruction. Make sure that the busy flag is reset (0) before issuing instructions.

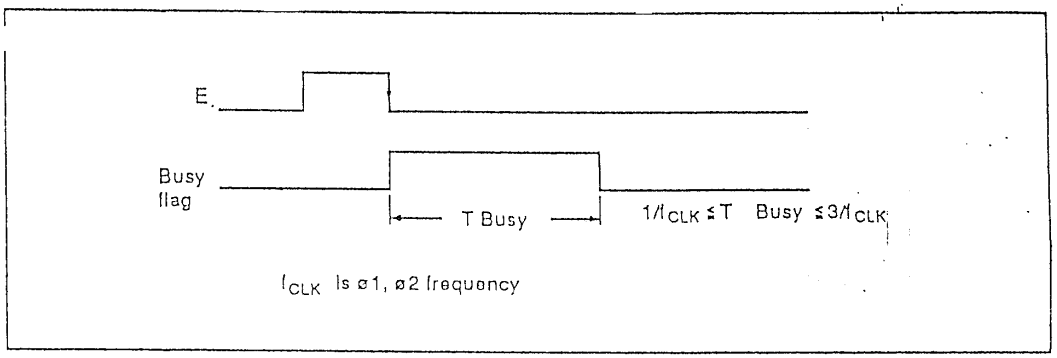

Figure 6 Busy Flag

Display On/Off Flip/Flop

The display on/off flip/flop selects one of two states, on state and off state of segments Y1 to Y64. In on state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in off state independent of the data in RAM. It is controlled by display on/off instruction. $\overline{RST}$ signal = 0 sets the segments in off state. The status of the flip/flop is output to DB5 by status read instruction. Display on/off instruction does not influence data in RAM. To control display data latch by this flip/flop, CL signal (display synchronous signal) should be input correctly.

Display Start Line Register

The display start line register specifies the line in RAM which corresponds to the top line of LCD panel when displaying contents in display data RAM on the LCD panel. It is used for scrolling of the screen.

6-bit display start line information is written into this register by the display start line set instruction. When high level of the FRM signal starts the display, the information in this register is transferred to the Z address counter, which controls the display address, presetting the Z address counter.

X, Y Address Counter

A 9-bit counter which designates addresses of the internal display data RAM. X address counter (upper 3 bits) and Y address counter (lower 6 bits) should be set to each address by the respective instructions.

1. X address counter
Ordinary register with no count functions. An address is set by instruction.

2. Y address counter
An address is set by instruction and is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Stores dot data for display. 1-bit data of this RAM corresponds to light on (data = 1) and light off (data = 0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment pins can be reversed by ADC signal.

As the ADC signal controls the Y address counter, reversing of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, never fail to connect ADC pin to V_{CC} or GND when using.

Figure 7 shows the relations between Y address of RAM and segment pins in the cases of ADC = 1 and ADC = 0 (display start line = 0, 1/64 duty cycle).

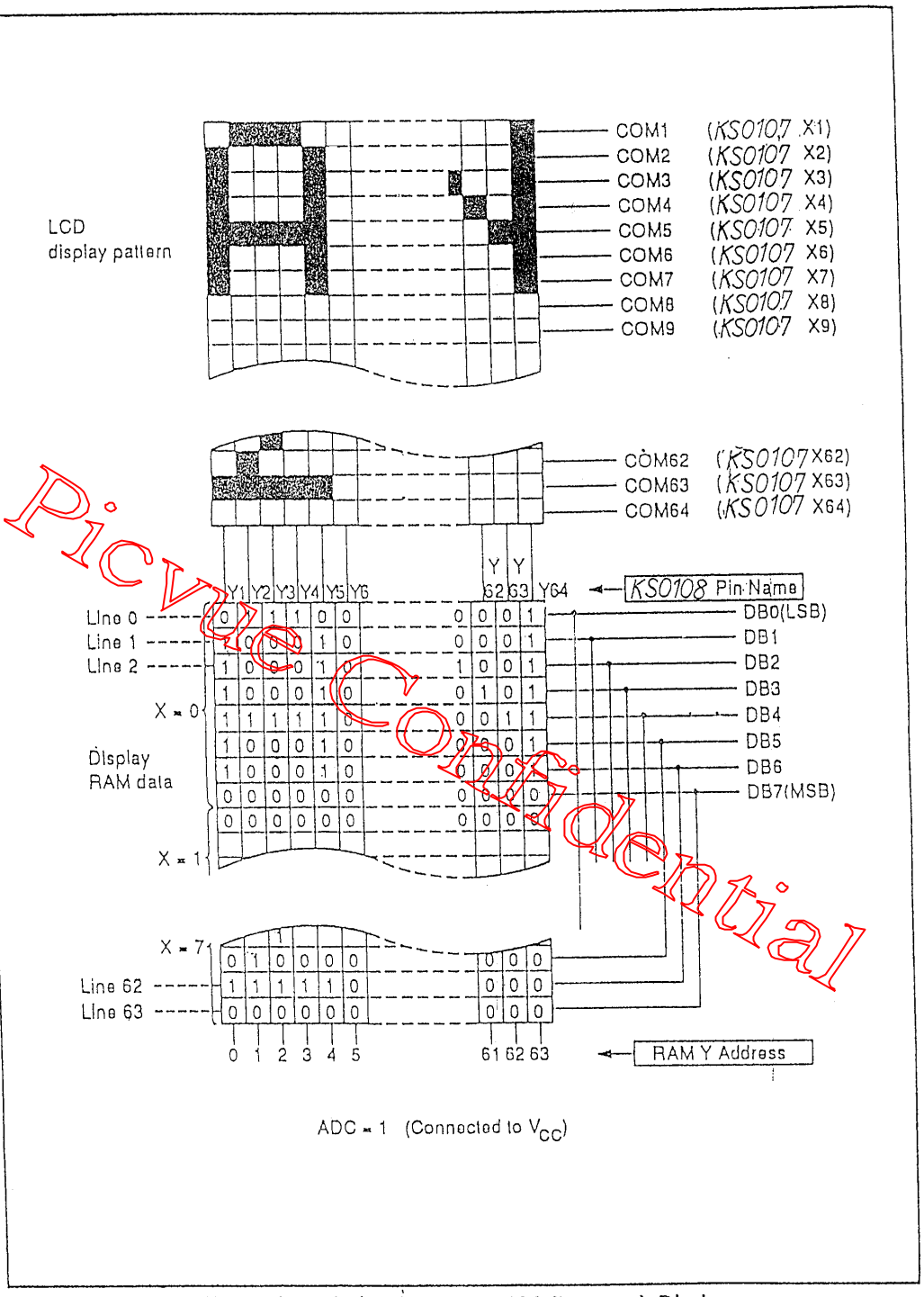

Figure 7 Relation between RAM Data and Display

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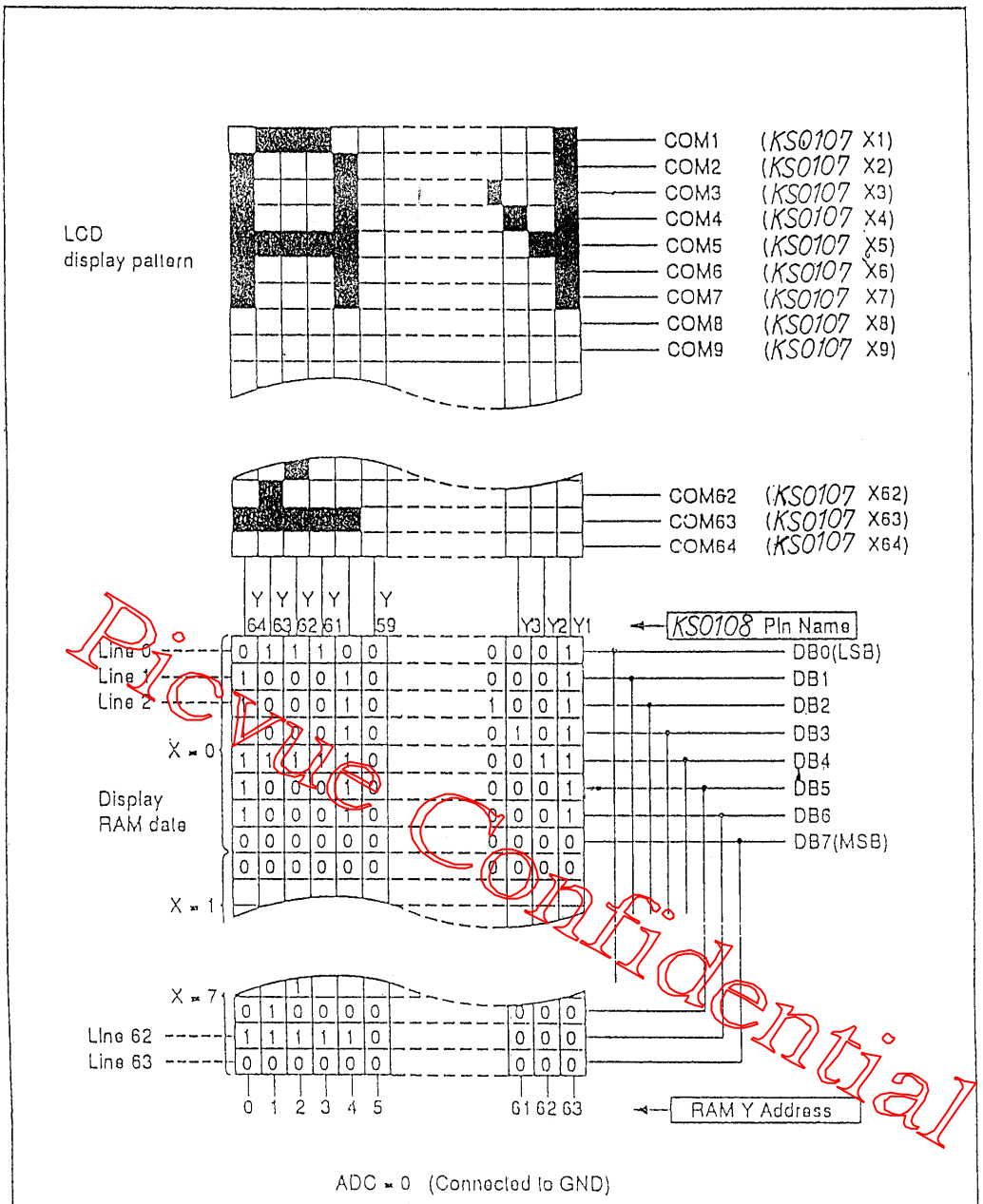


Figure 7 Relation between RAM Data and Display (cont)

PICVUE	PICVUE ELECTRONICS CO.,LTD.		
LCM NO : PVG120602EGE	REF.NO :	REV. :	/

Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6 bits and counts up at the fall of the CL signal. At the high level of FRM, the contents of the display start line register is preset at the Z counter.

Display Data Latch

The display data latch stores the display data temporarily that is output from display data RAM to the liquid crystal driving circuit. Data is latched at the rise of the CL signal. The display on/off instruction controls the data in this latch and does not influence data in display data RAM.

Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

Reset

The system can be initialized by setting $\overline{RST}$ terminal at low level when turning power on.

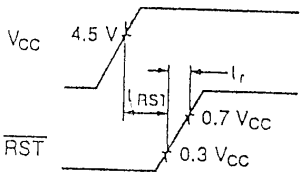
1. Display off
2. Set display start line register line 0.

While $\overline{RST}$ is low level, no instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4 = 0 (clear RESET) and DB7 = 0 (Ready) by status read instruction. The conditions of power supply at initial power up are shown in table 1.

Table 1 Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	—	—	μs
Rise time	t_r	—	—	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the registers except on/off register and in RAM.



Display Control Instructions

Outline

Table 2 shows the instructions. Read/write (R/W) signal, data/instruction (D/I) signal, and data bus signals (DB0 to DB7) are also called instructions because the internal operation depends on the signals from the MPU.
These explanations are detailed in the following pages. Generally, there are following three kinds of instructions:

1. Instruction to set addresses in the internal RAM
2. Instruction to transfer data from/to the internal RAM
3. Other instructions

In general use, the second type of instruction is used most frequently. Since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be shortened. During the execution of an instruction, the system cannot accept instructions other than status read instruction. Send instructions from MPU after making sure that the busy flag is 0, which is proof that an instruction is not being excuted.

Table 2 Instructions

Instructions	Code R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Functions
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected. 1: on, 0: off.
Display start line	0	0	1	1	Display start line (0–63)						Specifies the RAM line displayed at the top of the screen.
Set page (X address)	0	0	1	0	1	1	1	Page (0–7)			Sets the page (X address) of RAM at the page (X address) register
Set address	0	0	0	1	Y address (0–63)						Sets the Y address in the Y address counter.
Status read	1	0	Busy	0	ON/OFF	Reset	0	0	0	0	Reads the status. RESET 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Internal operation 0: Ready
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM. Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.

Note: 1 Busy time varies with the frequency (f_{CLK}) of $\phi 1$, and $\phi 2$.
($1/f_{CLK} \leq T_{BUSY} \leq 3/f_{CLK}$)

Detailed Explanation

Display on/off

	R/W	D/I	DB7						DB0
Code	0	0	0	0	1	1	1	1	1	D

← high-order bit low-order bit →

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

Display start line

	R/W	D/I	DB7						DB0
Code	0	0	1	1	A	A	A	A	A	A

← high-order bit low-order bit →

Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen. Figure 8 shows examples of display (1/64 duty cycle) when the start line = 0-3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

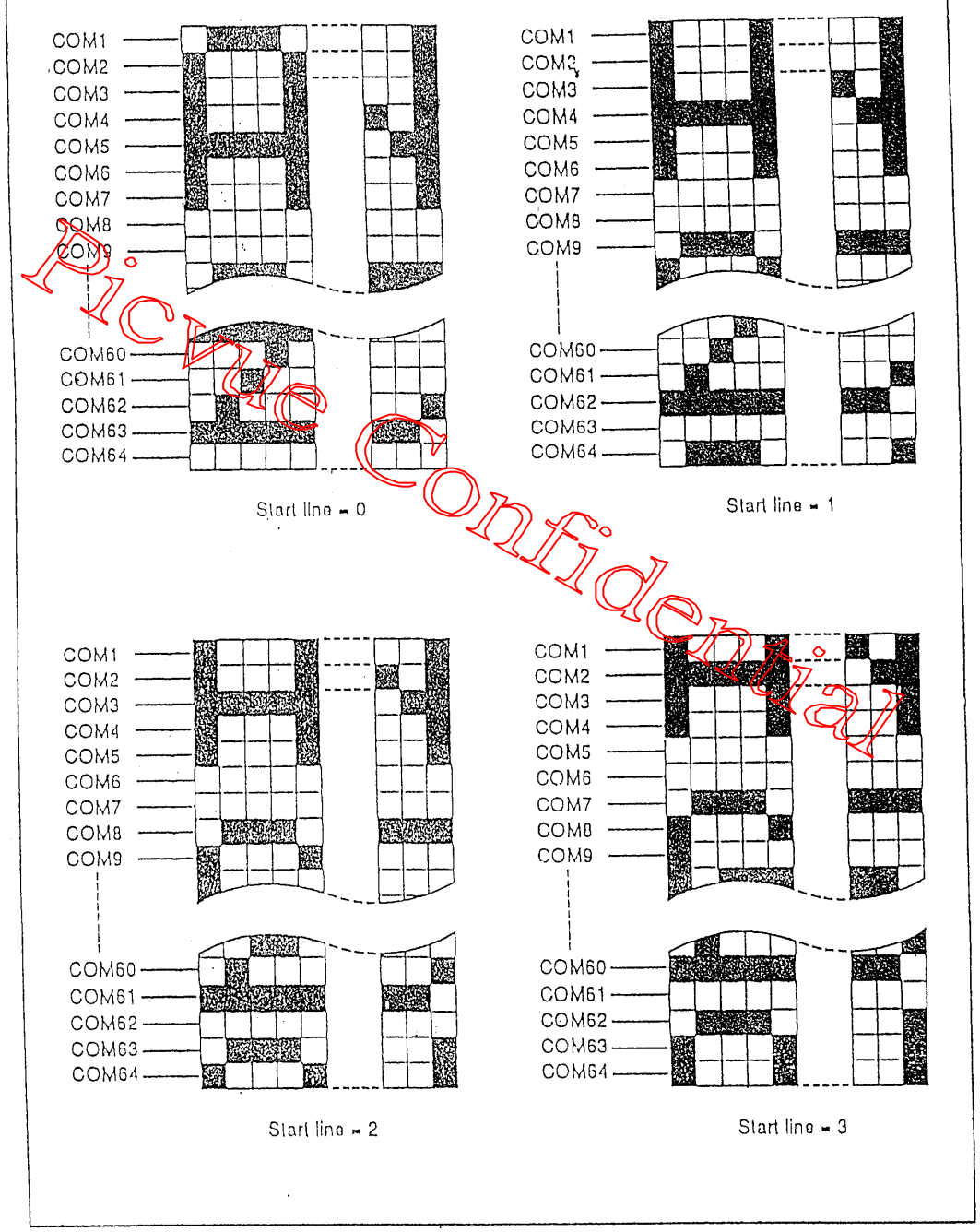


Figure 8 Relation Between Start Line and Display

Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A

← high-order bit low-order bit →

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See figure 9.

Set Y address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← high-order bit low-order bit →

Y address AAAAAA (binary) of the display data RAM is set in the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

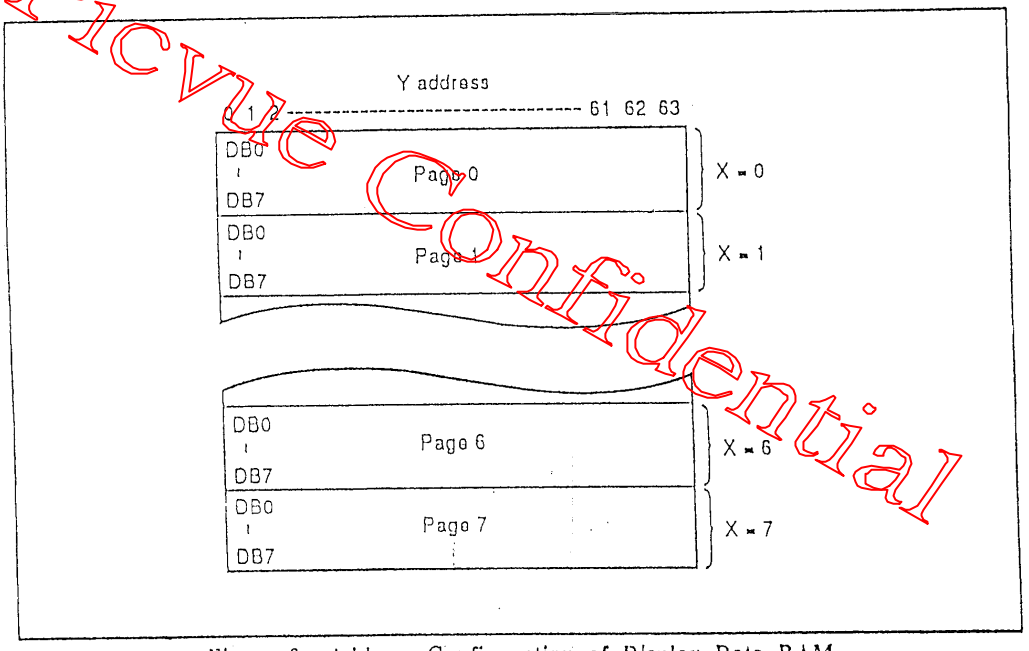
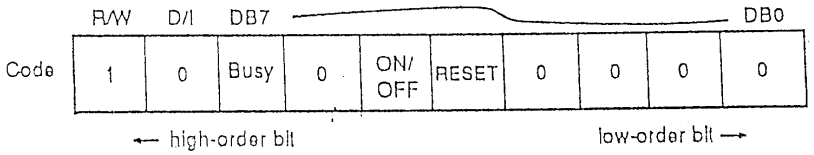


Figure 9 Address Configuration of Display Data RAM

Status Read

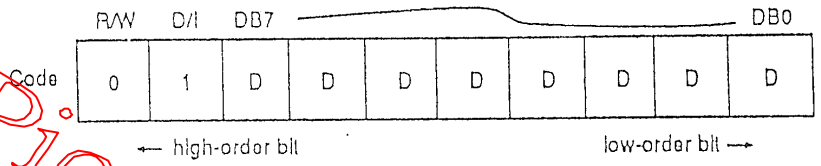


Busy: When Busy is 1, the LSI is executing internal operations. No instructions are accepted while Busy is 1, so you should make sure that Busy is 0 before writing the next instruction.

ON/OFF: Shows the liquid crystal display conditions: on condition or off condition.
When ON/OFF is 1, the display is in off condition.
When ON/OFF is 0, the display is in on condition.

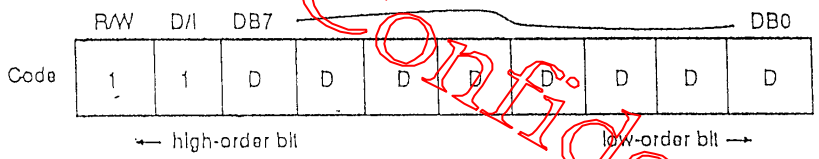
RESET RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.
RESET = 0 shows that initializing has finished and the system is in the usual operation condition.

Write Display Data



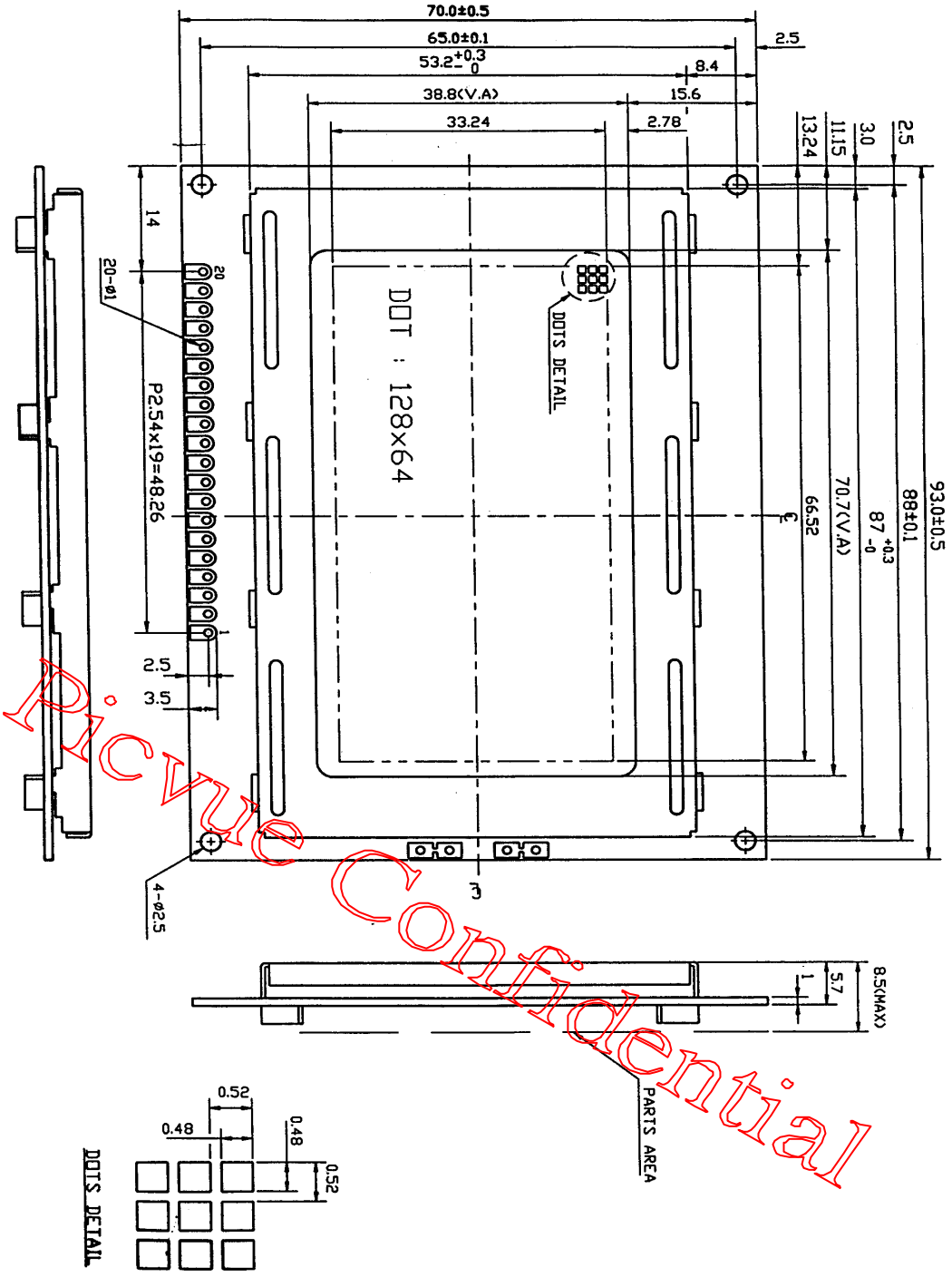
Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically

Read Display Data



Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.
One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in "FUNCTION OF EACH BLOCK".

11. DIMENTION OUTLINE :



PICVUE	PICVUE ELECTRONICS CO.,LTD.		
LCM NO : PVG120602EGE	REF.NO :	REV. :	/

12.1 HANDLING OF LCD

1. The surface is easy to get scratched !!
   The surface of LCD glass is covered with palarizer (organic film). This surface is quite soft and so should avoid rubbing with hard material for keeping it not get scratched.

2. Away from water !!
   LCD must not be used with drop of water adhered on it in order to keep electrodes from corrosion. Wipe the droplets off and use it dry.

3. Keep off dirty !!
   Saliva, fingerprint, starch or oily materials are easy to adhere on LCD surface . On case this happened , wipe it off using soft cloth slightly wetted with normalhexane. Better keep LCD away from other organic solvents.

4. High temperature and high humidity will cause LCD'S easy deterioration !!
   LCD dislike high terperature and high humidity. Store and use them under the condition where the temperature and humidity are kept in specified range.

12.2 User notes for pin-type LCD

1. Keep off high terperature and high stress !!
   High stress or high terperature will cause poor pin connection. Install LCD 2mm or more apart from PCB .Making the pin at both ends both sides dummy will help stress release.
   The connector pin installation area must be designed to the temperature not to exceed 80℃ when using.

2. Do not clean whole LCD parte after PCB soldering !!
This will cause washing solution (fleon , or trichloroethane) to penetrate into resin of pin , decomposes resin under sunlight producing chlorine and combines with water to produce hydrochloric acid
This acid will then desolve the electrodes , causing wire breaks.

12.3 Handling of LCM

1. Keep away from processing or modilying of metal frame fingers !!
This will often affect the consistency of C-MOS LSI signal output resulting in unusual display .

2. Take good care on CFL handling !!
When installing CFL to the unit,care must be taken not to be grasped by hand or hitted by hard material to avoid demages.

3. Do not hardly press metal frame or PCB !!
When pressure is applied to metal frame or PCB , will often give rise to distortion of conducting rubber , breakage of LCD or backlighting lamp , resulting in display failure .Therefore on installation of LCM , please use holes for fixing to keep LCM or lamp free from stress.

4. Through-hole-pad should not be peeled off !!
When repairing or soldering the connector , care must be taken not to peel off through-hole-pad. Watch closely the soldering iron temperature and soldering time duration.

5 Watch for an after image !!
When there is an object existing under the direct sunlight or fluorescent lamp above LCM unit , will often transfer the image to the LCM acting as an after image . Not put an abject above LCM to abstract the display .

6. Watch for low temperature bubbles !

Prolonged storing under the temperature even lower than specified temperature range or strong impact applied on the unit , will often give give rise to black or white bubbles appeared in the display .

12.4 Must be with human body earth when touching

Plase , must be well with human body earth at time of LCM handling Because it would become reasons why C-MOS , LSI being demolished if touch LCM without earth . It is advisable to wear conductive shoes, and operate under conductive sheet for safety.

12.5 Be using no AC current leakage welding hand.

Be sure there will have no AC current leakage for welding hand when is making use . It would probably destroyed by imvoluntarily voltage applying to LCM.

12.6 Must be with earth for electric driver

Please , must be well with earth when using electric driver for LCM installation . It had been reconized that LCM might be broken due to static electricity occurred by electric driver.

12.7 Keep the humidity of operation room above 45%

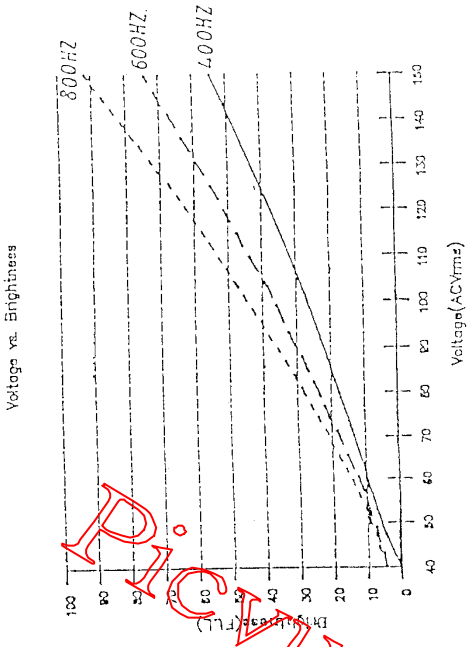
Please keep the room humidity above 45% .
Because the dryer the air , the easier static electricity will occur.
Further, please also hold attention to operation desks, chairs, shelfs push care be well with earth. Special attention have to be extended to the movement as taking LCM out or transferring from packing box.

12.8 Be attention to the use of cleaning machine

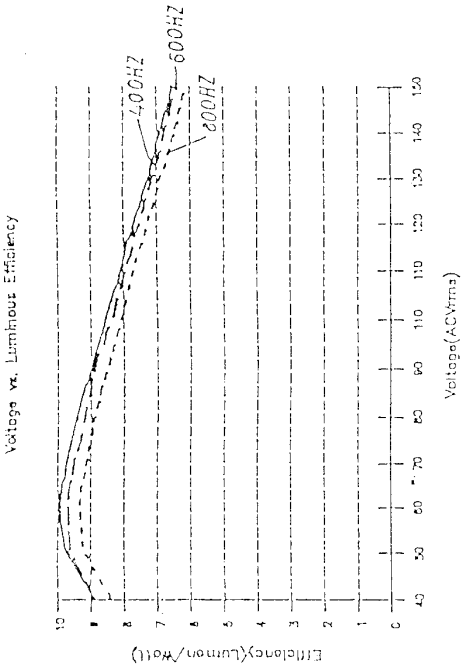
Do not get the mouth of cleaning machine near to the LCM when is cleaning the operation room by cleaning machine . It had been found sometime the LCM were demolished by static electricity.

13. EL Lamp Data

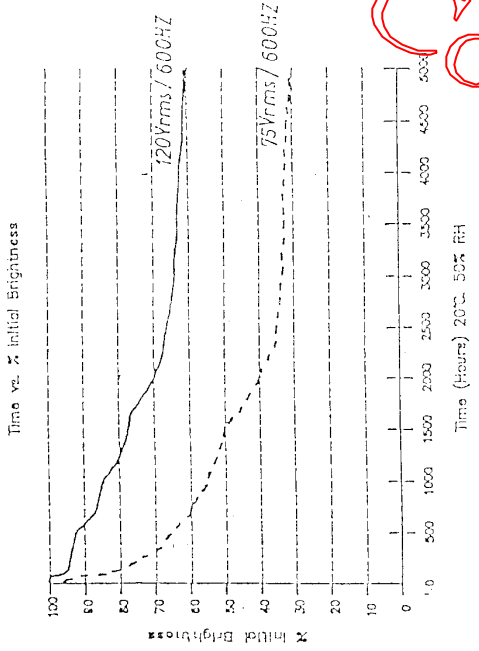
(1) Brightness:



(2) Efficiency:



(3) Initial Brightness:



(4) EL Specifications:

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Voltage	V	80	120	150	Volt rms A.C.	Without Inverter
Operation Frequency	F op	300	400	500	Hz	Without Inverter
Average luminous intensity	I v	—	120	—	cd/m²	F op=400Hz V = 120 V Without Inverter
Current Density	I d	—	1	—	mA/sq. in.	F op=400Hz V = 120 V Without Inverter
Color	Cool White					

14.0 RELIABILITY

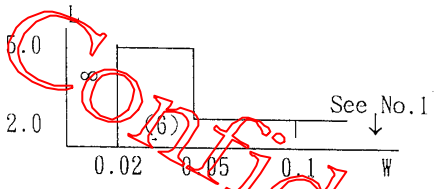
ITEM OF RELIABILITY TEST (GRAPHIC MODE)

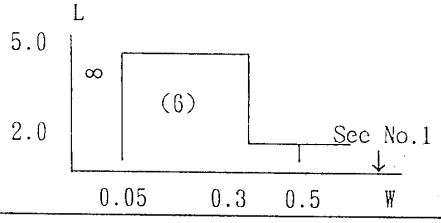
NO.	ITEM	CONDITION	CRITERION
1	HIGH TEMPERATURE OPERATING	50 °C 200Hrs	◦ NO DEFECT IN COSMETIC AND OPERATIONAL FUNCTION ARE ALLOWABLE. ◦ TOTAL CURRENT CONSUMPTION SHOULD BELOW DOUBLE OF INITIAL VALUE.
2	LOW TEMPERATURE OPERATING	0 °C 200Hrs	
3	HIGH HUMIDITY	60 °C ,90%RH ,96Hrs	
4	HIGH TEMPERATURE	60 °C 200Hrs	
5	LOW TEMPERATURE	-20 °C 200Hrs	
6	TEMPERATURE CYCLING	-20 °C↔25 °C↔70 °C 30Min 5Min 30Min 10 CYCLES	
7	VIBRATION	RANDOM WAVE 40~500Hz ACCELERATION: 2g 2 Hrs/EACH DIRECTION (X,Y,Z)	

NOTE:

1) ABOVE CONDITIONS ARE SUITABLE FOR PICVUE'S STD PRODUCTS.
2) FOR RESTRICT PRODUCTS, THE TEST CONDITIONS LISTED AS ABOVE MUST BE REVISED.

15.0 SCREEN COSMETIC CRITERIA (TRANSFLECTIVE)

<table>
<tr><th>NO</th><th>Defect</th><th>Judgement Criterion</th><th>Partition</th></tr>
<tr><td>1</td><td>Spots</td><td>
A) Clear
<table>
<tr><th>Size:d mm</th><th>Acceptable Qty in active area</th></tr>
<tr><td>d ≤ 0.1
0.1 < d ≤ 0.2
0.2 < d ≤ 0.3
0.3 < d</td><td>Disregard
6
2
0</td></tr>
</table>
Note: Including pin holes and defective dots which must be within one pixel size.
B) Unclear
<table>
<tr><th>Size:d mm</th><th>Acceptable Qty in active area</th></tr>
<tr><td>d ≤ 0.2
0.2 < d ≤ 0.5
0.5 < d ≤ 0.7
0.7 < d</td><td>Disregard
6
2
0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2</td><td>Lines</td><td>
A) Clear


Note:( ):Acceptable Qty in active area
L :Length(mm)
W :Width (mm)
∞ :Disregard
B) Unclear


</td><td>Minor</td></tr>
<tr><td colspan="4">"Clear" :The shade and size are not changed by Vop.
"Unclear" :The shade and size are changed by Vop.</td></tr>
</table>