

Version : Preliminary

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TECHNICAL SPECIFICATION

MODEL NO. : PW070DS1T1

☐ Customer's Confirmation

Date _____

By _____

☐ PVI's Confirmation

Confirmed By _____

Prepared By _____

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Date : FEB. 02, 2000

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TECHNICAL SPECIFICATION**CONTENTS**

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1. Application

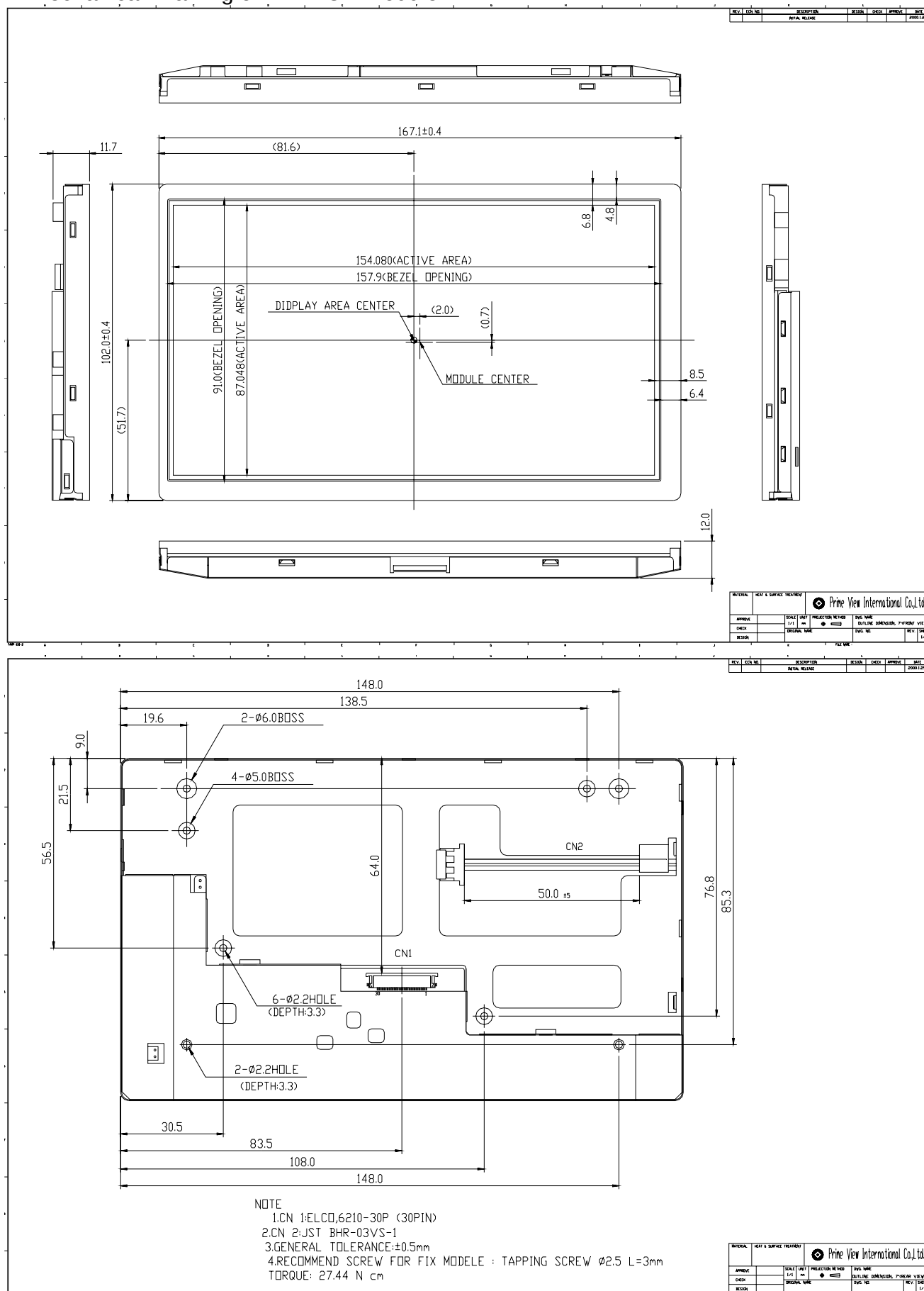
This technical specification applies to 7.0" color TFT-LCD module, P70AN1. The applications of the panel are car TV, portable DVD, GPS, multimedia applications and others AV system.

2. Features

- . Pixel in stripe configuration
- . Slim and compact
- . High Brightness
- . Image Reversion : Up/Down and Left/Right
- . 8 Video Display Mode

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	7.0 (16:9 diagonal)	inch
Display Mode	Normally White	
Display Format	1440(H)*234(V)	dot
Active Area	154.08 (H)*87.048 (V)	mm
Dot Pitch	0.107(H)*0.372 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	166.9 (W)*101.8 (H)*12.05 (D)	mm
Surface Treatment	Anti-Glare and Hard Coating	
Weight	200	g



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5. Input / Output Terminals

5-1) TFT-LCD Panel Driving

The interface connector is 6210-30P Series manufactured by ELCO or equivalent. (0.5mm pitch 30 pin)

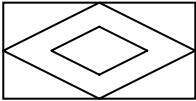
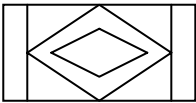
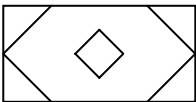
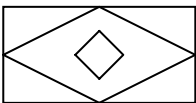
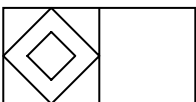
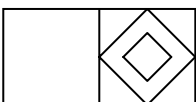
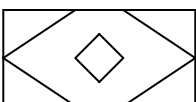
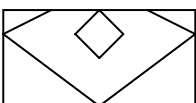
The connector interface pin assignments are listed in the Table below.

Pin No	Symbol	Description	Remark
1	NC	No Connection	
2	RED	Red Video Input	
3	GREEN	Green Video Input	
4	BLUE	Blue Video Input	
5	GND	Ground	
6	CSY	Composite Sync Input	
7	NC	No Connection	
8	NC	No Connection	
9	NC	No Connection	
10	NC	No Connection	
11	MODE 1	Display Mode Selection Switch (Refer to 5.2)	
12	MODE 2		
13	MODE 3		
14	GND	Ground	
15	BLK	Video Signal Mask Timing Output	
16	HSY	Horizontal Sync Output	
17	VSX	Vertical Sync Output	
18	VCC	Input Voltage For Logic/Logic Voltage For Source Driver	Note:5-1
19	POLS	Video Polarity Control Signal	
20	POLC	VCOM Polarity Control Signal	
21	GND	Ground	
22	U/D	Scanning Direction : (Low : Normal , High : Reverse)	
23	L/R	Scanning Direction : (Low : Normal , High : Reverse)	
24	N/P	NTSC/PAL Selection Signal(Low : PAL , High : NTSC)	
25	VD	Vertical Sync Input	Note:5-2
26	HD	Horizontal Sync Input	Note:5-2
27	GND	Ground	
28	VDD	Analog Voltage For Source Driver/Logic Voltage For Gate Driver	
29	VGON	Positive Voltage For Gate Driver	
30	VGOFF	Negative Voltage For Gate Driver	

Note 5-1:FPGA VCC=+3.3V, ASIC VCC=+5V

Note 5-2:Default is composite sync mode , if you uses separate mode , please contact PVI.

5.2)Display Mode

Display Mode	Display (Input Signal of 4:3 Aspect Ratio)	NO:11	NO:12	NO:13	Note
		Mode 1	Mode 2	Mode 3	
Full		Low	Low	Low	Input Video Signals Are Displayed In Full Screen.
Normal Center		High	Low	Low	Input Video Signals Are Displayed In The Center Screen.(4:3 Aspect Ratio)
Zoom 1		High	High	Low	Input Video Signal Of Central 176 Lines Are Display In Full Screen.(Vertically Extension)
Wide		Low	High	Low	Input Video Signals Are Displayed In Full Screen. (Horizontal Modification)
Normal Left		High	Low	High	Input Video Signals Are Display In the Left Screen. (4:3 Aspect Ratio)
Normal Right		Low	High	High	Input Video Signals Are Display In the Right Screen. (4:3 Aspect Ratio)
Zoom 2		Low	Low	High	Input Video Signal Of Central 204 Lines Are Display In Full Screen.(Vertically Extension)
Zoom 3		High	High	High	Same As Zoom 2 Mode Vertically Offset Centered

6 Absolute Maximum Ratings:

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage For Source Driver	V _{DD}	-0.5	7	V	
Supply Voltage For Gate Driver	H Level V _{GON}	0	40	V	
	L Level V _{GOFF}	-20	0	V	
Analog Input Voltage	V _R , V _G , V _B	-0.3	7.0	V	
Digital Input Signals		-0.5	5.5	V	
Digital Output Signals		-0.5	5.5	V	
Storage Temperature		-30	+80	°C	
Operation Temperature		-20	+70	°C	

7 Electrical Characteristics

7-1)Driving for TFT-LCD panel

		Symbol	MIN.	Typ	MAX	Unit	Remark
Supply Voltage For Source Driver	Analog	V _{DD}	4.5	5.0	5.5	V	
	Logic	V _{CC}	3.0	3.3	3.6	V	
Supply Voltage For Gate Driver	H level	V _{GON}	+15	+17	+19	V	
	L level	V _{GOFF}	-14	-12	-10	V	
Supply Voltage For controller		V _{DD}	4.5	5.0	5.5	V	
Analog input voltage	Amplitude						
	AC com						
Digital input voltage	H level	V _{IN}	+2.4	-	5	V	
	L level	V _{IL}	-0.3	-	0.5	V	
Digital output voltage	H level	V _{OH}	+2.4		5	V	
	L level	V _{OL}	0		0.5	V	

7-2) Backlight driving & Power Consumption

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
2	VL2	Input terminal (Low voltage side)	Note 7-1

Note 7-1 : Low voltage side of backlight inverter connects with Ground of inverter circuits.

Driving for backlight

Ta= 25

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	480	520	560	Vrms	$I_L=6mA$
Lamp current	I_L	4	6	8	mA	
Lamp frequency	P_L	20		60	KHz	Note 7-2
Kick-off voltage	Vs			1500	Vrms	
Kick-off voltage(-20)	Vs			TBD	Vrms	

Note 7-2 : The wave form of lamp driving voltage should be as closed to a perfect SIN wave as possible.

Power Consumption

Ta= 25

Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
LCD Panel Power Consumption			TBD		W	Note 7-3
Backlight Lamp Power Consumption			4.2		W	Note 7-4

Note 7-3 : The power consumption for backlight is not included.

Note 7-4 : Backlight lamp power consumption is calculated by $I_L \times V_L$.

7-4) Input / Output Connector

A) LCD Module Connector

The interface connector is 6210-30p Series manufactured by Elco or equivalent (0.5mm pitch 30pin)

B) Backlight Connector, JST BHR-03VS-1. Pin No. : 3, Pitch : 4 mm

7-5) Pixel Arrangement and Output Interface Pin

	1	2	3	4	5	6		1438	1439	1440
1	R	G	B	R	G	B		R	G	B
2	R	G	B	R	G	B		R	G	B
3	R	G	B	R	G	B		R	G	B
233	R	G	B	R	G	B		R	G	B
234	R	G	B	R	G	B		R	G	B

7-6)Signal Timing Waveforms
Timing Specification
[Horizontal]

Parameter	Symbol	Condition	NTSC	PAL	Unit	Notes
Horizontal Start Position	HPOS	-	11.35	11.54	usec	Note7-5
Horizontal Display Area	HDIS	-	50.01	50.36	usec	

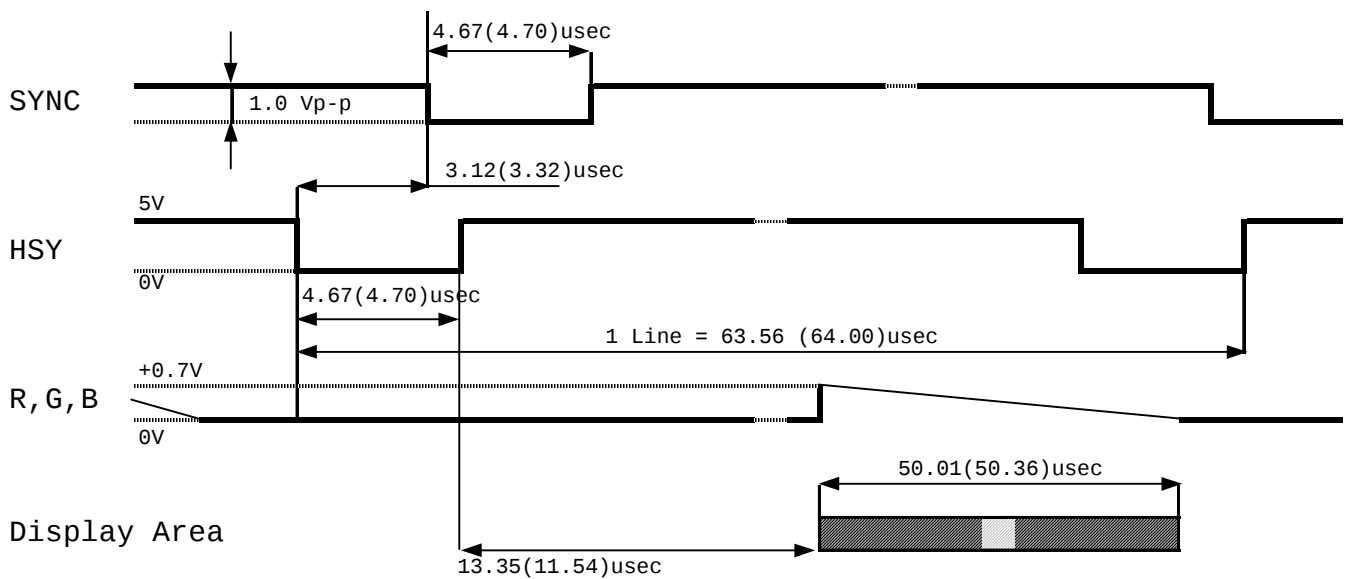
Notes :7-5

1. Sampling start based on the composite sync falling edge.
2. This value is default , if you want to charge ,please contact PVI.

[Vertical]

Parameter	Symbol	Condition		Display Mode					Unit	Notes
				Full Normal	Wide	Zoom 1	Zoom 2	Zoom 3		
Vertical Start Position	VPOS	NTSC	ODD EVEN	20 286	20 286	52 315	38 301	53 315	Line	Note 7-6
		PAL	ODD EVEN	26 339	26 363	62 375	50 363	62 375	Line	Note 7-6
Vertical Display Position	VDIS	NTSC		234	234	176	204	204	Line	
		PAL		281	281	210	234	234	Line	

Notes :7-6 Sampling start line number base on the vertical sync pulse (SYNC).



Note: 7-7 Values in brackets correspond to PAL mode ($f_H = 15.734(15.625)$ KHz).

7-7) Display Time Range

A) When sync. signal of NTSC system is applied.

a) Horizontally

11.35 ~ 63.4 μs.

b) Vertical

20 ~ 253 H

B) When sync. signal of PAL system is applied.

a) Horizontally

11.54.0 ~ 64 μs .

b) Vertical

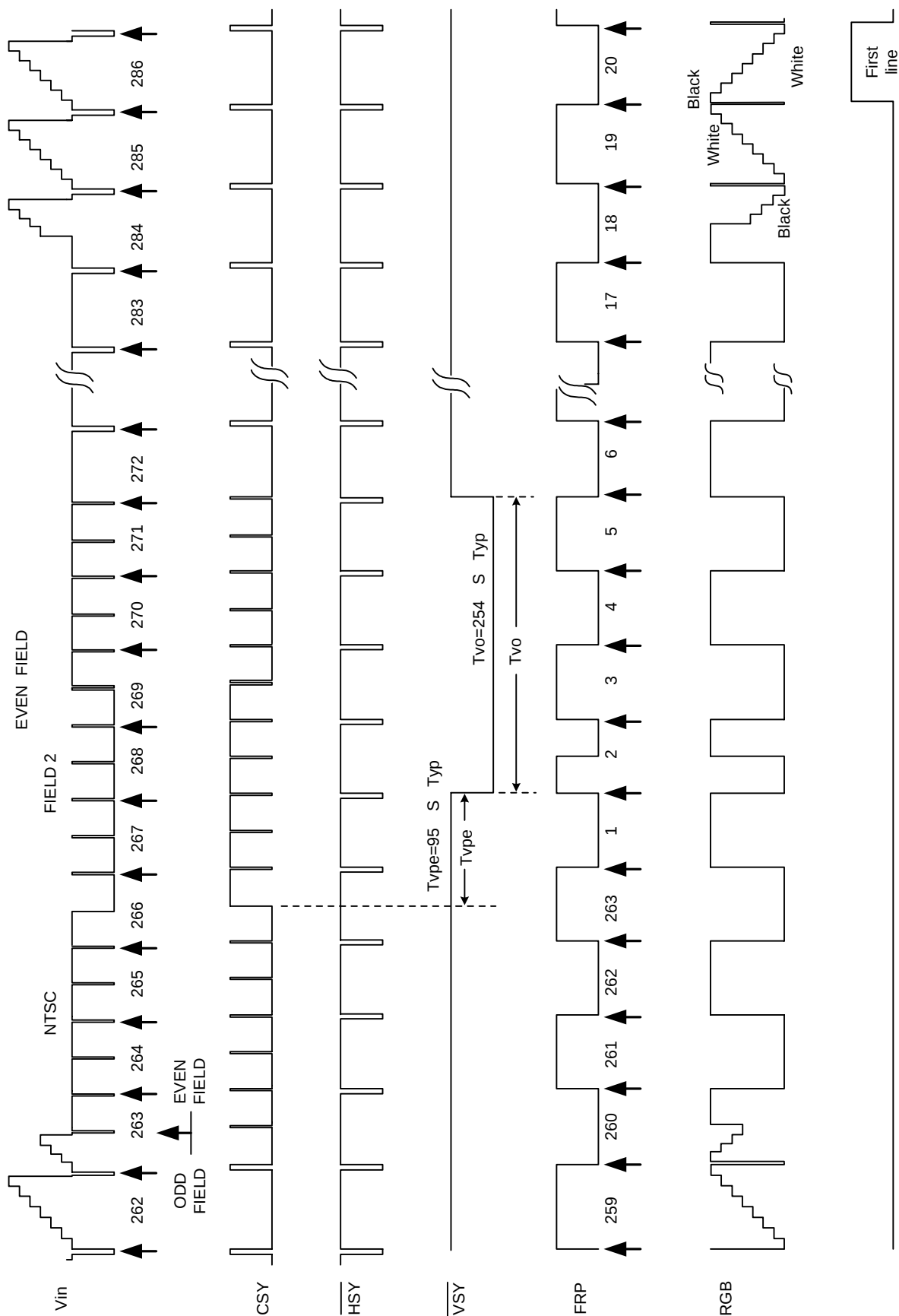
26 ~ 298 H

The diagram illustrates the timing of various video signals for the CCIR 601 standard. The signals are plotted against line numbers from 1 to 262. The signals shown are:

- Even and Odd Fields:** Indicated by arrows at the top of the diagram.
- NTSC:** A signal that is high for the first half of the frame and low for the second half.
- FIELD 1:** A signal that is high for the first half of the frame and low for the second half.
- ODD FIELD:** A signal that is high for the second half of the frame and low for the first half.
- CSY:** A signal that is high for the first half of the frame and low for the second half.
- HSY:** A signal that is high for the first half of the frame and low for the second half.
- VSY:** A signal that is high for the first half of the frame and low for the second half.
- FRP:** A signal that is high for the first half of the frame and low for the second half.
- RGB:** A signal that is high for the first half of the frame and low for the second half.

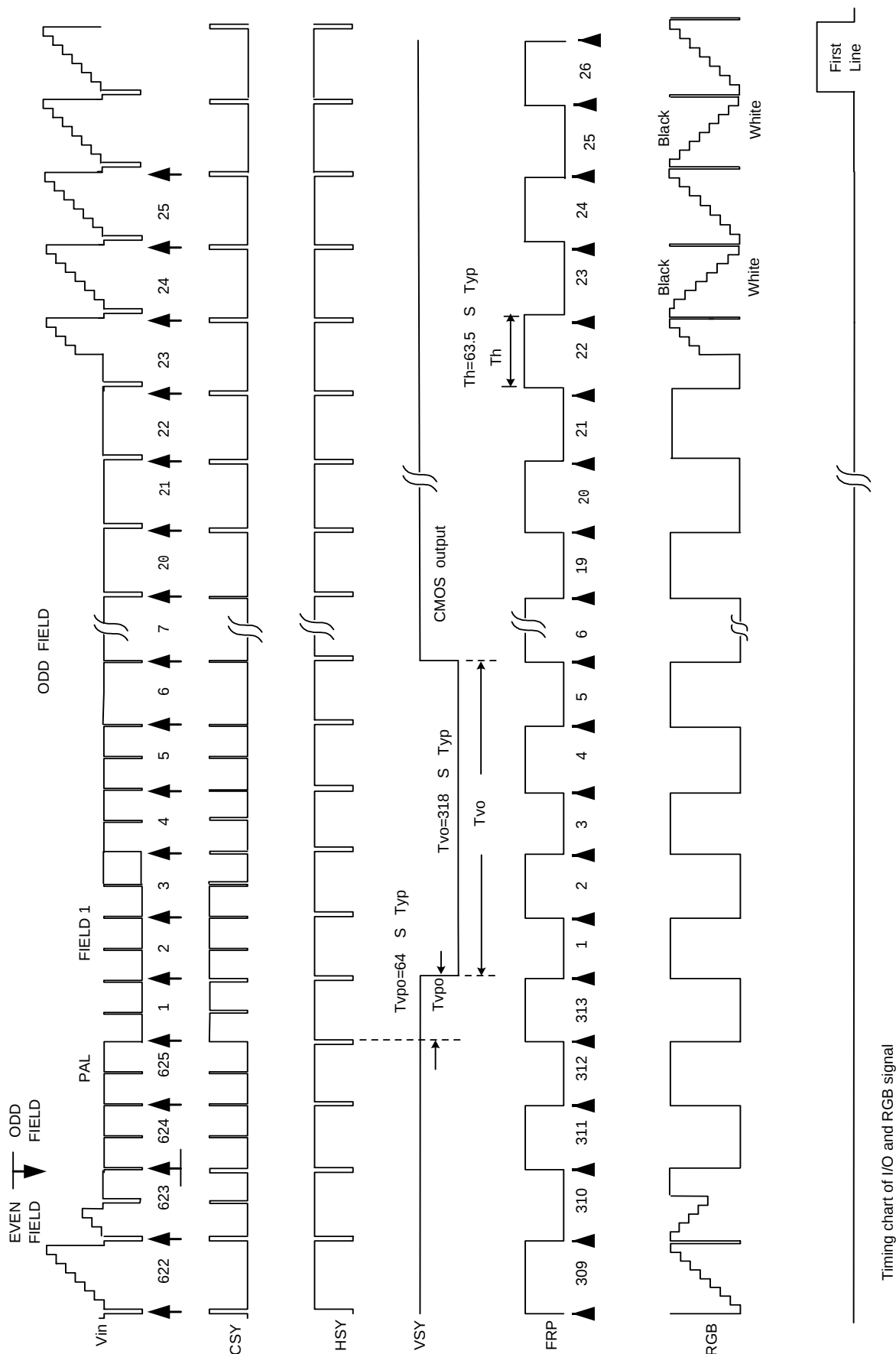
Key parameters and timing values are indicated:

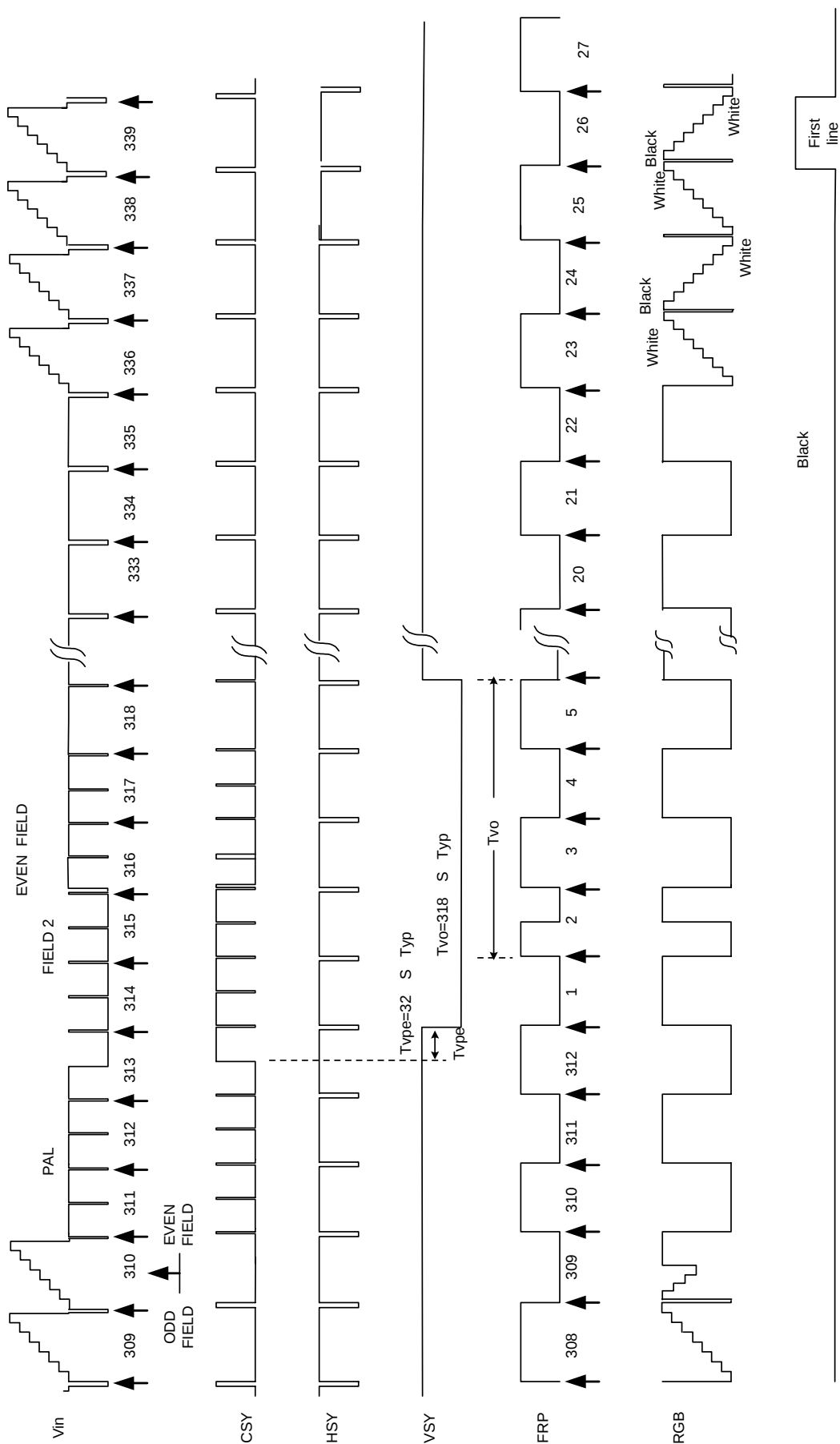
- Tvp0=63.5 S Typ:** The typical value for the time interval between the start of the first and second fields.
- Tvp0=254 S Typ:** The typical value for the time interval between the start of the first and second fields.
- Th=63.5 S Typ:** The typical value for the time interval between the start of the first and second fields.



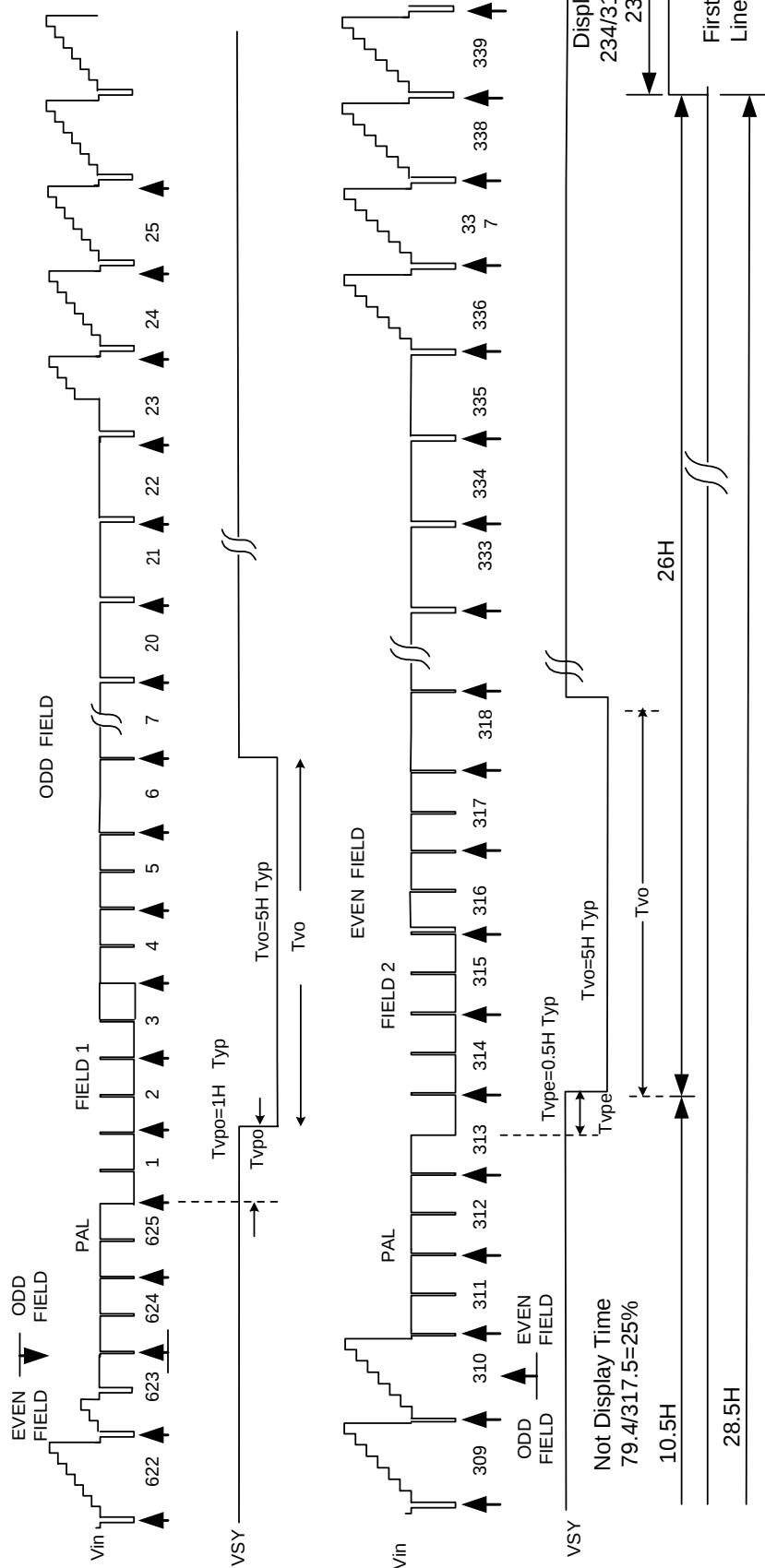
Timing chart of I/O and RGB signal

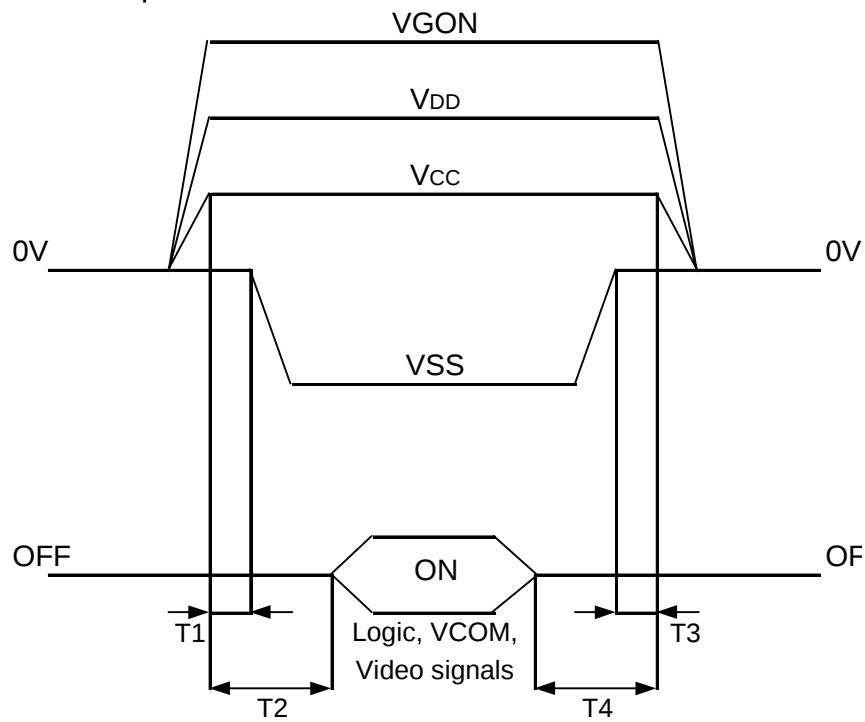
D) PAL System Timing Reference





Timing chart of I/O and RGB signal



8.Power Sequence


- 1) $10 \text{ msec} \leq T1 < T2, 0 < T3 < T4 \leq 10 \text{ msec}$
- 2) Vcc, VDD, VGON

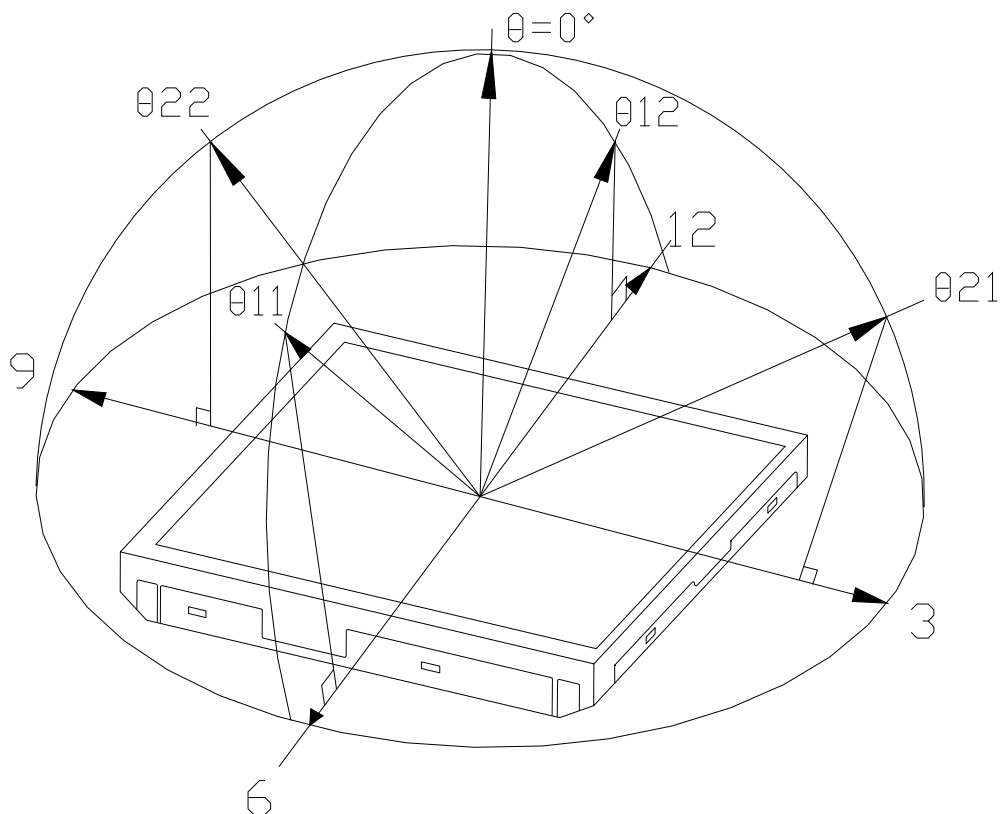
9. Optical Characteristics

9-1) Specification:

$T_a = 25$

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ_{21}, θ_{22}	$CR \geq 10$	45	55		deg	Note 9-1
	Vertical	θ_{12}		10	15		deg	Note 9-1
		θ_{11}		30	35		deg	Note 9-1
Contrast Ratio		CR		80	150			Note 9-2
Response time	Rise	Tr	$\theta = 0^\circ$			30	ms	Note 9-4
	Fall	Tf				50	ms	
Brightness				300	350		cd/m ²	Note 9-3
White		x						Note 9-3
Chromaticity		y						
Lamp Life Time _{+25°C}				10,000			hr	

Note 9-1: The definitions of viewing angles

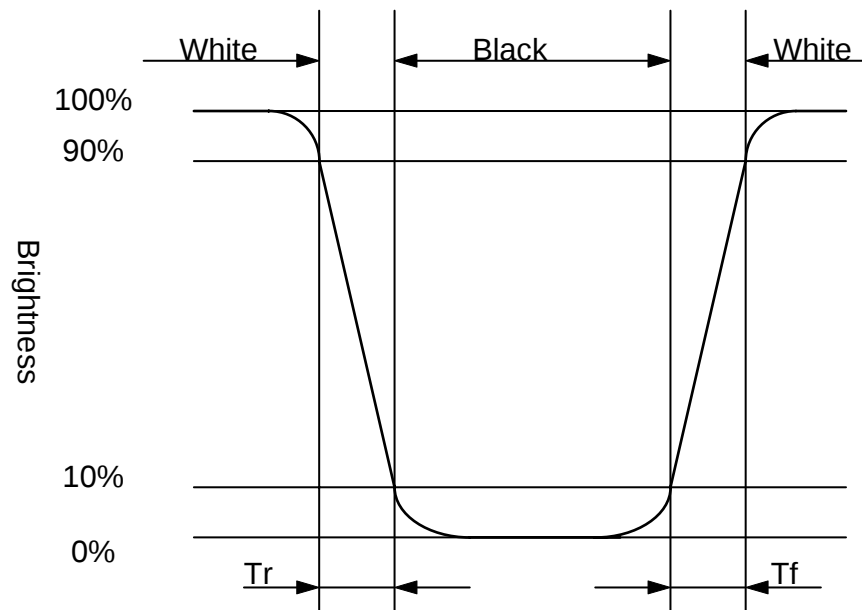


Note 9-2 : $CR = \frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$
 (Testing configuration see 8-2)

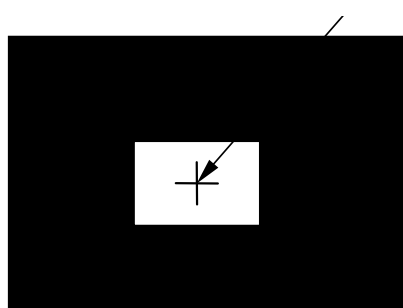
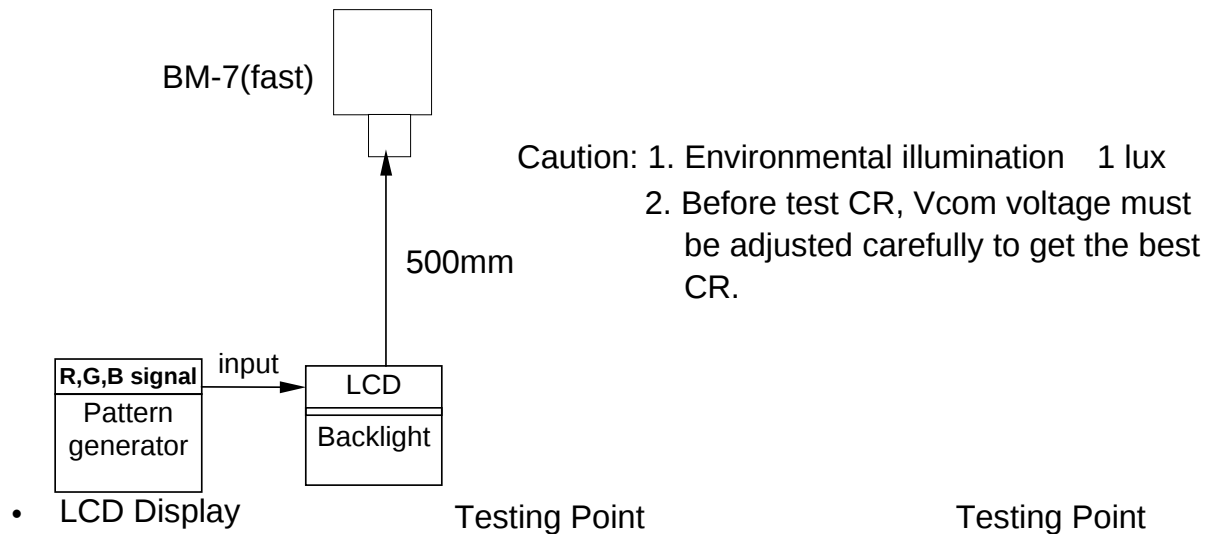
Contrast Ratio is measured in optimum common electrode voltage.

Note 9-3 : Topcon BM-7(fast) luminance meter 2°field of view is used in the testing (after 20~30 minutes operation).
 Lamp Current 6mA

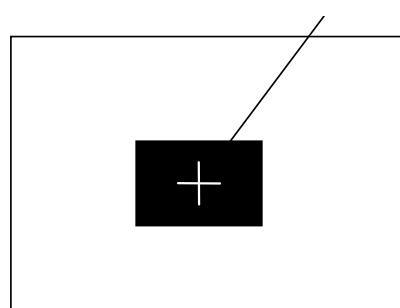
Note 9-4: The definition of response time:



9-2) Testing configuration

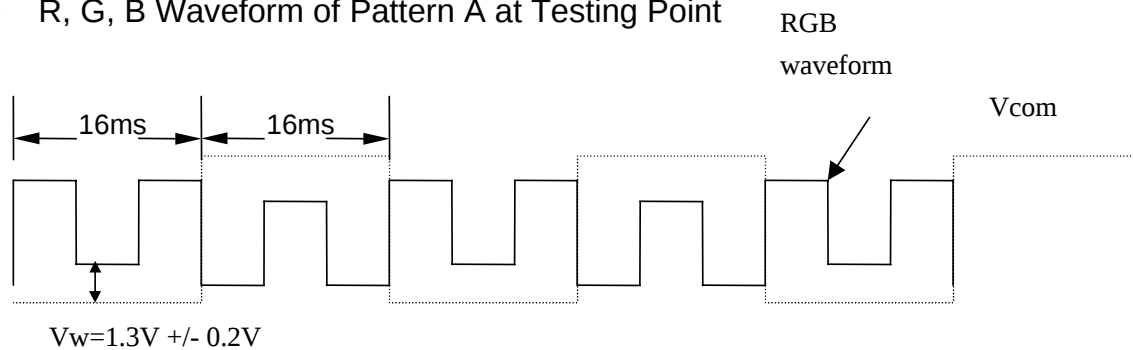


Pattern A

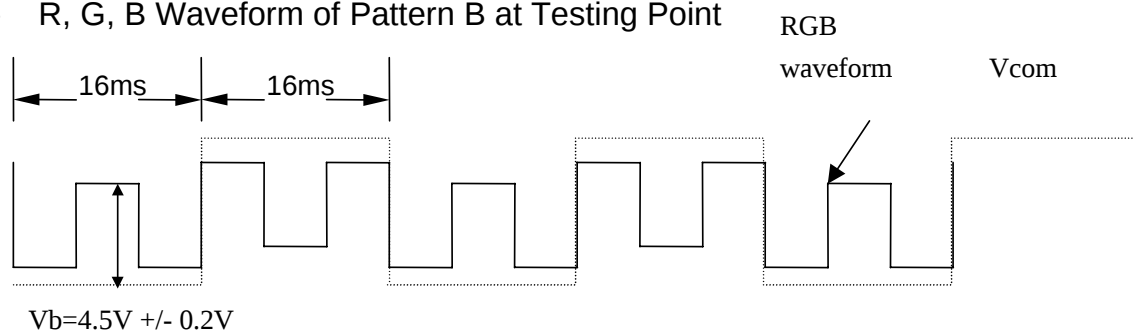


Pattern B

- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



10. Reliability Test

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80 , 240 hrs
2	Low Temperature Storage Test	Ta = -30 , 240 hrs
3	High Temperature Operation Test	Ta = +70 , 240 hrs
4	Low Temperature Operation Test	Ta = -20 , 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60 , 95%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-25 → +25 → +70 , 200 Cycles 30 min 5min 30 min
7	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz Amplitude : 1.0 mm Sweep time: 11 mins Test Period: 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction: ±X, ±Y, ±Z Cycle: 3 times
9	Electrostatic Discharge Test	150pF, 330Ω Air: ±15KV; Contact: ±8KV 10 times/point, 9 points/panel face

Ta: ambient temperature

[Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

The diagram illustrates the architecture of an LCD driver system. A central **Controller** block is connected to several peripheral components and receives various inputs.

Inputs to the Controller:

- HSY, VSY, CSY (bidirectional)
- BLK, U/D, R/L, N/P
- VGON, VGOFF
- Mode 1,2,3
- POLS, POLC (bidirectional)
- +5 V
- +17 V
- 12 V
- VR, VG, VB
- 3.3 V

Internal Blocks and Connections:

- The **Controller** is connected to a **PLL** block, which is part of a dashed box containing the **VCO** (Vibrating Crystal Oscillator) and **HPOS** (Horizontal Positioning) blocks. The **PLL** is connected to the **VR** (Variable Resistor) block within the **VCO**.
- The **Controller** is connected to the **V Driver (Gate)** block.
- The **V Driver (Gate)** block is connected to the **LCD Panel** block.
- The **Controller** is connected to the **H Driver (Source)** block.
- The **H Driver (Source)** block is connected to the **LCD Panel** block.
- The **LCD Panel** block is connected to the **Back-light** block.

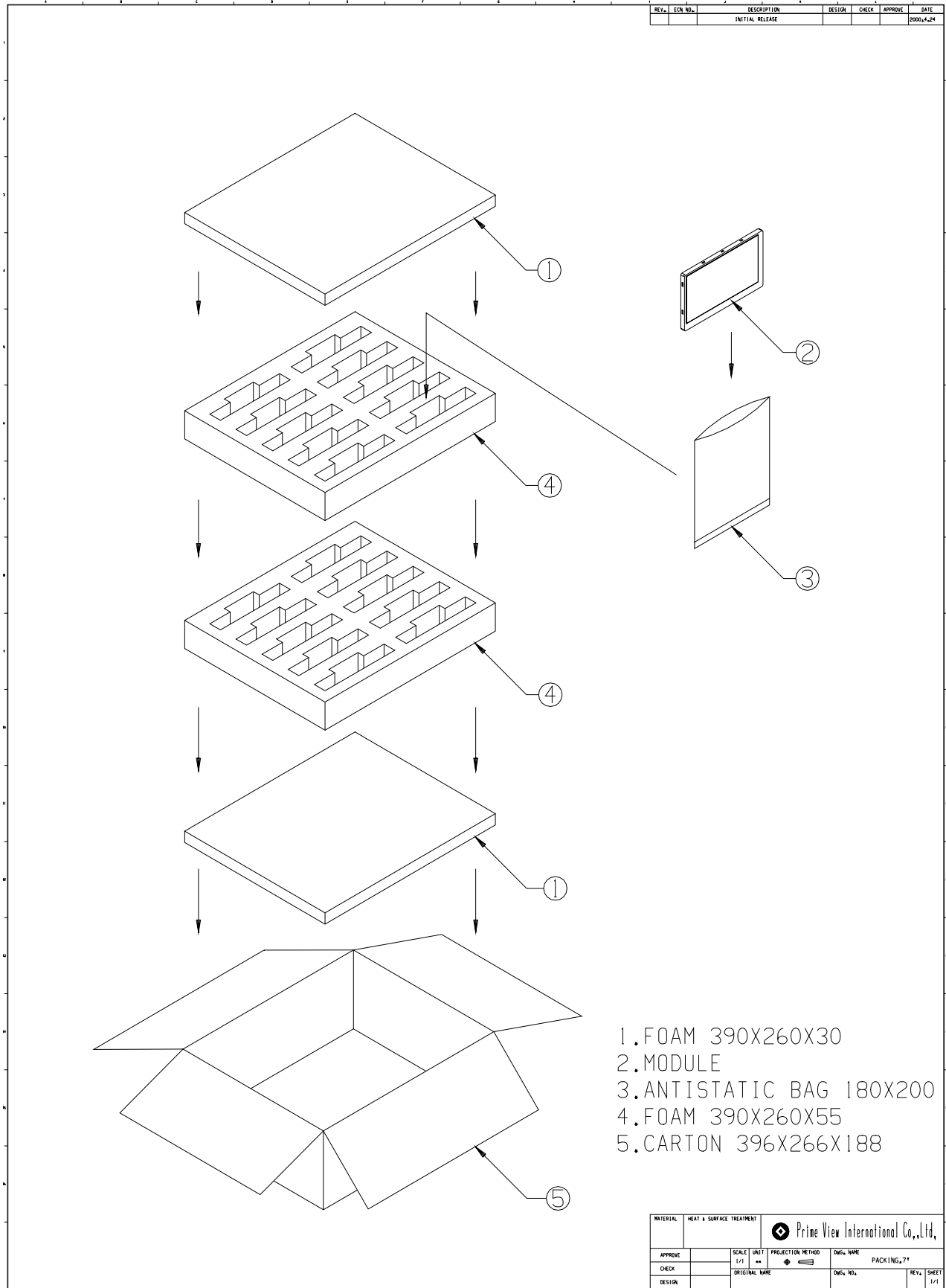
Outputs from the Controller:

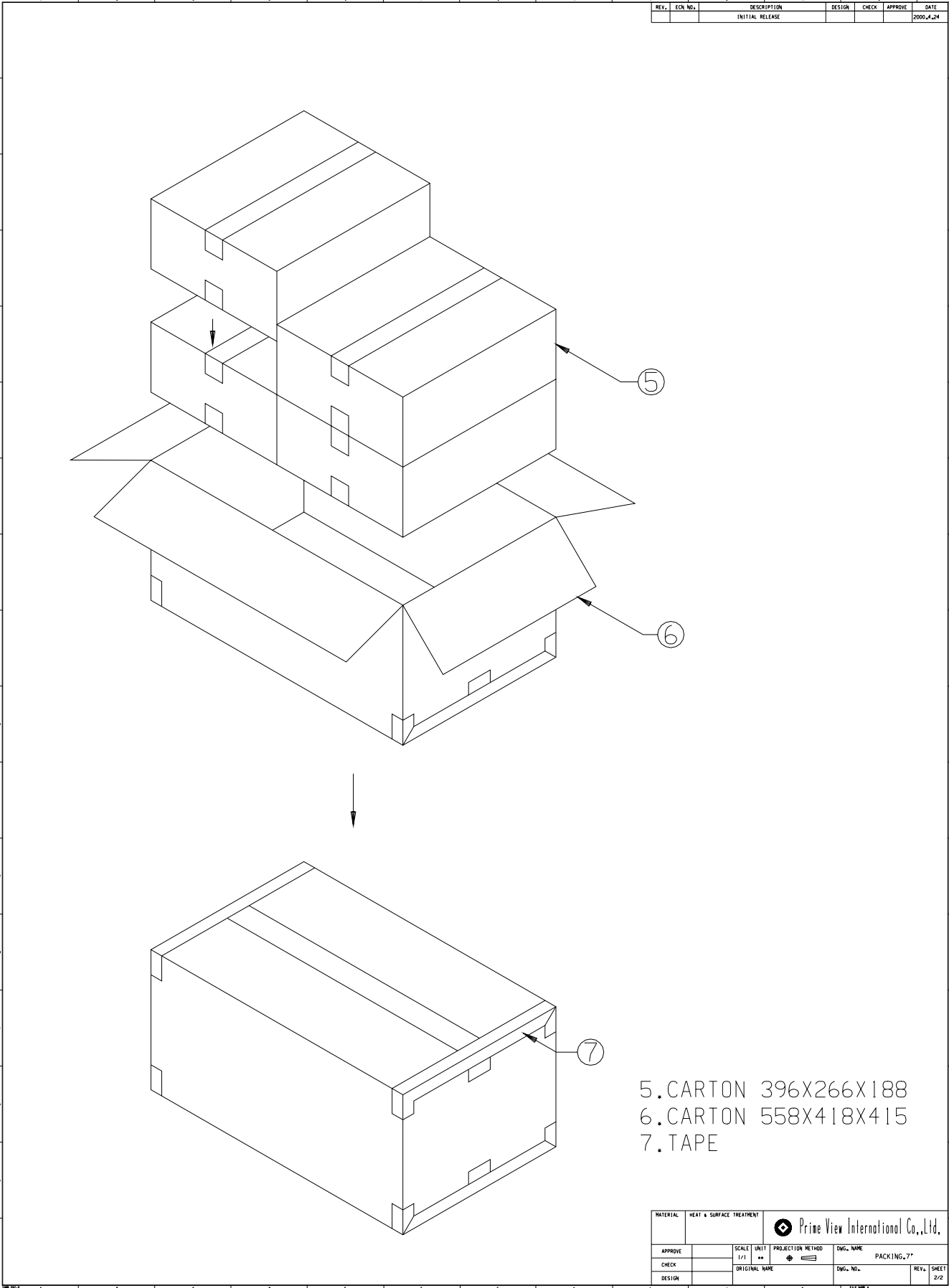
- PLL
- V Driver (Gate)
- H Driver (Source)

Other Connections:

- The **VR** block is connected to the **H Driver (Source)** block.
- The **VR** block is connected to the **LCD Panel** block.
- The **VR** block is connected to the **Back-light** block.
- The **VR** block is connected to the **Back-light** block.
- The **VR** block is connected to the **Back-light** block.

12. Packing





Revision History

Rev.	Issued Date	Revised Contents
0	FEB. 02,2000	NEW