

Version : 0.2

<p style="text-align: center;">TECHNICAL SPECIFICATION</p> <p style="text-align: center;">MODEL NO. : PW080XU1</p>
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Customer's Confirmation

Customer _____

Date _____

By _____

PVI's Confirmation

Confirmed By _____

Prepared By _____

Date :Jun. 03, 2005

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TECHNICAL SPECIFICATION

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1. Application

This technical specification applies to 8" color TFT-LCD module, PW080XU1.
The applications of the panel are car TV, portable DVD, GPS, multimedia applications and others AV system.

2. Features

- . Amorphous silicon TFT-LCD panel with Back-Light unit.

- . Pixel in stripe configuration

- . Compatible with NTSC and PAL system

- . Slim and compact

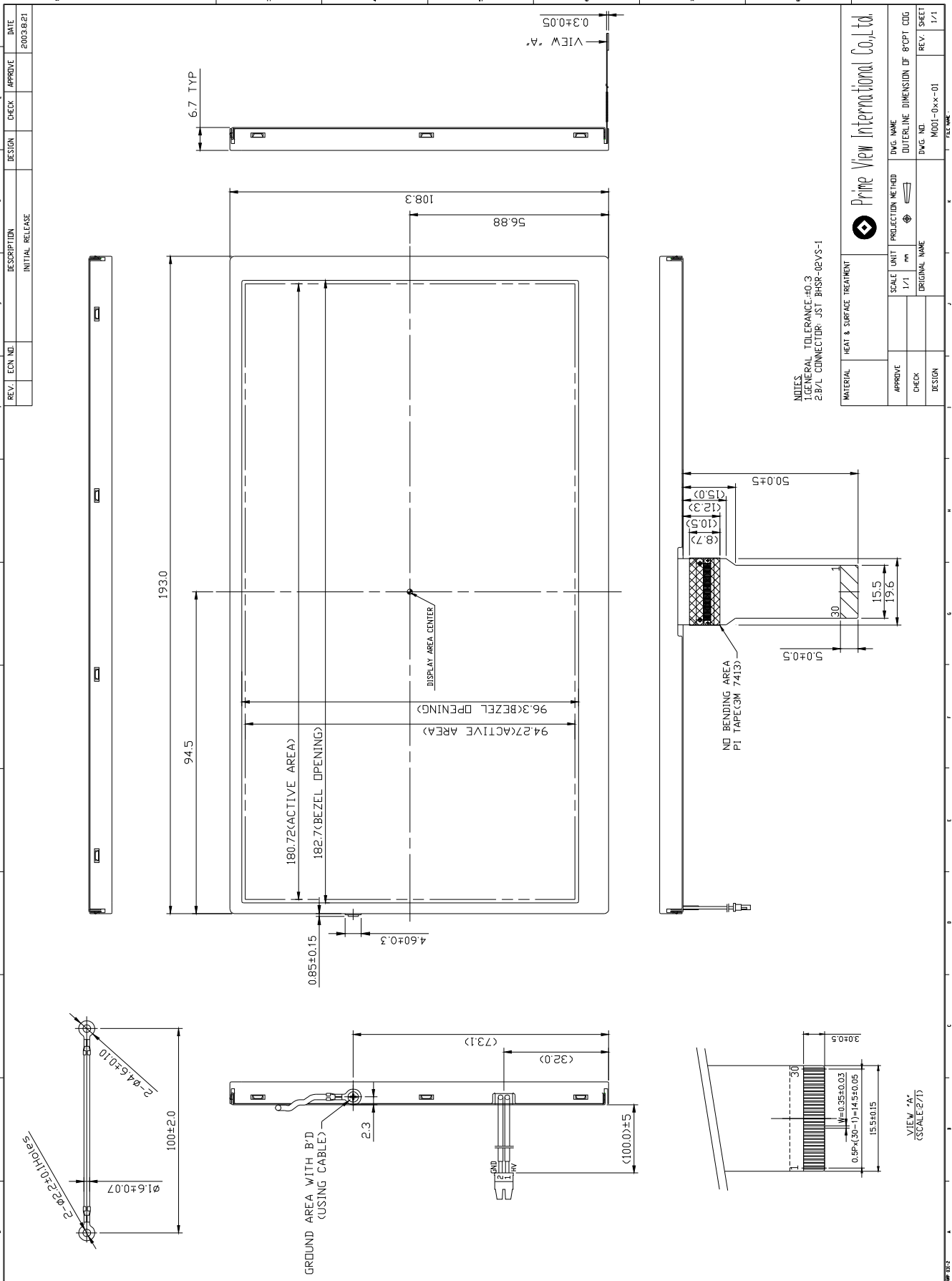
- . Up / Down and Left / Right Image Reversion

- . Support Multi Video Display Mode
(With PVI timing controller : PVI-1004D)

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	8 (16:8 diagonal)	Inch
Display Format	1440 (H) x220(V)	Dot
Active Area	180.72 (H)x94.27 (V)	Mm
Dot Pitch	0.126 (H)x0.429 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	193.0 (W)x108.3 (H)x6.7 (D) (typ.)	mm
Surface Treatment	Anti-Glare	
Weight	200±10	g

4. Mechanical Drawing of TFT-LCD Module



5. Input / Output Terminals

LCD Module Connector

FPC Down Connect , 30 Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	GND	-	Ground for logic circuit	
2	V _{CC}	I	Supply voltage of logic control circuit for gate driver	Note 5-3
3	NC	-	No connection	
4	V _{EE}	I	Negative power for gate driver	Note 5-4
5	NC	-	No connection	
6	V _{GH}	I	Positive power for gate driver	Note 5-5
7	NC	-	No connection	
8	STVD	I/O	Vertical start pulse	Note 5-1
9	STVU	I/O	Vertical start pulse	
10	CKV	I	Shift clock for gate driver	
11	U/D	I	Up / Down Control for gate driver	Note 5-1
12	OE3	I	Output enable for gate driver	
13	OE2	I	Output enable for gate driver	
14	OE1	I	Output enable for gate driver	
15	V _{COM}	I	Common electrode voltage	
16	STHL	I/O	Start pulse for source driver	Note 5-2
17	V _{SS2}	-	Ground for analog circuit	
18	V _R	I	Video Input R	
19	V _G	I	Video Input G	
20	V _B	I	Video Input B	
21	V _{SS1}	-	Ground for digital circuit	
22	V _{DD2}	I	Supply power for analog circuit	Note 5-6
23	CPH1	I	Sampling and shift clock for source driver	
24	CPH2	I	Sampling and shift clock for source driver	
25	CPH3	I	Sampling and shift clock for source driver	
26	V _{DD1}	I	Supply power for digital circuit	Note 5-7
27	R/L	I	Left / Right Control for source driver	Note 5-2
28	NC	I	No Connection	
29	OEH	I	Output enable for source driver	
30	STHR	I/O	Start pulse for source driver	Note 5-2

Note 5-1

U/D	STVD	STVU	scanning direction
V _{cc}	Input	output	down to up
GND	Output	input	up to down

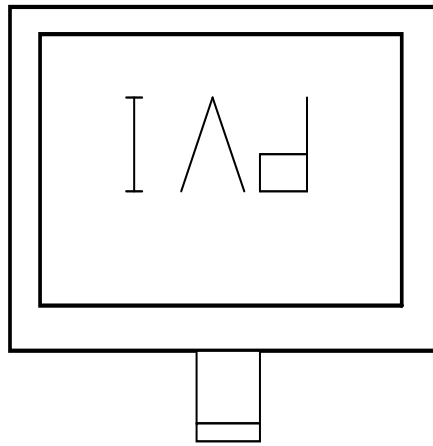
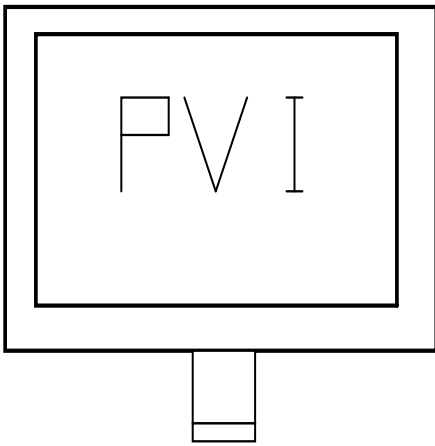
Note 5-2

R/L	STHL	STHR	scanning direction
V _{cc}	output	input	left to right
GND	input	output	right to left

The definitions of Note 5-1,5-2

U/D(PIN 11)=Low R/L(PIN 27)=High

U/D(PIN 11)=High R/L(PIN 27)=Low



Note 5-3 : V_{CC} TYP. = +3.3V

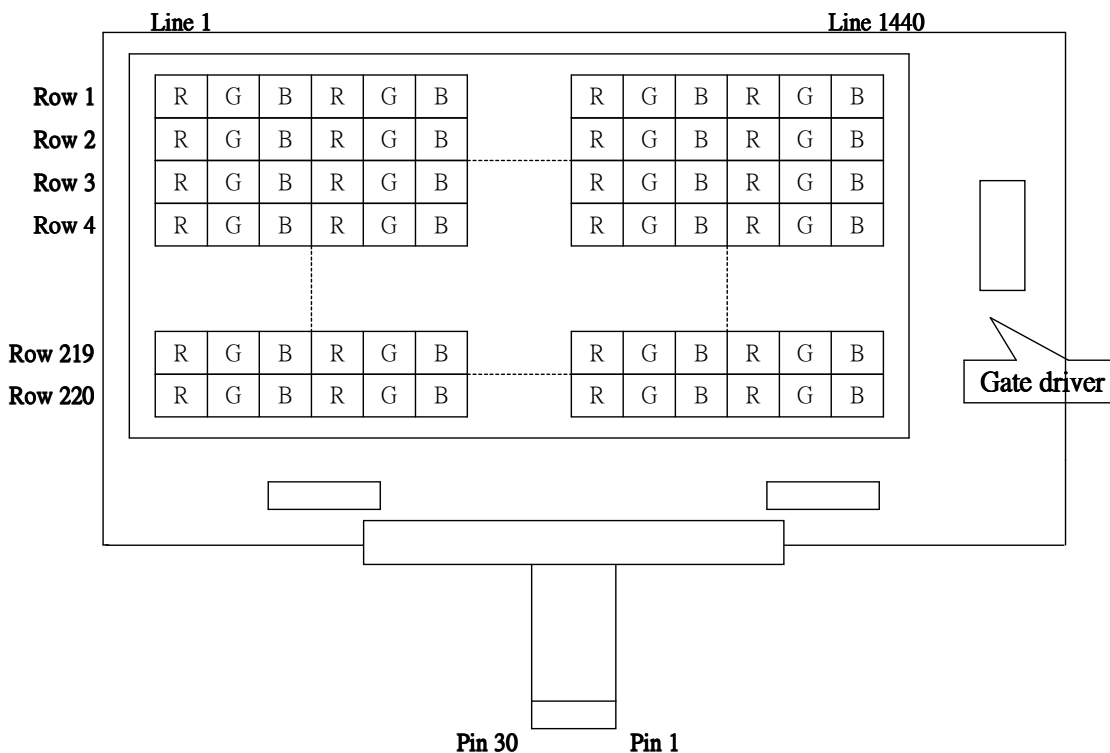
Note 5-4 : V_{EE} TYP. = -12V

Note 5-5 : V_{GH} TYP. = +17V

Note 5-6 : V_{DD2} TYP. = +5V

Note 5-7 : V_{DD1} TYP. = +3.3V

6. Pixel Arrangement and input connector pin NO.



7. Absolute Maximum Ratings

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage For Source Driver	V_{DD2}	-0.3	+5.8	V	
	V_{DD1}	-0.3	+7.0	V	
Supply Voltage For Gate Driver	V_{CC}	-0.3	+7.0	V	
	$V_{GH}-V_{EE}$	-0.3	+45.0	V	
	H Level V_{GH}	-0.3	+32.0	V	
	L Level V_{EE}	-22.0	+0.3	V	
Analog Signal Input Level	V_R, V_G, V_B	-0.2	$V_{DD1}+0.2$	V	Note 7-1
Storage Temperature		-20	+70	°C	
Operation Temperature		0	+60	°C	Note 7-2

Notes 7-1 : Analog Input Voltage means V_R, V_G, V_B .

Notes 7-2 : Optical characteristics shown in Table 10-1 are measured under $T_a=+25^{\circ}\text{C}$.

8. Electrical Characteristics
8-1) Recommended Driving condition for TFT-LCD panel

Parameter		Symbol	MIN.	Typ.	MAX.	Unit	Remark
Supply Voltage For Source Driver	Analog	V_{DD2}	+4.5	+5.0	+5.5	V	
	Logic	V_{DD1}	+3.0	+3.3	+3.6	V	
Supply Voltage For Gate Driver	H level	V_{GH}	+15	+17	+19	V	
	L level	$V_{EE\ DC}$	-13.0	-12	-10.5	V	DC Component of V_{EE}
		$V_{EE\ AC}$		+6.0		V_{P-P}	AC Component of V_{EE}
	Logic	V_{CC}	+3.0	+3.3	+3.6	V	
Analog Signal input Level		V_{iAC}		+4.0	+4.2	V	AC Component
		V_{iDC}		2.5		V	DC Component
Digital input voltage	H level	V_{IH}	0.7 V_{DD1}	-	V_{DD1}	V	
	L level	V_{IL}	-0.3	-	0.3 V_{DD1}	V	
Digital output voltage	H level	V_{OH}	0.7 V_{DD1}	-	V_{DD1}	V	
	L level	V_{OL}	-0.3	-	0.3 V_{DD1}	V	
V_{COM}		$V_{C\ AC}$	-	+6.0	-	V_{P-P}	AC Component of V_{COM}
		$V_{C\ DC}$		1.5		V	DC Component of V_{COM}

Note 8-1 : PVI strongly suggests that the $V_{COM\ DC}$ level shall be adjustable , and the adjustable level range is $1.5V\pm 1V$, every module's $V_{COM\ DC}$ level shall be carefully adjusted to show a best image performance.

8-2) Recommended driving condition for back light

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	500	550	600	Vrms	$I_L=6mA$
Lamp current	I_L	3	6	8	MA	Note 8-2
Lamp frequency	P_L	30	43	80	KHz	Note 8-3
Kick-off voltage(25°C) (Reference Value)	V_s		720	830	Vrms	Note 8-4
Kick-off voltage(0°C) (Reference Value)					Vrms	

Note 8-2 : In order to satisfy the quality of B/L , no matter use what kind of inverter , the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 8-3 : The waveform of lamp driving voltage should be as closed to a perfect sine wave as possible.

Note 8-4 : The Kick-off times ≥ 1 sec.

Back Light driving

Back Light Connector : JST BHSR-02VS-1, Pin No. : 2 , Pitch : 3.5 mm

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
2	VL2	Input terminal (Low voltage side)	Note 8-5

Note 8-5 : Low voltage side of back light inverter connects with Ground of inverter circuits.

8-3) Power Consumption

$T_a = 25\text{ }^\circ\text{C}$

Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
Supply current for Gate Driver (Hi level)	I_{GH}	$V_{GH} = +17V$	0.2	0.5	mA	
Supply current for Gate Driver (Low level)	I_{EE}	$V_{EE} = -12V$	1.0	2.0	mA	V_{EE} center voltage
Supply current for Source Driver(Digital)	I_{DD1}	$V_{DD1} = +3.3V$	1.2	2.0	mA	
Supply current for Source Driver(Analog)	I_{DD2}	$V_{DD2} = +5V$	7.0	10.0	mA	
Supply current for Gate Driver (Digital)	I_{CC}	$V_{CC} = +3.3V$	0.1	0.2	mA	
LCD Panel Power Consumption			54.3	89.0	mW	Note 8-6
Back Light Lamp Power Consumption			3.30		W	Note 8-7

Note 8-6 : The power consumption for back light is not included.

Note 8-7 : Back light lamp power consumption is calculated by $I_L \times V_L$.

8-4) Timing Characteristics Of Input Signals

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
Rising time	t_r	-	-	10	ns	
Falling time	t_f	-	-	10	ns	
High and low level pulse width	t_{CPH}	9.2	9.6	10.0	M _{HZ}	CPH1~CPH3
CPH pulse duty	t_{CWH}	30	50	70	%	CPH1~CPH3
STH setup time	t_{SUH}	20	-	-	ns	STHR,STHL
STH hold time	t_{HDH}	20	-	-	ns	STHR,STHL
STH pulse width	t_{STH}	-	1	-	t_{CPH}	STHR,STHL
STH period	t_H	61.5	63.5	65.5	μ s	STHR,STHL
OEH pulse width	t_{OEH}	-	1.40	-	μ s	OEH
Sample and hold disable time	t_{DIS1}	-	7.43	-	μ s	
OEV pulse width	t_{OEV}	-	18	-	μ s	OEV
CKV pulse width	t_{CKV}	-	31.75	-	μ s	CKV
Clean enable time	t_{DIS2}	-	9.0	-	μ s	
Horizontal display start	t_{SH}	-	0	-	$t_{CPH}/3$	
Horizontal display timing range	t_{DH}	-	480	-	$t_{CPH}/3$	
STV setup time	t_{SUV}	400	-	-	ns	STVU,STVD
STV hold time	t_{HDV}	400	-	-	ns	STVU,STVD
STV pulse width	t_{STV}	-	-	1	t_H	STVU,STVD
Horizontal lines per field	t_V	256	262	268	t_H	
Vertical display start	t_{SV}		3	-	t_H	
Vertical display timing range	t_{DV}		234	-	t_H	
VCOM rising time	t_{COM}		-	5	μ s	
VCOM falling time	t_{COM}		-	5	μ s	
VCOM delay time	t_{DCOM}		-	3	μ s	
RGB delay time	t_{DRGB}		-	1	μ s	

8-5) Signal Timing Waveforms

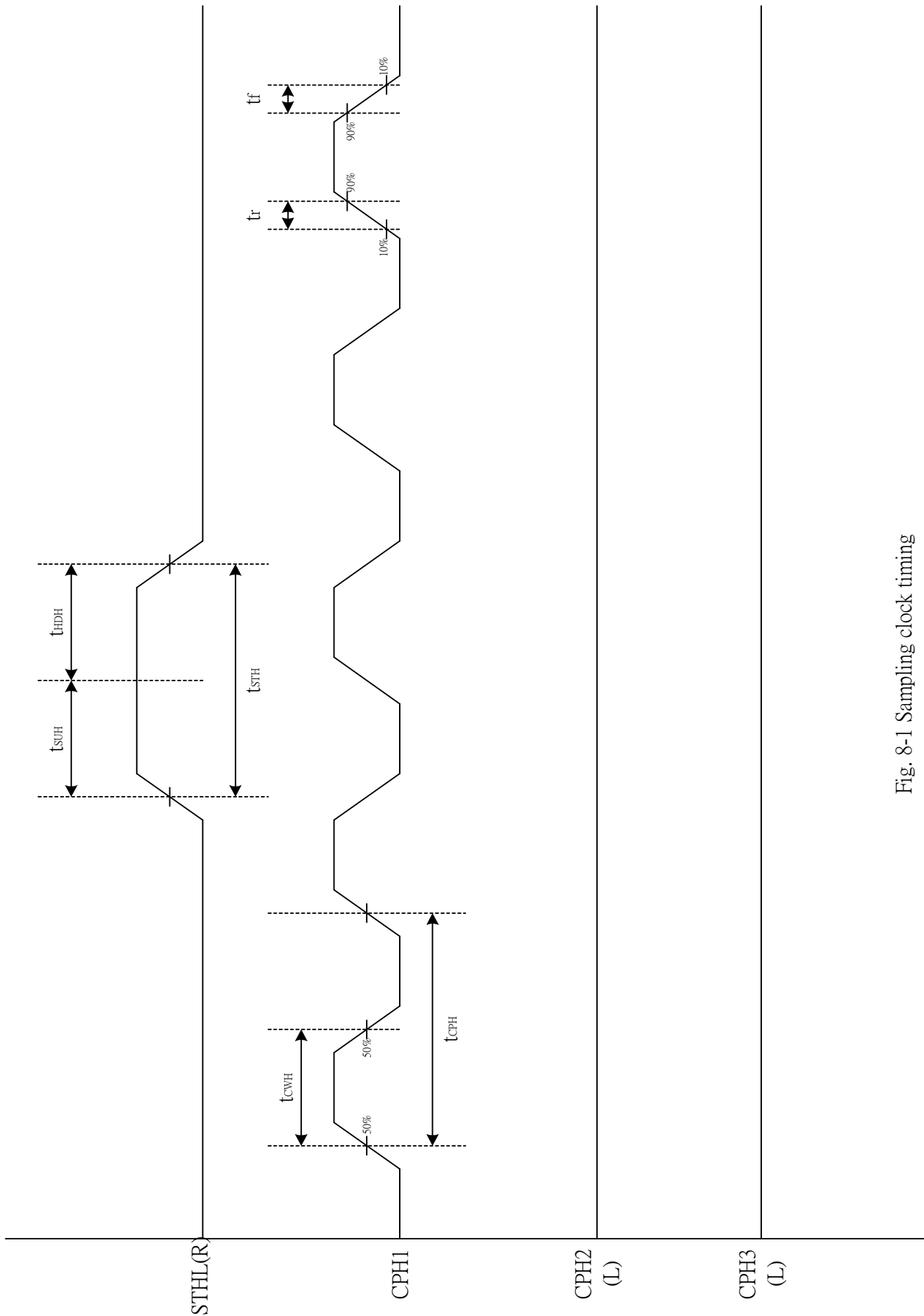


Fig. 8-1 Sampling clock timing

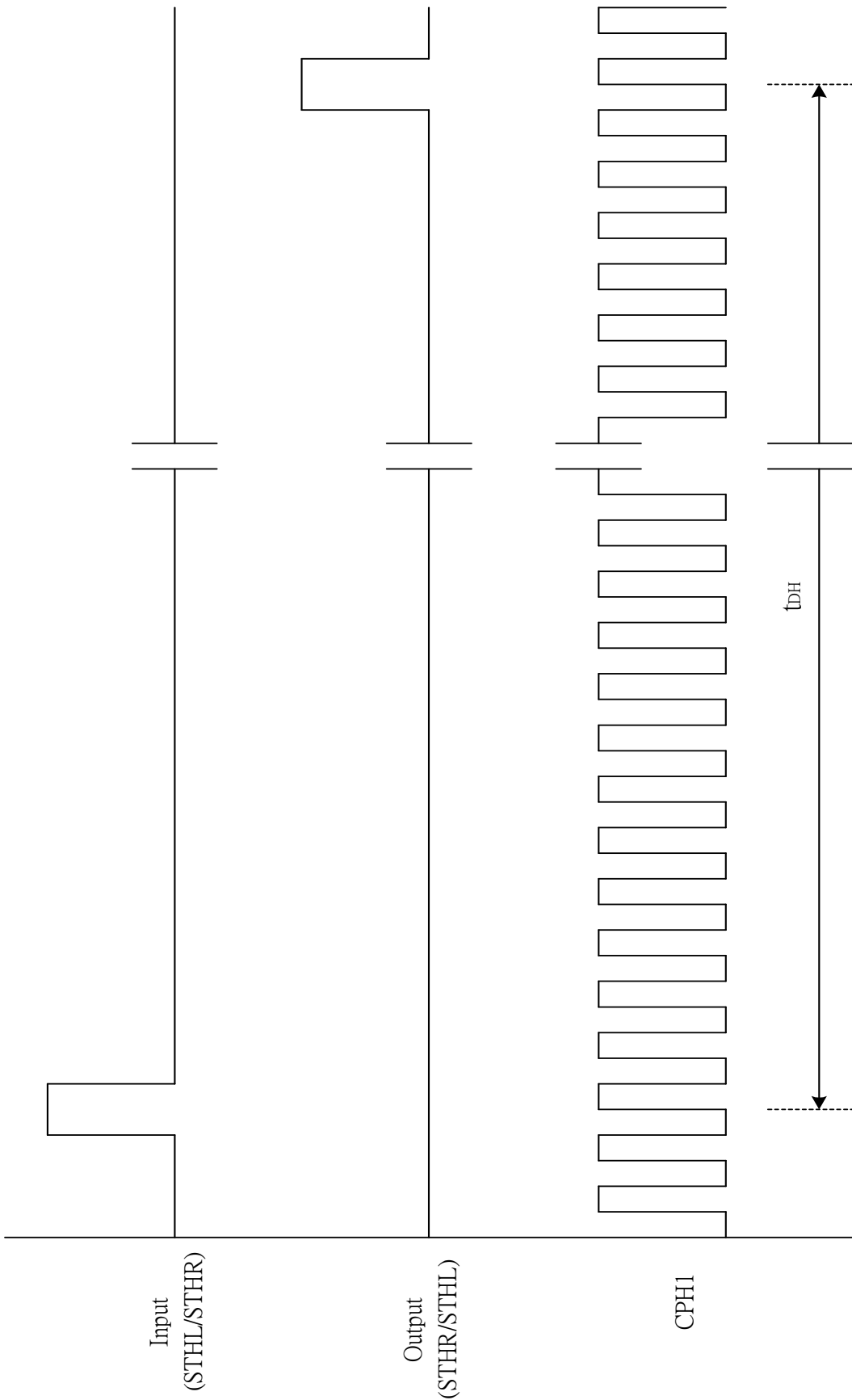


Fig. 8-2 Horizontal display timing range

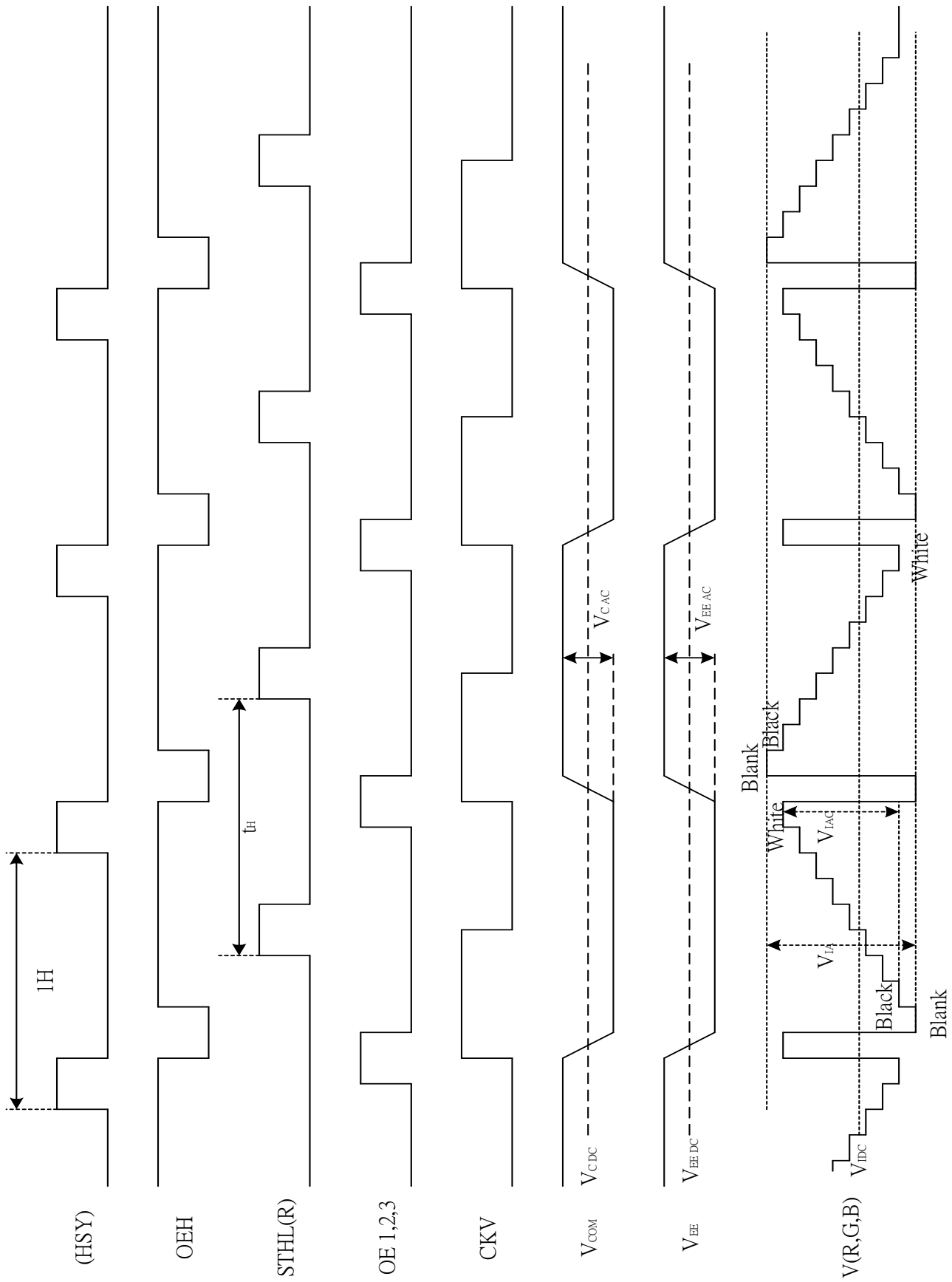
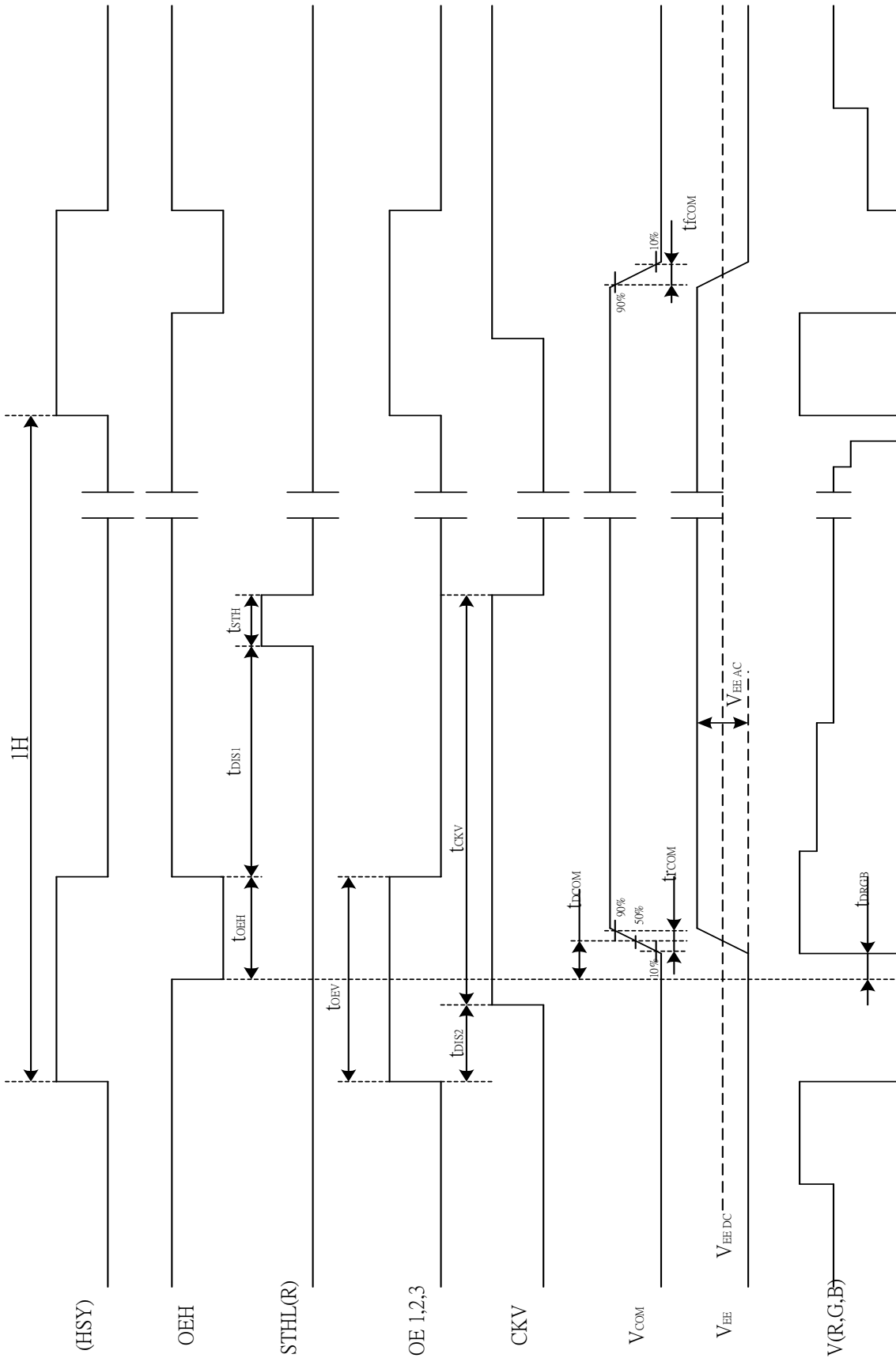


Fig. 8-3 (a) Horizontal timing



Note : The falling edge of OEV should be synchronized with the falling edge of OEH

Fig. 8-3 (b) Detail horizontal timing

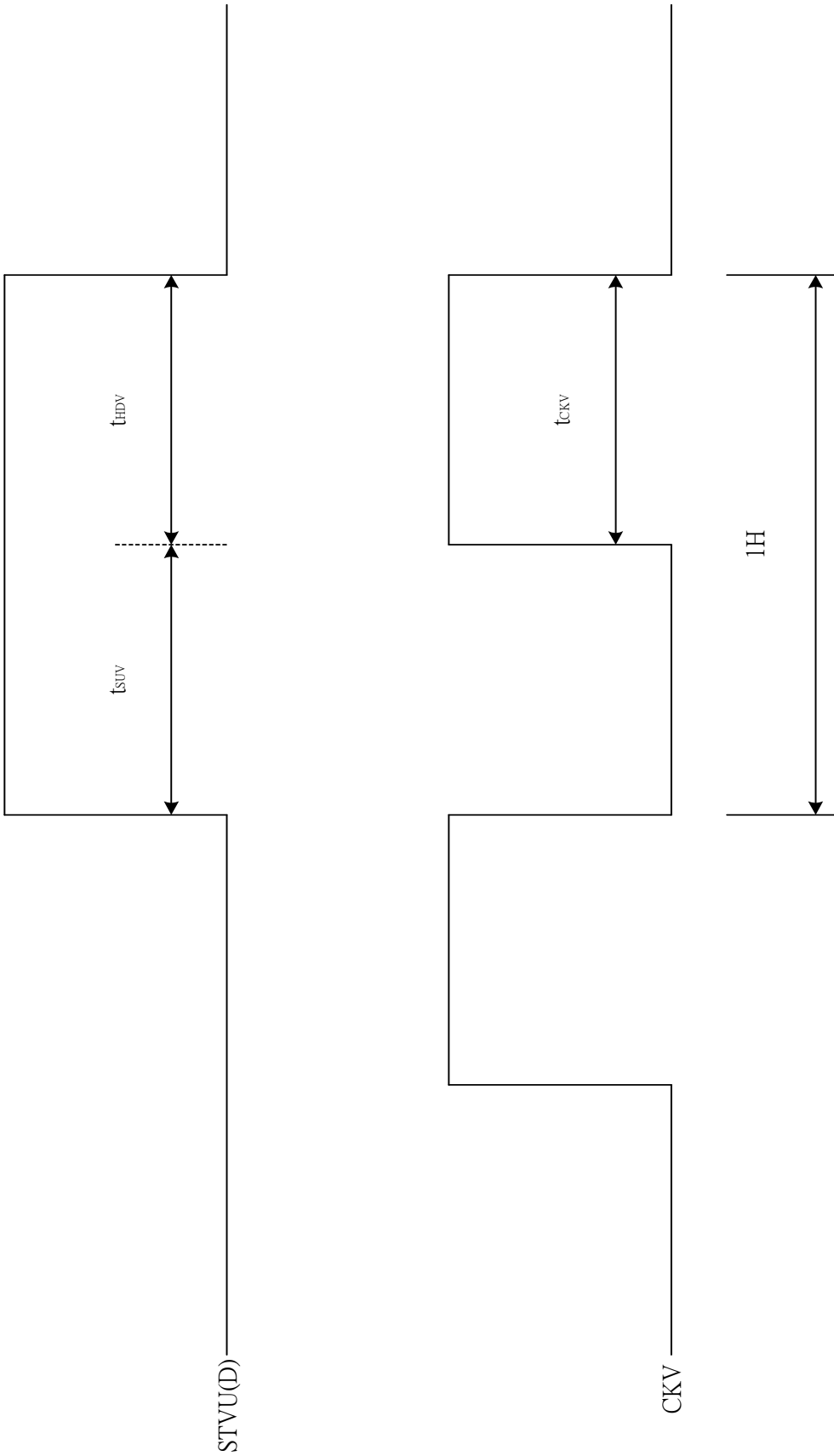


Fig. 8-4 Vertical shift clock timing

Vertical timing (From up to down)

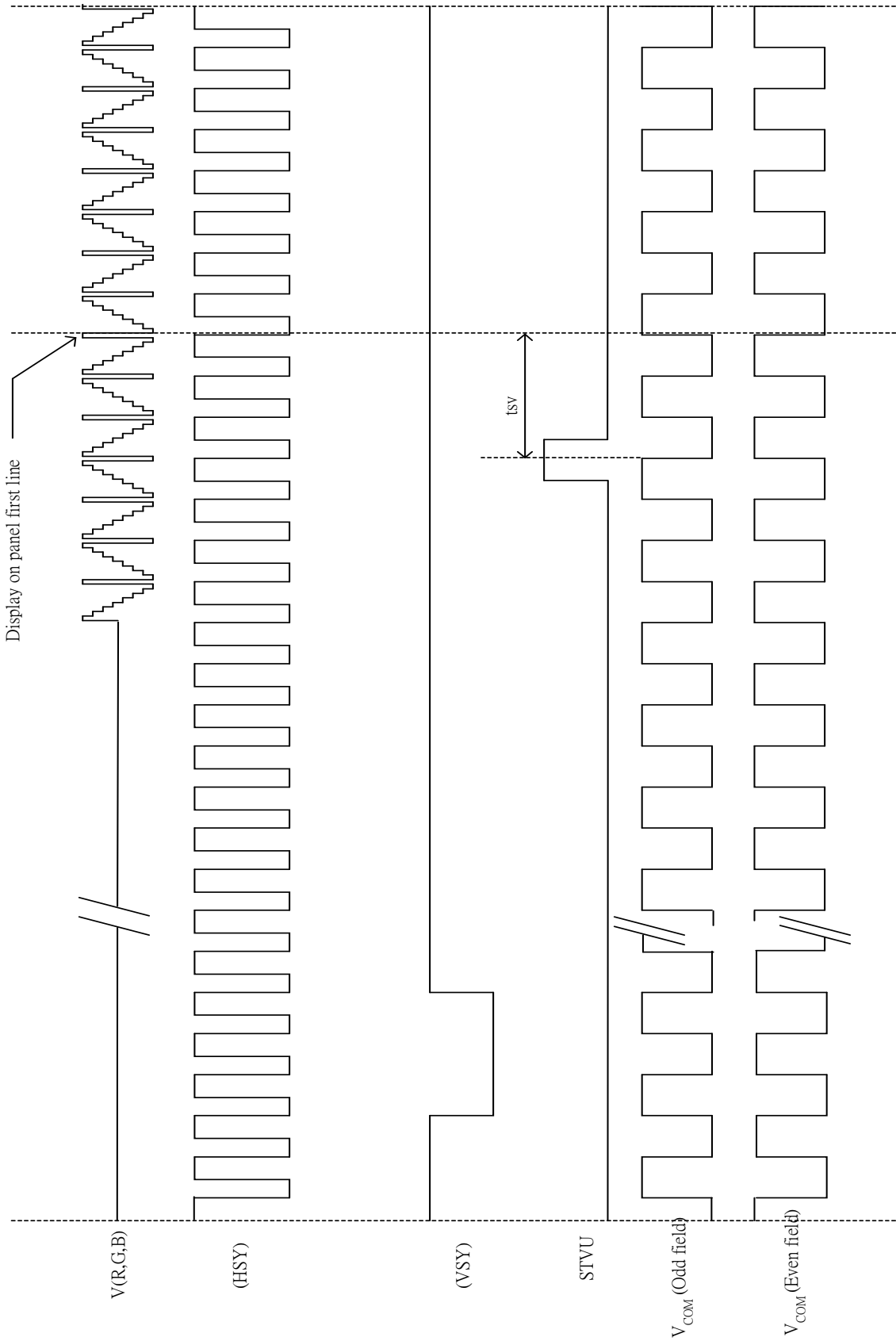


Fig. 8-5 (a) Vertical timing (From Up to Down)

Vertical timing (From down to up)

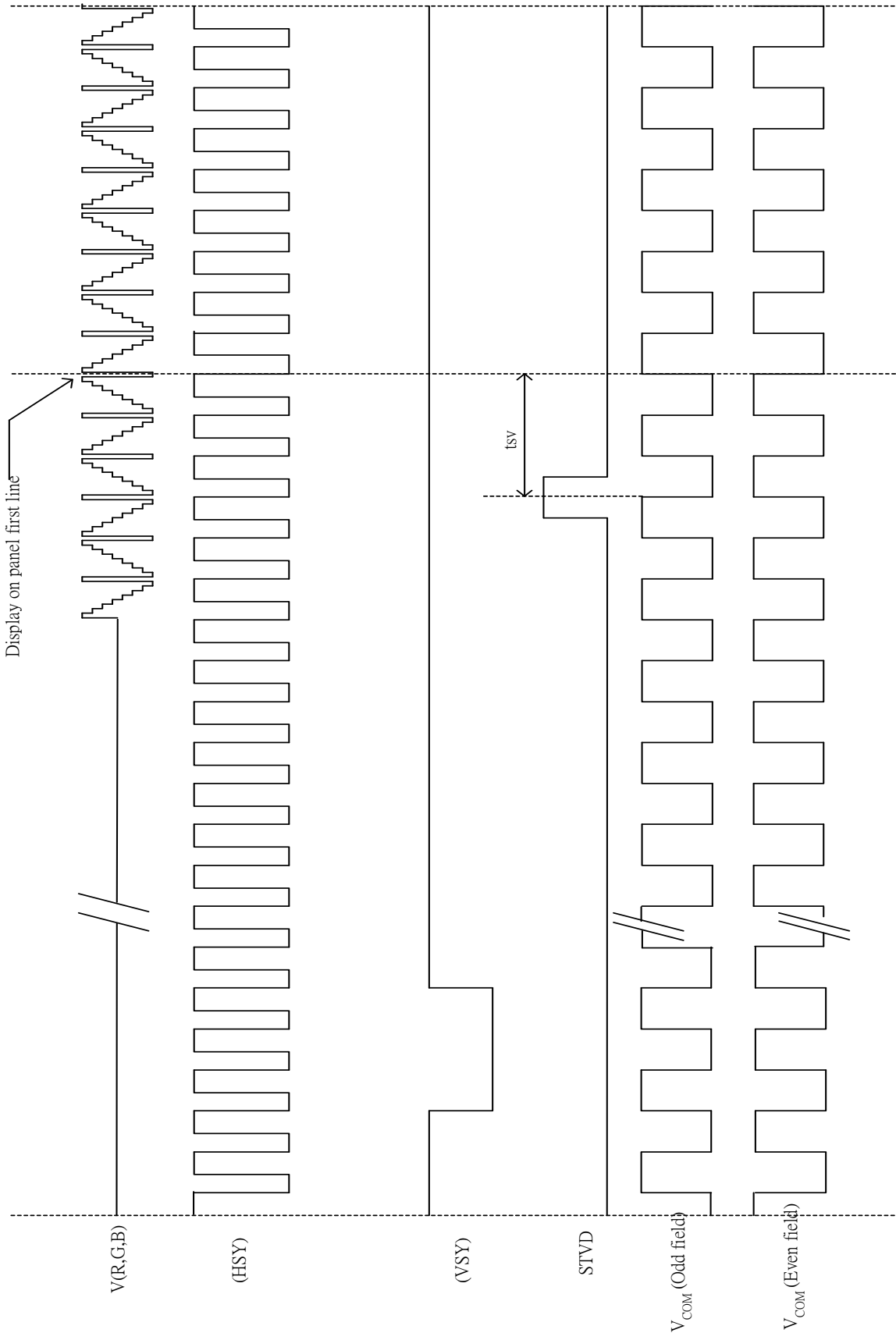
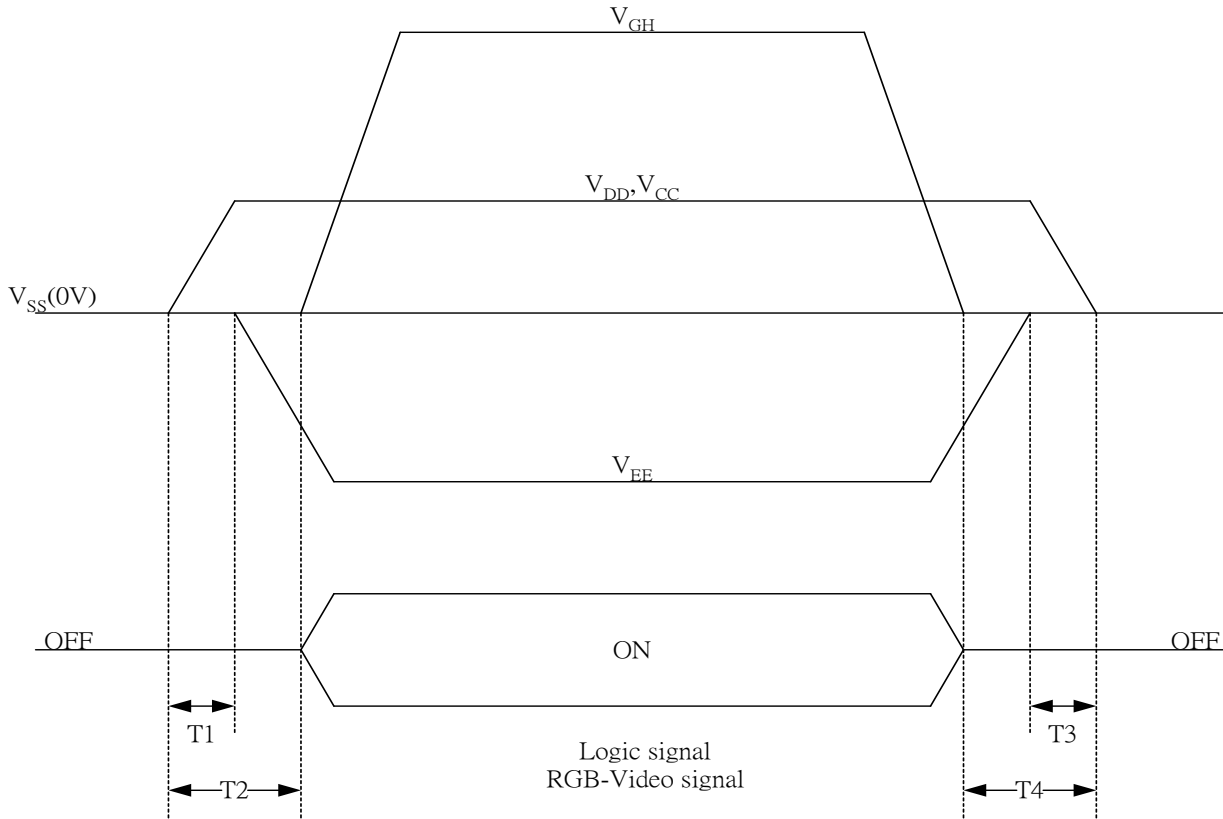


Fig. 8-5 (b) Vertical timing (From Down to Up)

9. Power on Sequence

The Power on Sequence only effect by V_{CC} , V_{SS} , V_{DD} , V_{EE} and V_{GH} , the others do not care.



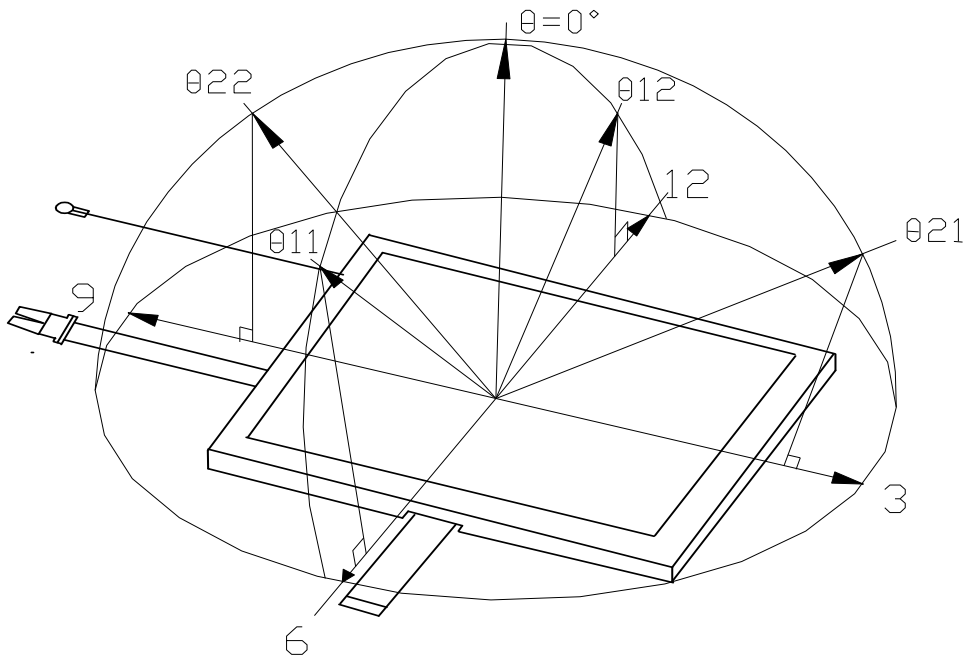
- 1) $10ms \leq T1 < T2$
- 2) $0ms < T3 \leq T4 \leq 10ms$

10. Optical Characteristics

10-1) Specification $T_a = 25^\circ C$

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	$\theta 21, \theta 22$	$CR \geq 10$	45	50		deg	Note 10-1
	Vertical	$\theta 12$		10	15		deg	
		$\theta 11$		30	35		deg	
Contrast Ratio		CR	At optimized Viewing angle	200	350			Note 10-2
Response time	Rise	T_r	$\theta = 0^\circ$		15	30	ms	Note 10-4
	Fall	T_f			25	50	ms	
Brightness		L	$\theta = 0^\circ$	300	350		cd/m^2	Note 10-3
White Chromaticity		x	$\theta = 0^\circ$	0.28	0.31	0.34		
		y		0.30	0.33	0.36		
Uniformity		U		70	75		%	Note 10-5
Lamp Life Time				20000	30000		hr	

Note 10-1 : The definitions of viewing angles



Note 10-2 : $CR = \frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

(Testing configuration see 8-2)

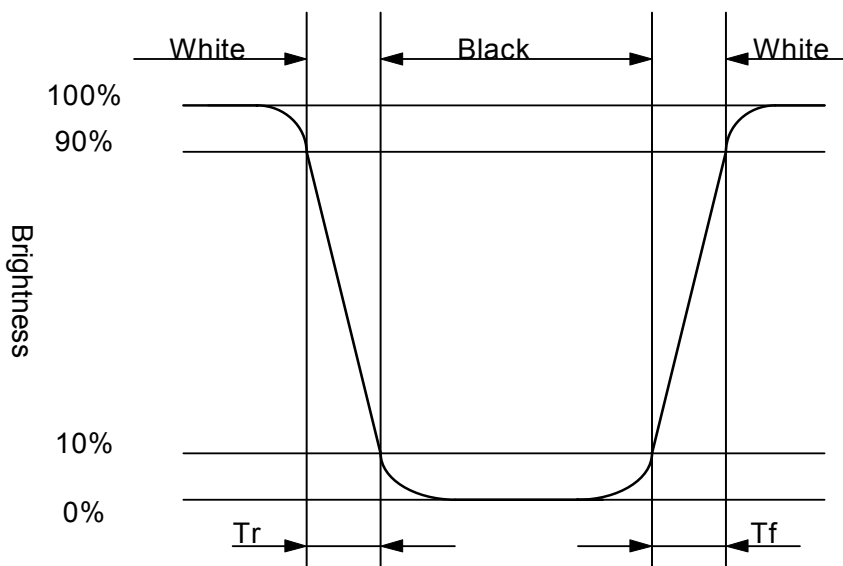
Contrast Ratio is measured in optimum common electrode voltage.

Note 10-3 : 1.Topcon BM-7(fast) luminance meter 1°field of view is used in the testing (after 20~30 minutes operation).

2.Lamp current : 6 mA

3.Inverter model : TDK-347.

Note 10-4 : The definition of response time:



Note 10-5 : The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

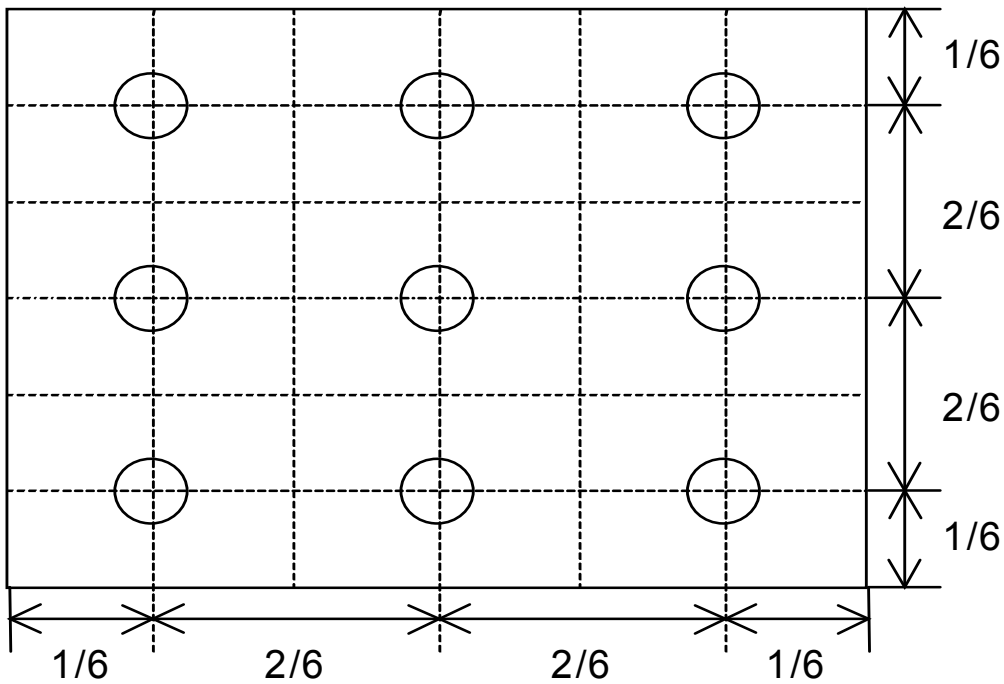
Luminance meter : BM-5A or BM-7 fast (TOPCON)

Measurement distance : 500 mm +/- 50 mm

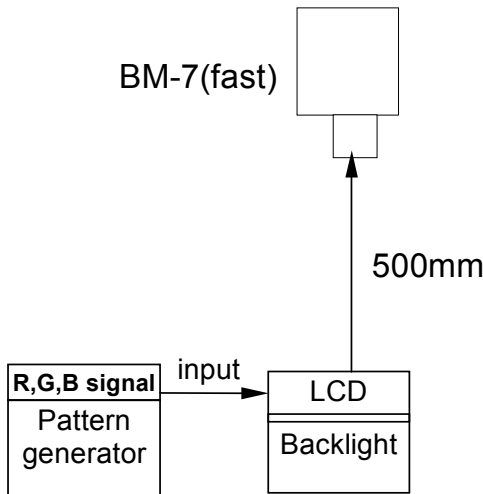
Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).

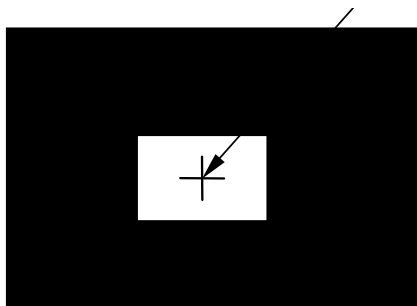


10-2) Testing configuration

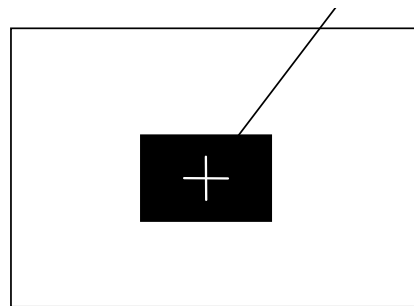


Caution: 1. Environmental illumination ≤ 1 lux
 2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display Testing Point Testing Point

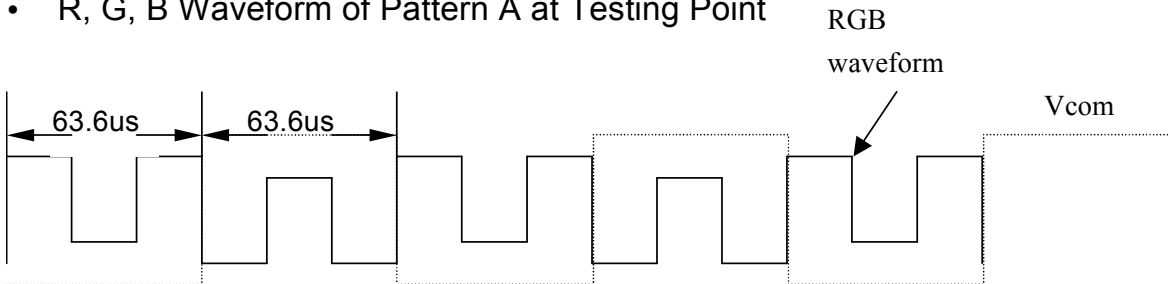


Pattern A

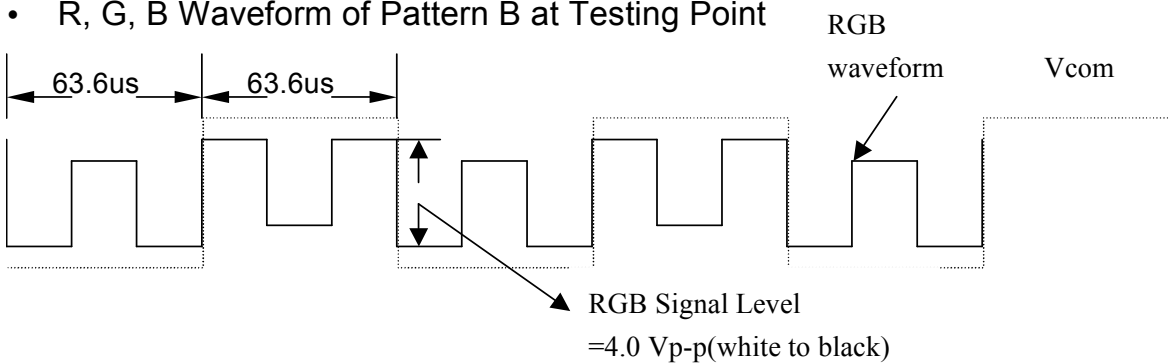


Pattern B

- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



11. Handling Cautions

11-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
 - 1.The noise from the backlight unit will increase.
 - 2.The output from inverter circuit will be unstable.
 - 3.In some cases a part of module will heat.
- c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

11-2) Precautions in mounting

- a) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- b) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- c) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

11-3) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.

12. Reliability Test

No.	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +70°C, 240 hrs
2	Low Temperature Storage Test	Ta = -20°C, 240 hrs
3	Low Temperature Operation Test	Ta = 0°C, 240 hrs
4	High Temperature & High Humidity Operation Test	Ta = +60°C, 90%RH, 240 hrs
5	Thermal Cycling Test (non-operating)	-20°C ↔ +70°C, 200Cycles 30 min 30 min
6	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz Amplitude : 1 mm Sweep time : 11 mins Test Period : 6 Cycles for each direction of X, Y, Z
7	Shock Test (non-operating)	100G, 6ms Direction : ±X, ±Y, ±Z Cycle : 3 times
8	Electrostatic Discharge Test (non-operating)	200pF, 0Ω ±200V 1 time / each terminal

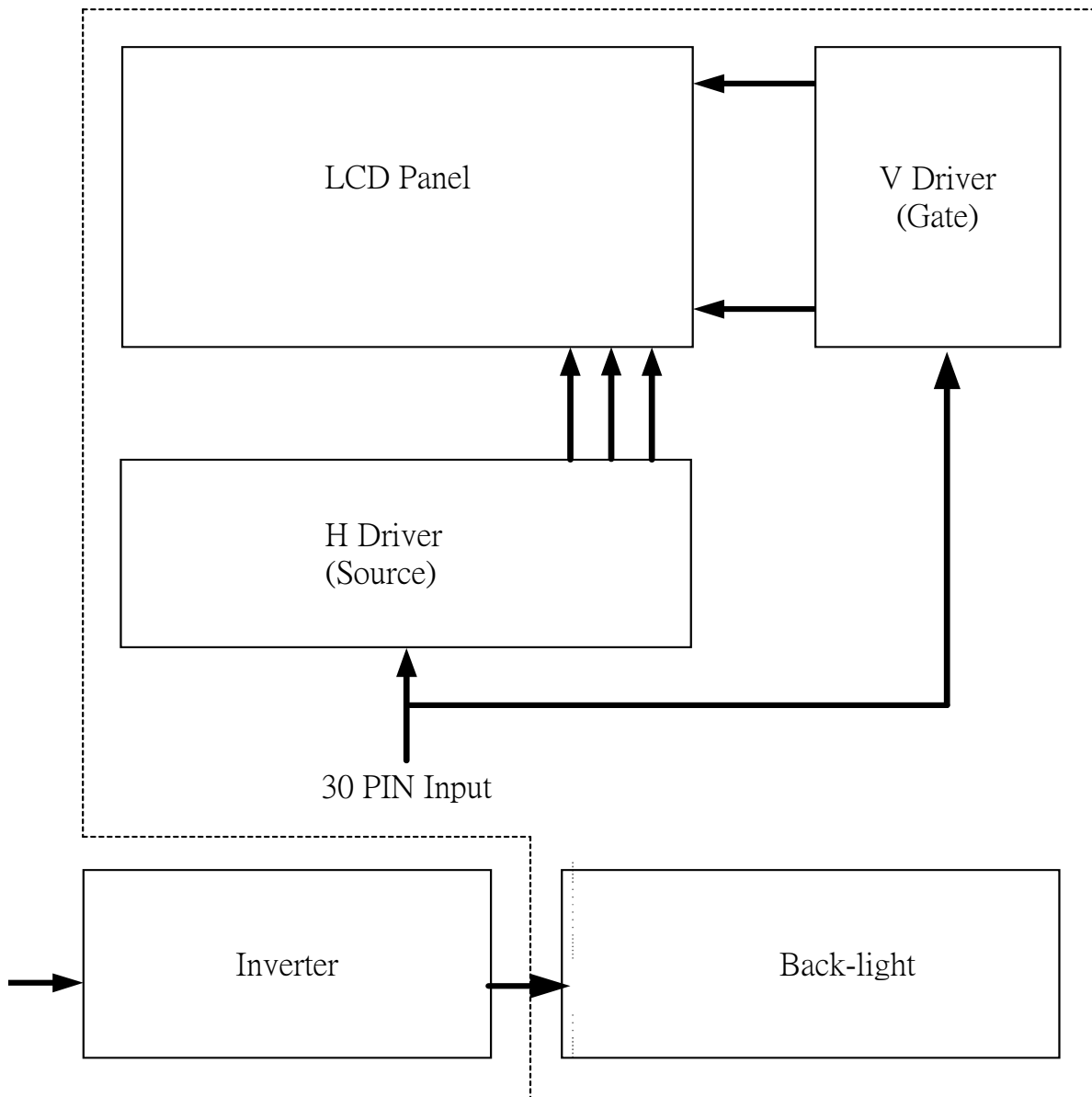
Ta: ambient temperature

Note : The protective film must be removed before temperature test.

[Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

13. Block Diagram



14. Packing

ZONE	REV.	DOCUMENT NO.	DESCRIPTION	DATE	REV. BY
<p>NOTE: 1. Q'TY: 20 pcs panel/carton. 2. Dimension: 530*295*230mm 3. Weight: 7.5 Kg</p>					
MTL.SPEC.		UNSPECIFIED TOL'S		REMARK	
		ANGLE			
		ROUGHNESS			
APPROVE		SCALE	UNIT	SHEET	DWG.TITLE
CHECK				1 of 1	PW080XU Module Packing Draw
DRAWN	Jimmyc	'05.04.28		MTL.NO.	DWG FILE:
				REV.	SIZE
				01	A4

Revision History

Rev.	Issued Date	Revised Contents
0.1	Apr. 14, 2005	Preliminary
0.2	Jun. 03, 2005	Modify: Page24: Packing