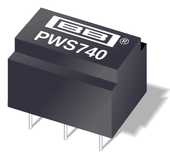
BURR - BROWN®



PWS740

Distributed Multi-Channel Isolated DC-TO-DC CONVERTER

FEATURES

- ISOLATED ±7 TO ±20VDC OUTPUTS
- BARRIER 100% TESTED AT 1500VAC, 60Hz
- LOWEST POSSIBLE COST PER CHANNEL
- MINIMUM PC BOARD SPACE
- 80% EFFICIENCY (8 CHANNELS, RATED LOADS)
- FLEXIBLE USE WITH PWS745 COMPONENTS

APPLICATIONS

- INDUSTRIAL MEASUREMENT AND CONTROL
- DATA ACQUISITION SYSTEMS
- TEST EQUIPMENT

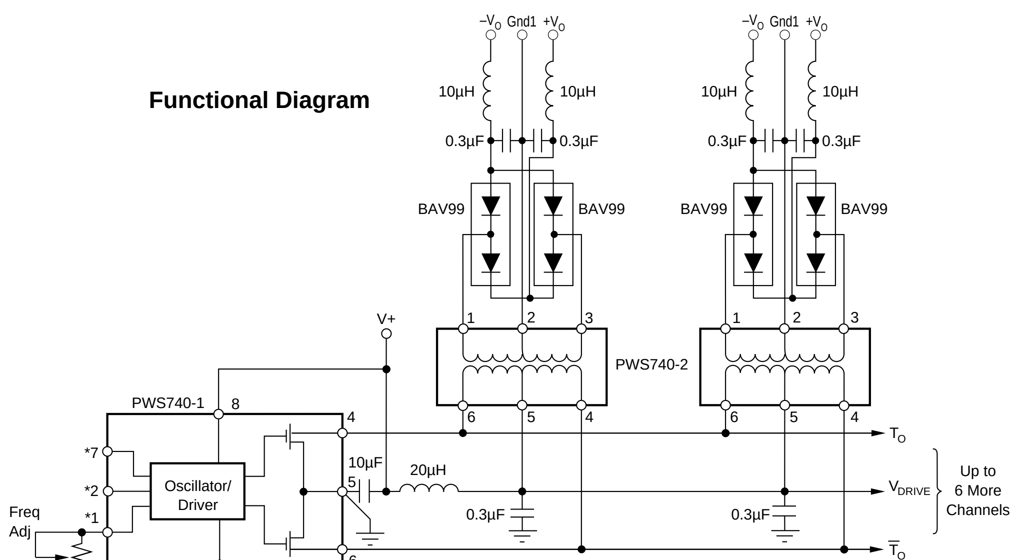
DESCRIPTION

The PWS740 is a multichannel, isolated DC-to-DC converter with a 1500VAC continuous isolation rating. The outputs track the input voltage to the converter over the range of 7 to 20VDC. The converter's modular design, comprising three components, minimizes the cost of isolated multichannel power for the user.

The PWS740-1 is a high-frequency (400kHz nominal) oscillator/driver, handling up to eight channels. This part is a hybrid containing an oscillator and two power FETs. It is supplied in a TO-3 case to provide the power dissipation necessary at full load. Transformer impedance limits the maximum input current to about 700mA at 15V input, well within the unit's thermal limits. A TTL-compatible ENABLE pin provides output shut-down if desired. A SYNC pin allows synchronization of several PWS740-1s.

The PWS740-2 is a trifilar-wound isolation transformer using a ferrite core and is encapsulated in a plastic package, allowing a higher isolation voltage rating. One PWS740-2 is used per isolated channel.

Functional Diagram



* Optional features; if unused, leave open.
** User Option

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-758H
Printed in U.S.A. January, 1998

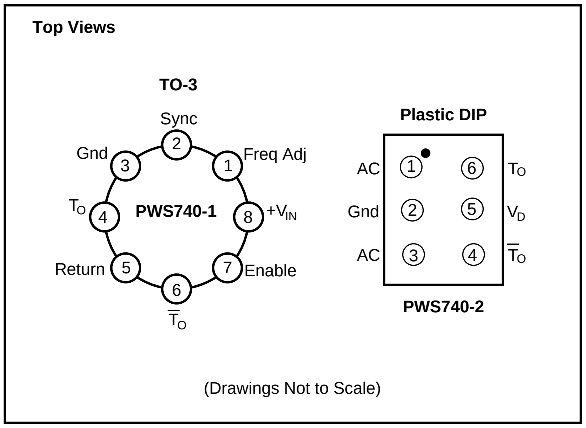
SPECIFICATIONS

ELECTRICAL

At V_{IN} = 15V, output load on each of 8 channels = ±15mA, T_A = +25°C, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
PWS740 SYSTEM					
ISOLATION					
Rated Voltage	Continuous, AC, 50/60Hz			1500	VACrms
	Continuous, DC			2121	VDC
Test Voltage	10s, minimum	4000			VACrms
Impedance	Measured from Pin 2 to Pin 5 of the PWS740-2		10^{12} || 3		Ω || pF
Leakage Current	240VACrms, 60Hz Per Channel		0.5	1.5	µA
INPUT					
Rated Voltage			15		VDC
Voltage Range		7		20	VDC
Current	±30mA Output Load on 8 Channels, V_{IN} = 15V		520		mA
	Rated Output Load on 8 Channels, V_{IN} = 15V		300		mA
Current Ripple	Full Output Load on 8 Channels, V_{IN} = 15V with π Filter on Input		1		mA
OUTPUT					
Rated Voltage	±15mA Output Load on 8 Channels	14	15	16	VDC
Voltage at Min Load	±1mA/Channel		30		VDC
Voltage Range	±15mA Output Load on Each Channel	±7		±20	VDC
V_{OUT} vs Temp	±15mA Output Load on Each Channel		±0.05		V/°C
Load Regulation	±3mA < Output Load < ±30mA		0.25		V/mA
Tracking Regulation	V_{OUT}/V_{IN}		1.2		V/V
Ripple Voltage	See Typical Performance Curves				
Noise Voltage	See Theory of Operation				
Current $\|+I_{OUT}\| + \|-I_{OUT}\|$	Each Channel			60	mA
TEMPERATURE					
Specification		–25		+85	°C
Operation		–25		+85	°C
PWS740-1 OSCILLATOR/DRIVER					
Frequency	V_{IN} = 15V	350	400	470	kHz
Supply		7	15	20	V
Enable	Drivers On	2		V_S	V
	Drivers Off	0		0.8	V
PWS740-2 ISOLATION TRANSFORMER					
Isolation Test Voltage	10s, minimum	4000			VACrms
	60s, minimum	1500			VACrms
Rated Isolation Voltage	Continuous			1500	VACrms
Isolation Impedance			10^{12} || 3		Ω || pF
Isolation Leakage	240VAC		0.5	1.5	µA
Primary Inductance	400kHz, Pin 1 to Pin 5		300		µH
Winding Ratio	Primary/Secondary		68/76		
DIODE BRIDGE SPECIFICATIONS					
Reverse Recovery	$I_F = I_R$ = 50mA		40		ns
Reverse Breakdown	I_R = 100µA	55			V
Reverse Current	V_R = 40V			1.5	µA
Forward Voltage	I_F = 100mA			1.8	V

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

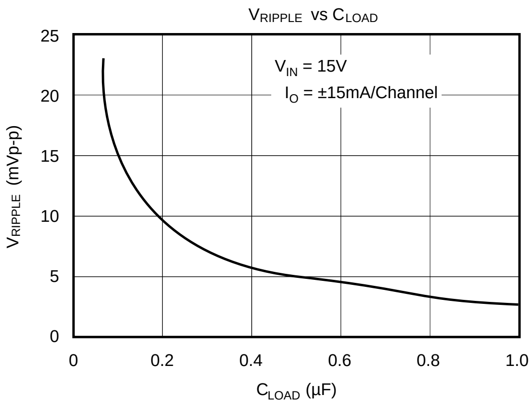
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

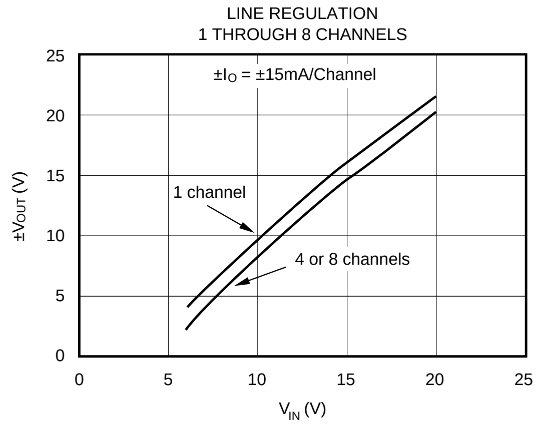
PACKAGE INFORMATION

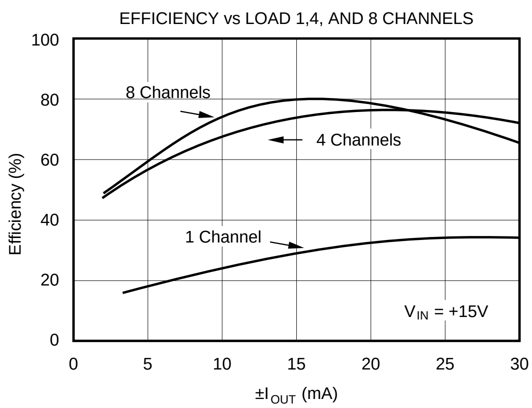
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
PWS740-1 Driver	TO-3	030
PWS740-2 Transformer	6-Pin Plastic DIP	216

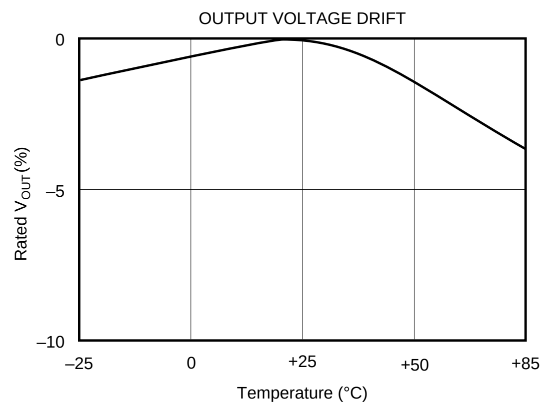
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

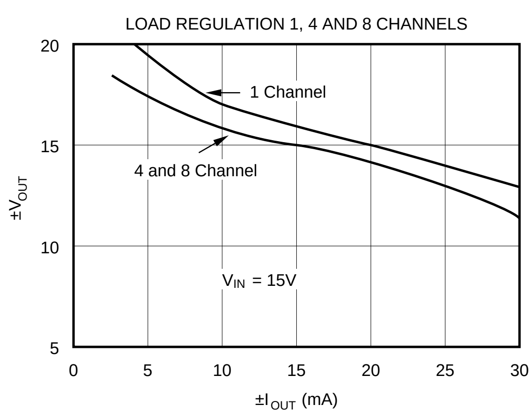
TYPICAL PERFORMANCE CURVES

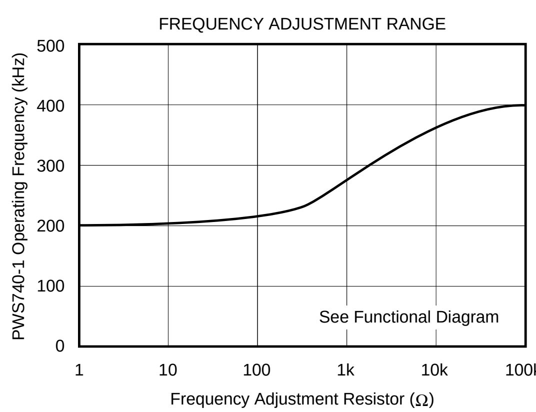












PIN DESCRIPTIONS OF PWS740-1 DRIVER

$+V_{IN}$, RETURN, AND GND

These are the power supply pins. The ground connection, RETURN, for the N-channel MOSFET sources is brought out separately from the ground connection for the oscillator/driver chip. The waveform of the FETs' ground return current (and also the current in the V_{DRIVE} line) is an 800kHz sawtooth. A capacitor between $+V_{IN}$ and the FET ground provides a bypass for the AC portion of this current.

The power should never be instantaneously interrupted to the PWS740 system (i.e., a break in the line from V+, either accidental or by means of a series switch). Normal power-down of the V+ supply is not considered instantaneous. Should a rapid break in input power occur, however, the transformers' voltage will rapidly increase to maintain current flow. Such a voltage spike may damage the PWS740-1. The bypass capacitors at the $+V_{IN}$ pin of the PWS740-1 and the V_{DRIVE} pins of the transformers provide a path for the primary current if power is interrupted; however, total protection requires some type of bidirectional 1A voltage clamping at the $+V_{IN}$ pin. A low cost SA20A TransZorb® from General Semiconductor[1] or equivalent, which will clamp the $+V_{IN}$ pin between –0.6V and +23V, is recommended.

T_O AND $\overline{T}_O$

These pins are the drains of the N-channel MOSFET switches which drive all the transformer primaries in parallel. The signals on these pins are 400kHz complementary square waves with twice the amplitude of the voltage at $+V_{IN}$. It is these lines that allow the power to be distributed to the individual high voltage isolation transformers. Without proper printed circuit board layout techniques, these lines could generate interference to analog circuits. See the next section on PCB layout.

ENABLE

A high TTL logic level on this pin activates the MOSFET driver circuitry. A low TTL level applied to the ENABLE pin shuts down all drive to the transformers and the output voltages go to zero (only the oscillator is unaffected). For continuous operation, the ENABLE pin can be left open or tied to a voltage between +2V and +V.

SYNCHRONIZATION

The SYNC pin is used to synchronize up to eight PWS740-1 oscillators. Synchronization is useful to prevent beat frequencies in the supply voltages. The SYNC pins of two or more PWS740-1s are tied together to force all units to the same frequency of oscillation. The resultant frequency is slightly higher than that of the highest unsynchronized unit. If this feature is not required, leave the SYNC pin open. The SYNC pin is sensitive to capacitance loading. 150pF or less is recommended. Also external parasitic capacitive feedback between either T_O and the SYNC pin can cause unstable operation (commonly seen as jitter in the T_O outputs). Keep SYNC connections and T_O lines as physically isolated as possible. Avoid shorting the SYNC pin directly to ground or supply potentials; otherwise, damage may result.

Figure 1 shows a method for synchronizing a greater number of PWS740-1 drivers. One unit is chosen as the master. Its synchronization signal, buffered by a high-speed unity gain amplifier can synchronize up to 20 slave units. Pin 1 of each slave unit must be grounded to assure synchronization. Minimize capacitive coupling between the buffered sync line and the outputs of the drivers, especially at the end of long lines. Capacitance to ground is not critical, but total stray capacitance between the sync line and switching outputs should be kept below 50pF. Where extreme line lengths are needed, such as between printed circuit boards, additional OPA633 buffers may be added to keep drive impedance at an acceptably low value. Because of temperature-influenced shifts in the switching levels, best operation of this circuit will occur when differences in ambient temperatures between the PWS740-1 drivers are minimized, typically within a 35°C range.

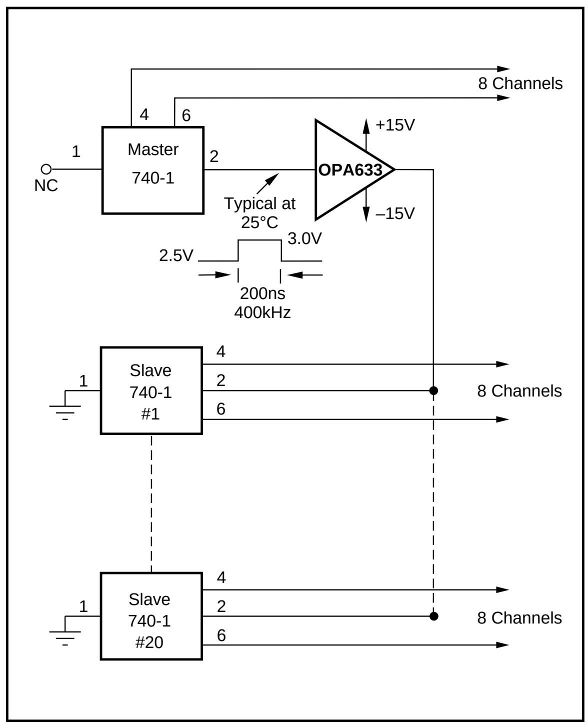


FIGURE 1. Master/Slave Synchronization of Multiple PWS740 Drivers.

(1) General Semiconductor Industries Inc., 2001 W. 10th Place, Tempe AZ 85281, 602-968-3101.

TransZorb® General Semiconductor Industries Inc.

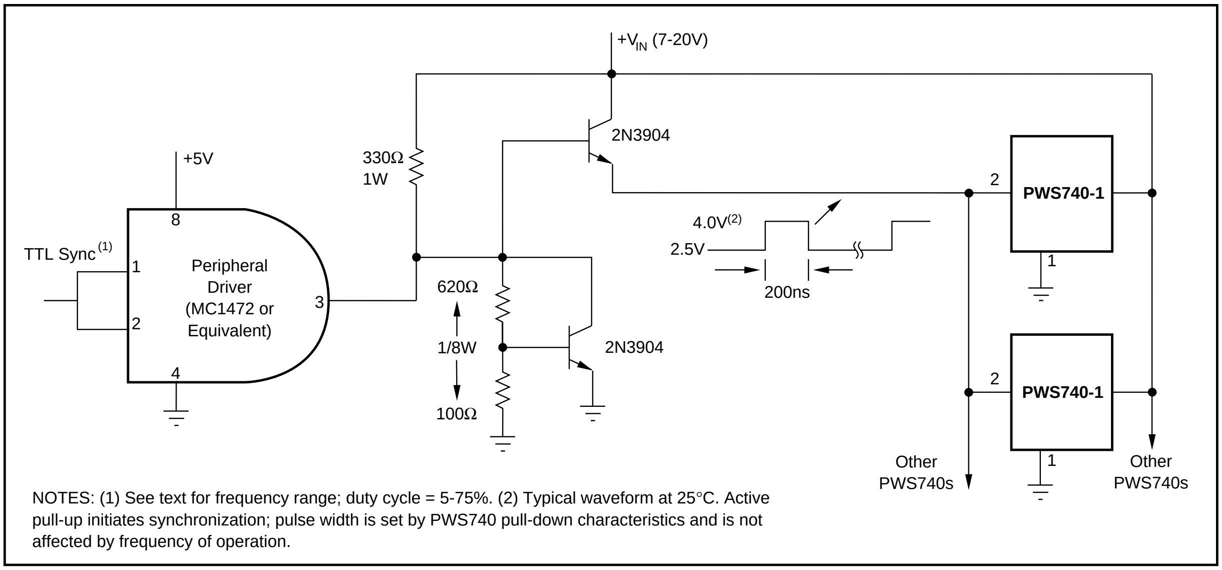


FIGURE 2. External Synchronization of Multiple PWS740 Drivers with TTL-Level Signals.

If larger temperature gradients are likely to occur, the user may wish to consider the synchronization method shown in Figure 2. This circuit is driven from an external TTL-compatible source such as a system clock or a simple free-running oscillator constructed of TTL gates. The output stage provides temperature compensation over the rated temperature range of the PWS740. The signal source frequency should be about 800kHz for rated performance, but may range from 500kHz to 2MHz with slightly reduced performance. Precautions with regard to circuit coupling and layout are the same as for the circuit of Figure 1. Repeaters using the OPA633 may be used for long line lengths. Symmetry and good high-frequency layout practice are important in successful application of both of these synchronization techniques.

FREQUENCY ADJUSTMENT

The FREQ ADJ pin may be connected to an external potentiometer to lower an unsynchronized PWS740-1 oscillator frequency. This may be useful if the frequency of the PWS740-1 is too close to some other signal's frequency in the system and beat interference is possible. See Typical Performance Curves. Use of this pin is not usually required; if not used, leave open for rated performance.

THEORY OF OPERATION

EXTERNAL FILTER COMPONENTS

Filter components are necessary to reduce the input ripple current and the output voltage noise. Without any input filtering, the sawtooth currents in the FET switches would flow in the +V supply line. Since this AC current can be as great as 1A peak, voltage interference with other components using this supply line would likely occur. The input ripple current can be reduced to approximately 1mA peak with the addition of two components—a bypass capacitor between the $+V_{IN}$ pin and ground, and a series inductor in the V_{DRIVE} line. A 10µF tantalum capacitor is adequate for bypass. A parallel 0.33µF ceramic capacitor will extend the bandwidth of the tantalum. Additional bypass capacitors at each primary center-tap of the transformers are recommended. In general, the higher the capacitance, the lower the ripple, but the parasitic series inductance of the bypass capacitors will eventually be the limiting factor. The inductor value recommended is approximately 20µH. Greater reduction in ripple current is achieved with values up to 100µH; then physical size may become a concern. The inductor should be rated for at least 2A and its DC resistance should be less than 0.1Ω. An example of a low cost indicator is part number 51591 from Pulse Engineering[2].

Output voltage filtering is achieved with a 0.33µF capacitor connecting each V_{OUT} pin of the diode bridge to ground. Short leads and close placement of the capacitors to the unit provide optimum high frequency bypassing. The 800kHz output ripple should be below 5mVp-p. Higher frequency noise bursts are also present at the outputs. They coincide with the switch times and are approximately 20mV in amplitude. Inductance of 10µH or less in series with the output loads will significantly reduce the noise as seen by the loads.

PC BOARD LAYOUT CONSIDERATIONS

Multilayer printed circuit boards are recommended for PWS740 systems. Two-layer boards are certainly possible with satisfactory operation; however, three layers provide greater density and better control of interference from the FET switch signals. Should four-layer boards be required for other circuitry, the use of separate layers for power and ground planes, a layer for switching signals, and a layer for analog signals would allow the most straightforward layout for the PWS740 system. The following discussion pertains to a three- or four-layer board layout.

(2) Pulse Engineering, PO Box 12235, San Diego CA 92112, 619-268-2400.

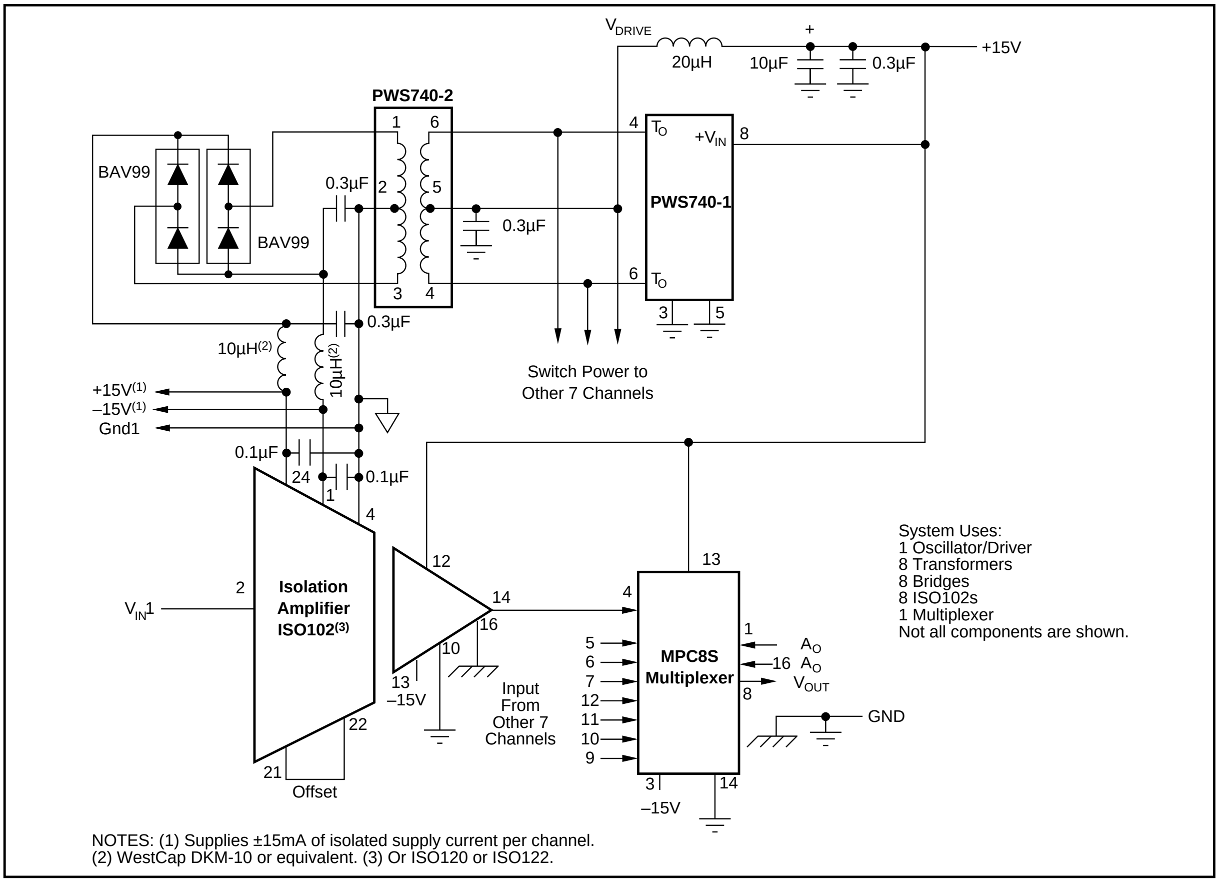


FIGURE 3. Low Cost Eight-Channel Isolation Amplifier Block with Channel-to-Channel Isolation.

Critical consideration should go to minimizing electromagnetic radiation from the switching signal's lines. T_O and $\overline{T}_O$. You can identify the path of the switching current by starting at the $+V_{IN}$ pin. The dynamic component of the current is supplied primarily from the bypass capacitor. The high frequency current flows through the inductor and down the V_{DRIVE} line, through one side of the transformer windings, returning in the T_O with the "on" FET switch, and then back up through the bypass capacitor. This current path defines a loop antenna which transmits magnetic energy. The magnetic field lines reinforce at the center of the loop, while the field lines reinforce at the center of the loop, while the field lines from opposite points of the loop oppose each other outside the loop. Cancellation of magnetic radiation occurs when the loop is collapsed to two tightly spaced parallel line segments, each carrying the same current in opposite directions. For this reason, the printed circuit traces for both T_O connections should lay directly over a power plane forming the V_{DRIVE} connection. This plane need not extend much wider than T_O and $\overline{T}_O$. All of the current in the plane will flow directly under the T_O traces because this is the path of least inductance (and least radiation).

Another potential problem with the T_O lines is electric field radiation. Fortunately, the V_{DRIVE} plane is effective at terminating most of the field lines because of its proximity to these lines. Additional shielding can be obtained by running ground trace(s) along the T_O lines, which also facilitate minimum loop area connections for the transformer's center tap bypass capacitors.

The connections between the secondary (output side) of the transformer and the diode bridges should be kept as short as possible. Unnecessary stray capacitance on these lines could cause tuned circuit peaking to occur, resulting in a slight increase of output voltage.

The PWS740 is intended for use with the ISO102, ISO120 or ISO122 isolation amplifiers (see Figure 3). Place the PWS740-2 transformer on the V_{OUT} side of the buffer rather than on the C_1 (bandwidth control) side to prevent possible pickup of switch signal by the ISO102.

The best ground connection ties the ISO102 output analog common pin to the PWS740-1 ground pin with a ground plane. This is where a four-layer board design becomes convenient. The digital ground of the ISO102 can be connected to the ground plane or closer to the +V supply. If possible, you should include the analog components that the ISO102 drives on the same board. For example, if several ISO102s are multiplexed to an analog/digital converter, then having all components sharing the same ground plane will significantly simplify ground errors. Avoid connecting digital ground and the PWS740 ground together locally, leaving the ISO102 analog ground to be connected off of the board; the differential voltage between analog and digital ground may become too great.

OUTPUT CURRENT RATINGS

The PWS740-1 driver contains "soft-start" driver circuitry to protect the driver FETs and eliminate high inrush currents during turn-on. Because the PWS740 can have between one and eight channels connected, it was not possible to provide a suitable internal current limit within the driver. Instead, impedance-limiting protects the driver and transformer from overload. This means that the internal impedance of each PWS740-2 transformer is high enough that, when short-circuited at its output, it limits the current drawn from the driver to a safe value. In addition, the wire size and mass of the transformer are large enough that the transformer does not receive damage under continuous short-circuit conditions.

The PWS740-1 is capable of driving up to eight individual channels to their full current rating. The total current which can be drawn from each isolation channel is a function of total power being drawn from both DC V+ and V– outputs. For example, if one output is not used, then maximum current can be drawn from the other output. In all cases, the maximum total current that can be drawn from any individual channel is:

$$| I_L + | + | I_L - | \leq 60\text{mA}$$

It should be noted that many analog circuit functions do not simultaneously draw full rated current from both the positive and negative supplies. Thus, the PWS740 can power more circuits per channel than is first apparent. For example, an operational amplifier does not draw maximum current from both supplies simultaneously. If a circuit draws 10mA from the positive supply and 3mA from the negative supply, the PWS740 could power (60 ÷ 13), about four devices per channel.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter period of time. The relationship between actual test conditions and the continuous derated maximum specification is an important one. Burr-Brown has chosen a deliberately conservative one: $V_{TEST} = (2 \times V_{CONTINUOUS\ RATING}) + 1000V$. This choice is appropriate for conditions where system transient voltages are not well defined.[3] Where the real voltages are well-defined or where the isolation voltage is not continuous, the user may choose a less conservative derating to establish a specification from the test voltage.

(3) Reference National Electrical Manufacturers Association (NEMA) Standards part ICS I-109 and ICS1-111.