PX1011A/PX1012A

PCI Express stand-alone X1 PHY

Rev. 02 — 18 May 2006 Product data sheet

1. General description

The PX1011A/PX1012A is a high-performance, low-power, single-lane PCI Express electrical PHYsical layer (PHY) that handles the low level PCI Express protocol and signaling. The PX1011A/1012A PCI Express PHY is compliant to the *PCI Express Base Specification, Rev. 1.0a*, and *Rev. 1.1*. The PX1011A/1012A includes features such as clock and data recovery (CDR), data serialization and de-serialization, 8b/10b encoding, analog buffers, elastic buffer and receiver detection, and provides superior performance to the Media Access Control (MAC) layer devices.

The PX1011A/1012A is a 2.5 Gbit/s PCI Express PHY with 8-bit data PXPIPE interface. Its PXPIPE interface is a superset of the PHY Interface for the PCI Express (PIPE) specification, enhanced and adapted for off-chip applications with the introduction of a source synchronous clock for transmit and receive data. The 8-bit data interface operates at 250 MHz with SSTL_2 signaling. The SSTL_2 signaling is compatible with the I/O interfaces available in FPGA products.

The PX1011A/1012A PCI Express PHY supports advanced power management functions. The PX1011AI/PX1012AI is for the industrial temperature range (–40 °C to +85 °C).

2. Features

2.1 PCI Express interface

- Compliant to *PCI Express Base Specification 1.1*
- Single PCI Express 2.5 Gbit/s lane
- Data and clock recovery from serial stream
- Serializer and De-serializer (SerDes)
- Receiver detection
- 8b/10b coding and decoding, elastic buffer and word alignment
- Supports loopback
- Supports direct disparity control for use in transmitting compliance pattern
- Supports lane polarity inversion
- Low jitter and Bit Error Rate (BER)

2.2 PHY/MAC interface

- Based on Intel PHY Interface for PCI Express architecture v1.0 (PIPE)
- Adapted for off-chip with additional synchronous clock signals (PXPIPE)
- 8-bit parallel data interface for transmit and receive at 250 MHz
- 2.5 V SSTL_2 class I signaling

2.3 JTAG interface

- JTAG (IEEE 1149.1) boundary scan interface
- Built-In Self Test (BIST) controller tests SerDes and I/O blocks at speed
- 3.3 V CMOS signaling

2.4 Power management

- Dissipates < 300 mW in L0 normal mode
- Support power management of L0, L0s and L1

2.5 Clock

- 100 MHz external reference clock with ±300 ppm tolerance
- Supports spread spectrum clock to reduce EMI
- On-chip reference clock termination

2.6 Miscellaneous

- LFBGA81 lead or lead free package
- Operating ambient temperature
  - Commercial: 0 °C to +70 °C
  - Industrial: –40 °C to +85 °C
- ESD protection voltage for Human Body Model (HBM): 2000 V

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDD1}	digital supply voltage 1	for JTAG I/O	3.0	3.3	3.6	V
V_{DDD2}	digital supply voltage 2	for SSTL_2 I/O	2.3	2.5	2.7	V
V_{DDD3}	digital supply voltage 3	for core	1.2	1.25	1.3	V
V_{DD}	supply voltage	for high-speed serial I/O and PVT	1.15	1.2	1.25	V
V_{DDA1}	analog supply voltage 1	for serializer	1.2	1.25	1.3	V
V_{DDA2}	analog supply voltage 2	for serializer	3.0	3.3	3.6	V
$f_{clk(ref)}$	reference clock frequency		99.97	100	100.03	MHz
T_{amb}	ambient temperature	operating				
		commercial	0	-	+70	°C
		industrial	–40	-	+85	°C

4. Ordering information

Table 2. Ordering information

Type number	Solder process	Package		
		Name	Description	Version
PX1011A-EL1	SnPb solder ball compound	LFBGA81	plastic low profile fine-pitch ball grid array package; 81 balls; body 9 × 9 × 1.05 mm	SOT643-1
PX1011A-EL1/G	Pb-free (SnAgCu solder ball compound)	LFBGA81	plastic low profile fine-pitch ball grid array package; 81 balls; body 9 × 9 × 1.05 mm	SOT643-1
PX1011AI-EL1/G	Pb-free (SnAgCu solder ball compound)	LFBGA81	plastic low profile fine-pitch ball grid array package; 81 balls; body 9 × 9 × 1.05 mm	SOT643-1
PX1012A-EL1/G	Pb-free (SnAgCu solder ball compound)	LFBGA81	plastic low profile fine-pitch ball grid array package; 81 balls; body 9 × 9 × 1.05 mm	SOT643-1
PX1012AI-EL1/G	Pb-free (SnAgCu solder ball compound)	LFBGA81	plastic low profile fine-pitch ball grid array package; 81 balls; body 9 × 9 × 1.05 mm	SOT643-1

5. Marking

Table 3. Leaded package marking

Line	Marking	Description
A	PX1011A-EL1	full basic type number
B	xxxxxxx	diffusion lot number
C	2PNyyww	manufacturing code: 2 = diffusion site P = assembly site N = leaded yy = year code ww = week code

Table 4. Lead-free package marking

Line	Marking	Description
A	PX1011A-EL1/G PX1012A-EL1/G PX1011AI-EL1/G[1] PX1012AI-EL1/G[1]	full basic type number
B	xxxxxxx	diffusion lot number
C	2PGyyww	manufacturing code: 2 = diffusion site P = assembly site G = lead-free yy = year code ww = week code

[1] Industrial temperature range.

6. Block diagram

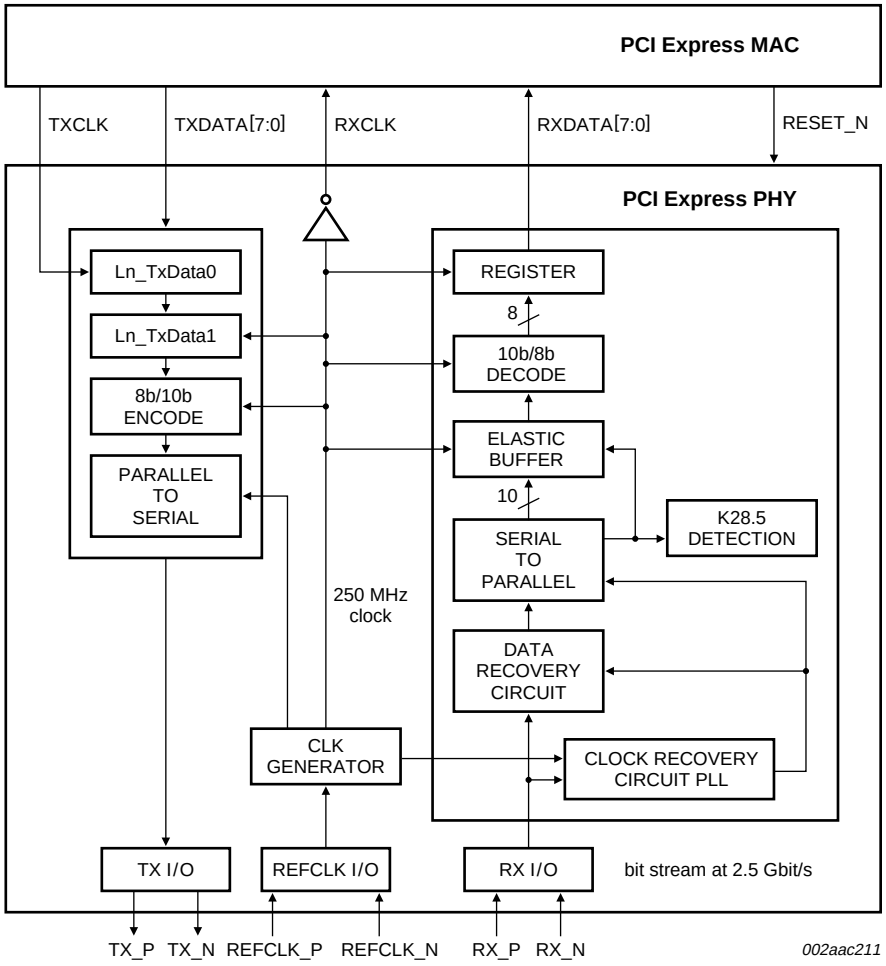
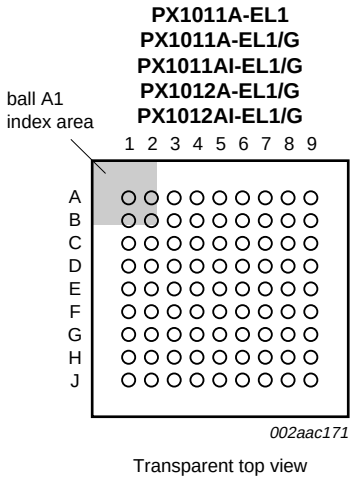


Fig 1. Block diagram

7. Pinning information

7.1 Pinning



Transparent top view

Fig 2. Pin configuration

	1	2	3	4	5	6	7	8	9
A	V_{SS}	RXIDLE	RXDATA6	RXDATA4	RXDATA3	RXDATA1	RXDATAK	RXCLK	RXSTATUS0
B	REFCLK_P	V_{SS}	RXDATA7	RXDATA5	V_{SS}	RXDATA2	RXDATA0	V_{SS}	RXSTATUS1
C	REFCLK_N	V_{SS}	V_{DDD2}	V_{SS}	V_{DDD2}	V_{SS}	V_{DDD2}	RXVALID	RXSTATUS2
D	V_{SS}	V_{SS}	V_{DD}	V_{DDA2}	V_{DDA1}	PVT	V_{SS}	PHYSTATUS	TXDATA0
E	RX_P	V_{SS}	V_{DDD1}	TMS	V_{DDD1}	V_{DDD3}	V_{DDD2}	V_{SS}	TXDATA1
F	RX_N	V_{SS}	TCK	TRST_N	V_{DDD3}	V_{DDD3}	V_{SS}	TXDATA3	TXDATA2
G	V_{SS}	V_{SS}	TDI	V_{SS}	V_{DDD2}	V_{SS}	V_{DDD2}	TXDATA5	TXDATA4
H	TX_P	V_{SS}	TDO	TXIDLE	V_{SS}	PWRDWN0	RXDET_LOOPB	V_{SS}	TXDATA6
J	TX_N	VREFS	RESET_N	RXPOL	TXCOMP	PWRDWN1	TXDATAK	TXCLK	TXDATA7

002aac210

Transparent top view.

Fig 3. Ball mapping

7.2 Pin description

The PHY input and output pins are described in Table 5 to Table 12. Note that input and output is defined from the perspective of the PHY. Thus a signal on a pin described as an output is driven by the PHY and a signal on a pin described as an input is received by the PHY. A basic description of each pin is provided.

Table 5. PCI Express serial data lines

Symbol	Pin	Type	Signaling	Description
RX_P	E1	input	PCIe I/O	differential input receive pair with 50 Ω on-chip termination
RX_N	F1	input	PCIe I/O	
TX_P	H1	output	PCIe I/O	differential output transmit pair with 50 Ω on-chip termination
TX_N	J1	output	PCIe I/O	

Table 6. PXPIPE interface transmit data signals

Symbol	Pin	Type	Signaling	Description
TXDATA[7:0]	J9, H9, G8, G9, F8, F9, E9, D9	input	SSTL_2	8-bit transmit data input from the MAC to the PHY
TXDATAK	J7	input	SSTL_2	selection input for the symbols of transmit data; LOW = data byte; HIGH = control byte

Table 7. PXPIPE interface receive data signals

Symbol	Pin	Type	Signaling	Description
RXDATA[7:0]	B3, A3, B4, A4, A5, B6, A6, B7	output	SSTL_2	8-bit receive data output from the PHY to the MAC
RXDATAK	A7	output	SSTL_2	selection output for the symbols of receive data; LOW = data byte; HIGH = control byte

Table 8. PXPIPE interface command signals

Symbol	Pin	Type	Signaling	Description
RXDET_ LOOPB	H7	input	SSTL_2	used to tell the PHY to begin a receiver detection operation or to begin loopback; LOW = reset state
TXIDLE	H4	input	SSTL_2	forces TX output to electrical idle. TXIDLE should be asserted while in power states P0s and P1.
TXCOMP	J5	input	SSTL_2	used when transmitting the compliance pattern; HIGH-level sets the running disparity to negative
RXPOL	J4	input	SSTL_2	signals the PHY to perform a polarity inversion on the receive data; LOW = PHY does no polarity inversion; HIGH = PHY does polarity inversion
RESET_N	J3	input	SSTL_2	PHY reset input; active LOW
PWRDWN0	H6	input	SSTL_2	transceiver power-up and power-down inputs (see Table 13); 0x2 = reset state
PWRDWN1	J6	input	SSTL_2	

Table 9. PXPIPE interface status signals

Symbol	Pin	Type	Signaling	Description
RXVALID	C8	output	SSTL_2	indicates symbol lock and valid data on RX_DATA and RX_DATAK
PHYSTATUS	D8	output	SSTL_2	used to communicate completion of several PHY functions including power management state transitions and receiver detection
RXIDLE	A2	output	SSTL_2	indicates receiver detection of an electrical idle; this is an asynchronous signal
RXSTATUS0	A9	output	SSTL_2	encodes receiver status and error codes for the received data stream and receiver detection (see Table 15)
RXSTATUS1	B9	output	SSTL_2	
RXSTATUS2	C9	output	SSTL_2	

Table 10. Clock and reference signals

Symbol	Pin	Type	Signaling	Description
TXCLK	J8	input	SSTL_2	source synchronous 250 MHz transmit clock input from MAC. All input data and signals to the PHY are synchronized to this clock.
RXCLK	A8	output	SSTL_2	source synchronous 250 MHz clock output for received data and status signals bound for the MAC.
REFCLK_P	B1	input	PCIe I/O	100 MHz reference clock input. This is the spread spectrum source clock for PCI Express. Differential pair input with 50 Ω on-chip termination.
REFCLK_N	C1	input	PCIe I/O	
PVT	D6	-	analog I/O	input or output to create a compensation signal internally that will adjust the I/O pads characteristics as PVT drifts. Connect to V_{DD} through a 49.9 Ω resistor.
VREFS	J2	input		reference voltage input for SSTL_2 class I signaling. Connect to 1.25 V.

Table 11. 3.3 V JTAG signals

Symbol	Pin	Type	Signaling	Description
TMS	E4	input	3.3 V CMOS	test mode select input
TRST_N	F4	input	3.3 V CMOS	test reset input for the JTAG interface; active LOW
TCK	F3	input	3.3 V CMOS	test clock input for the JTAG interface
TDI	G3	input	3.3 V CMOS	test data input
TDO	H3	output	3.3 V CMOS	test data output

Table 12. PCI Express PHY power supplies

Symbol	Pin	Type	Signaling	Description
V_{DDA1}	D5	power		1.25 V analog power supply for serializer and de-serializer
V_{DDA2}	D4	power		3.3 V analog power supply for serializer and de-serializer
V_{DDD1}	E3, E5	power		3.3 V power supply for JTAG I/O
V_{DDD2}	C3, C5, C7, E7, G5, G7	power		2.5 V power supply for SSTL_2 I/O
V_{DDD3}	E6, F5, F6	power		1.25 V power supply for core
V_{DD}	D3	power		1.2 V power supply for high-speed serial PCI Express I/O pads and PVT
V_{SS}	A1, B2, B5, B8, C2, C4, C6, D1, D2, D7, E2, E8, F2, F7, G1, G2, G4, G6, H2, H5, H8	ground		ground

8. Functional description

The main function of the PHY is to convert digital data into electrical signals and vice versa. The PCI Express PHY handles the low level PCI Express protocol and signaling. The PX1011A/1012A PCI Express PHY consists of the Physical Coding Sub-layer (PCS), a Serializer and De-serializer (SerDes) and a set of I/Os (pads). The PCI Express PHY handles the low level PCI Express protocol and signaling. This includes features such as Clock and Data Recovery (CDR), data serialization and de-serialization, 8b/10b encoding, analog buffers, elastic buffer and receiver detection.

The PXPIPE interface between the MAC and PX1011A/1012A is a superset of the PHY Interface for the PCI Express (PIPE) specification. The following feature have been added:

- Source synchronous clocks for RX and TX data to simplify timing closure.

The 8-bit data width PXPIPE interface operates at 250 MHz with SSTL_2 class I signaling. Px1011A/1012A does not integrate SSTL_2 termination resistors inside the IC.

The PCI Express link consists of a differential input pair and a differential output pair. The data rate of these signals is 2.5 Gbit/s.

8.1 Receiving data

Incoming data enters the chip at the RX interface. The receiver converts these signals from small amplitude differential signals into rail-to-rail digital signals. The carrier detect circuit detects whether data is present on the line and passes this information through to the SerDes and PCS.

If a valid stream of data is present the Clock and Data Recovery unit (CDR) first recovers the clock from the data and then uses this clock for re-timing the data (i.e., recovering the data).

The de-serializer or Serial-to-Parallel converter (S2P) de-serializes this data into 10-bits parallel data.

Since the S2P has no knowledge about the data, the word alignment is still random. This is fixed in the digital domain by the PCS block. It first detects a 10-bit comma character (K28.5) from the random data stream and aligns the bits. Then it converts the 10-bit raw data into 8-bit words using 8b/10b decoding. An elastic buffer and FIFO brings the resulting data to the right clock domain, which is the RX source synchronous clock domain.

8.2 Transmitting data

When the PHY transmits, it receives 8-bit data from the MAC. This data is encoded using an 8b/10b encoding algorithm. The 2 bits overhead of the 8b/10b encoding ensures the serial data will be DC-balanced and has a sufficient 0-to-1 and 1-to-0 transition density for clock recovery at the receiver side.

The serializer or Parallel-to-Serial converter (P2S) serializes the 10 bits data into serial data streams. These data streams are latched into the transmitter, where they are converted into small amplitude differential signals. The transmitter has built-in de-emphasis for a larger eye opening at the receiver side.

The PLL has a sufficiently high bandwidth to handle a 100 MHz reference clock with a 30 kHz to 33 kHz spread spectrum.

8.3 Clocking

There are three clock signals used by the PX1011A/1012A:

- REFCLK is a 100 MHz external reference clock that the PHY uses to generate the 250 MHz data clock and the internal bit rate clock. This clock may have 30 kHz to 33 kHz spread spectrum modulation.
- TXCLK is a reference clock that the PHY uses to clock the TXDATA and command. This source synchronous clock is provided by the MAC. The PHY expects that the rising edge of TXCLK is centered to the data. The TXCLK has to be synchronous with RXCLK.
- RXCLK is a source synchronous clock provided by the PHY. The RXDATA and status signals are synchronous to this clock. The PHY aligns the rising edge of RXCLK to the center of the data. RXCLK may be used by the MAC to clock its internal logic.

8.4 Reset

The PHY must be held in reset until power and REFCLK are stable. It takes the PHY 64 μs maximum to stabilize its internal clocks. RXCLK frequency is the same as REFCLK frequency, 100 MHz, during this time. The PHY de-asserts PHYSTATUS when internal clocks are stable.

The PIPE specification recommends that while RESET_N is asserted, the MAC should have RXDET_LOOPB de-asserted, TXIDLE asserted, TXCOMP de-asserted, RXPOL de-asserted and power state P1. The MAC can also assert a reset if it receives a physical layer reset packet.

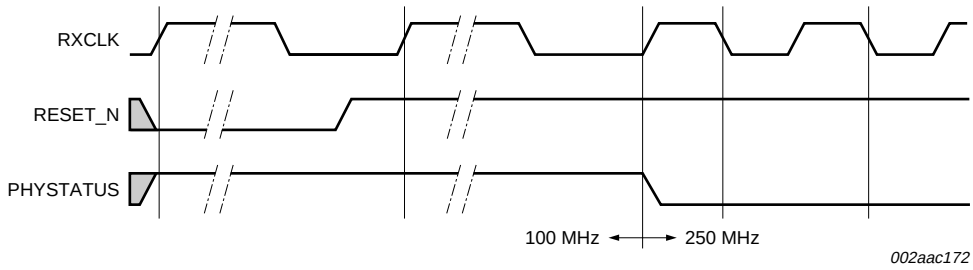


Fig 4. Reset

8.5 Power management

The power management signals allow the PHY to manage power consumption. The PHY meets all timing constraints provided in the PCI Express base specification regarding clock recovery and link training for the various power states.

Four power states are defined: P0, P0s, P1 and P2. P0 state is the normal operational state for the PHY. When directed from P0 to a lower power state, the PHY can immediately take whatever power saving measures are appropriate.

In states P0, P0s and P1, the PHY keeps internal clocks operational. For all state transitions between these three states, the PHY indicates successful transition into the designated power state by a single cycle assertion of PHYSTATUS. For all power state transitions, the MAC must not begin any operational sequences or further power state transitions until the PHY has indicated that the initial state transition is completed. TXIDLE should be asserted while in power states P0s and P1.

- **P0 state:** All internal clocks in the PHY are operational. P0 is the only state where the PHY transmits and receives PCI Express signaling. P0 is the appropriate PHY power management state for most states in the Link Training and Status State Machine (LTSSM). Exceptions are listed for each lower power PHY state (P0s, P1 and P2).
- **P0s state**: The MAC will move the PHY to this state only when the transmit channel is idle.

While the PHY is in either P0 or P0s power states, if the receiver is detecting an electrical idle, the receiver portion of the PHY can take appropriate power saving measures. Note that the PHY is capable of obtaining bit and symbol lock within the PHY-specified time (N_FTS with or without common clock) upon resumption of signaling on the receive channel. This requirement only applies if the receiver had previously been bit and symbol locked while in P0 or P0s states.

- **P1 state**: Selected internal clocks in the PHY are turned off. The MAC will move the PHY to this state only when both transmit and receive channels are idle. The PHY indicates a successful entry into P1 (by asserting PHYSTATUS). P1 should be used for the disabled state, all detect states, and L1.idle state of the Link Training and Status State Machine (LTSSM).
- **P2 state**: PHY will enter P1 instead.

Table 13. Summary of power management state

PWRDWN[1:0]	Power management state	Transmitter	Receiver	TX PLL	RXCLK	RX PLL/CDR
00b	P0, normal operation	on[1]	on	on	on	on
01b	P0s, power saving state	idle[2]	idle	on	on	on
10b	P1, lower power state	idle[2]	idle	on	on	off
11b	illegal, PHY will enter P1	-	-	-	-	-

[1] TXIDLE = 0

[2] TXIDLE = 1

8.6 Receiver detect

When the PHY is in the P1 state, it can be instructed to perform a receiver detection operation to determine if there is a receiver at the other end of the link. Basic operation of receiver detection is that the MAC requests the PHY to do a receiver detect sequence by asserting RXDET_LOOPB. When the PHY has completed the receiver detect sequence, it drives the RXSTATUS signals to the value of 011b if a receiver is present, and to 000b if there is no receiver. Then the PHY will assert PHYSTATUS to indicate the completion of receiver detect operation. The MAC uses the rising edge of PHYSTATUS to sample the RXSTATUS signals and then de-asserts RXDET_LOOPB. A few cycles after the RXDET_LOOPB de-asserts, the PHYSTATUS is also de-asserted.

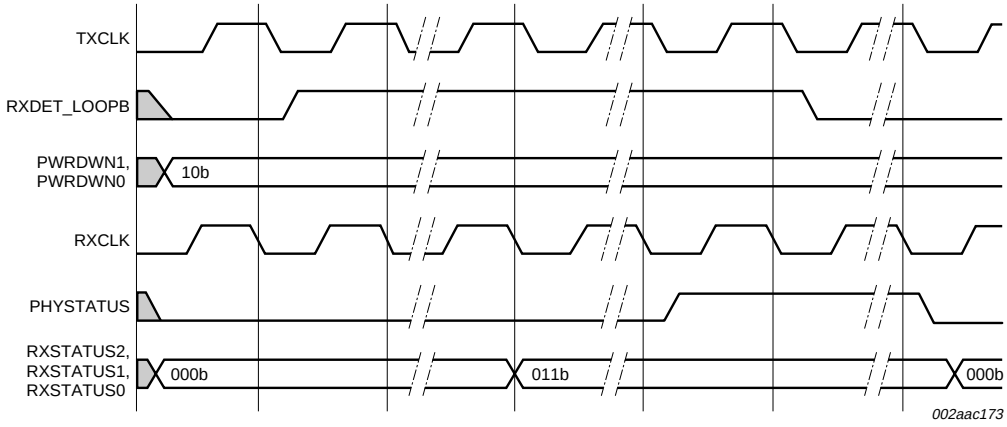


Fig 5. Receiver detect - receiver present

8.7 Loopback

The PHY supports an internal loopback from the PCI Express receiver to the transmitter with the following characteristics.

The PHY retransmits each 10-bit data and control symbol exactly as received, without applying scrambling or descrambling or disparity corrections, with the following rules:

- If a received 10-bit symbol is determined to be an invalid 10-bit code (i.e., no legal translation to a control or data value possible), the PHY still retransmits the symbol exactly as it was received.
- If a SKP ordered set retransmission requires adding a SKP symbol to accommodate timing tolerance correction, any disparity can be chosen for the SKP symbol.

- The PHY continues to provide the received data on the PXPIPE interface, behaving exactly like normal data reception.
- The PHY transitions from normal transmission of data from the PXPIPE interface to looping back the received data at a symbol boundary.

The PHY begins to loopback data when the MAC asserts RXDET_LOOPB while doing normal data transmission. The PHY stops transmitting data from the PXPIPE interface, and begins to loopback received symbols. While doing loopback, the PHY continues to present received data on the PXPIPE interface.

The PHY stops looping back received data when the MAC de-asserts RXDET_LOOPB. Transmission of data on the parallel interface begins immediately.

The timing diagram of Figure 6 shows example timing for beginning loopback. In this example, the receiver is receiving a repeating stream of bytes, Rx-a through Rx-z. Similarly, the MAC is causing the PHY to transmit a repeating stream of bytes Tx-a through Tx-z. When the MAC asserts RXDET_LOOPB to the PHY, the PHY begins to loopback the received data to the differential TX_P and TX_N lines.

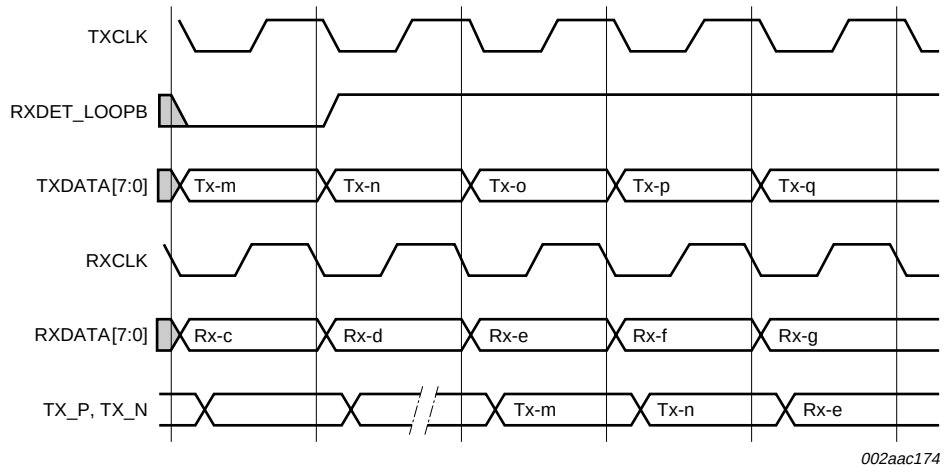


Fig 6. Loopback start

The timing diagram of Figure 7 shows an example of switching from loopback mode to normal mode. As soon as the MAC detects an electrical idle ordered-set, the MAC de-asserts RXDET_LOOPB, asserts TXIDLE and changes the POWERDOWN signals to state P1.

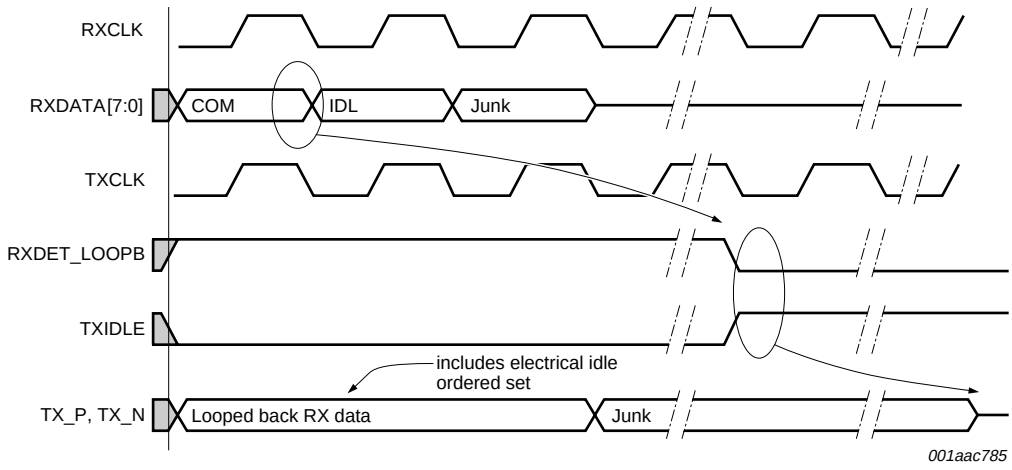


Fig 7. Loopback end

8.8 Electrical idle

The PCI Express Base Specification requires that devices send an Electrical Idle ordered-set before TX goes to the electrical idle state.

The timing diagram of Figure 8 shows an example of timing for entering electrical idle.

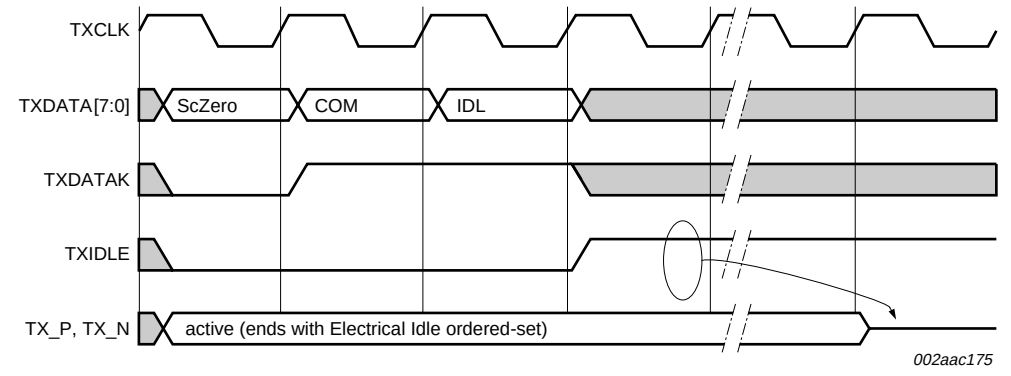


Fig 8. Electrical Idle

Table 14 summarizes the function of some PXPIPE control signals.

Table 14. Control signals function summary

PWRDWN[1:0]	RXDET_LOOPB	TXIDLE	Function description
P0: 00b	0	0	normal operation
	0	1	transmitter in idle
	1	0	loopback mode
	1	1	illegal
P0s: 01b	X	0	illegal
		1	transmitter in idle
P1: 10b	X	0	illegal
	0	1	transmitter in idle
	1	1	receiver detect

8.9 Clock tolerance compensation

The PHY receiver contains an elastic buffer used to compensate for differences in frequencies between bit rates at the two ends of a link. The elastic buffer is capable of holding at least seven symbols to handle worst case differences (600 ppm) in frequency and worst case intervals between SKP ordered-sets. The PHY is responsible for inserting or removing SKP symbols in the received data stream to avoid elastic buffer overflow or underflow. The PHY monitors the receive data stream, and when a Skip ordered-set is received, the PHY can add or remove one SKP symbol from each SKP ordered-set as appropriate to manage its elastic buffer. Whenever a SKP symbol is added or removed, the PHY will signal this to the MAC using the RXSTATUS signals. These signals have a non-zero value for one clock cycle and indicate whether a SKP symbol was added or removed from the received SKP ordered-set. RXSTATUS should be asserted during the clock cycle when the COM symbol of the SKP ordered-set is moved across the parallel interface. If the removal of a SKP symbol causes no SKP symbols to be transferred across the parallel interface, then RXSTATUS is asserted at the same time that the COM symbol (that was part of the received skip ordered-set) is transmitted across the parallel interface.

Figure 9 shows a sequence where the PHY inserted a SKP symbol in the data stream.

Figure 10 shows a sequence where the PHY removed a SKP symbol from a SKP ordered-set.

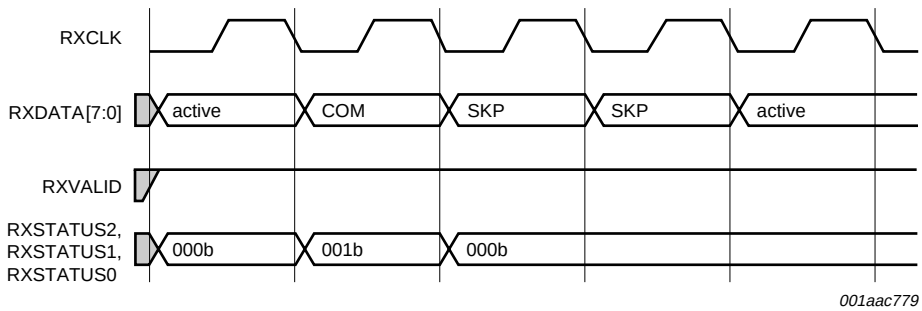


Fig 9. Clock correction - insert a SKP

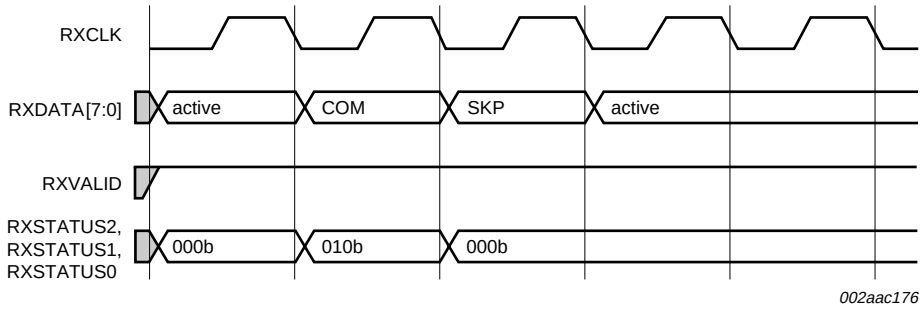


Fig 10. Clock correction - remove a SKP

8.10 Error detection

The PHY is responsible for detecting receive errors of several types. These errors are signaled to the MAC layer using the receiver status signals RXSTATUS.

Table 15. Function table PXPIPE status interface signals

Operating mode	Output pin		
	RXSTATUS2	RXSTATUS1	RXSTATUS0
Received data OK	L	L	L
One SKP added	L	L	H
One SKP removed	L	H	L
Receiver detected	L	H	H
8b/10b decode error	H	L	L
Elastic buffer overflow	H	L	H
Elastic buffer underflow	H	H	L
Receive disparity error	H	H	H

Because of higher level error detection mechanisms (like CRC) built into the data link layer of PCI Express, there is no need to specifically identify symbols with errors. However, timing information about when the error occurred in the data stream is important. When a receive error occurs, the appropriate error code is asserted for one clock cycle at the point closest to where the error actually occurred.

There are four error conditions that can be encoded on the RXSTATUS signals. If more than one error should happen to occur on a received byte, the errors are signaled with the priority shown below.

1. 8b/10b decode error
2. Elastic buffer overflow
3. Elastic buffer underflow
4. Disparity error

8.10.1 8b/10b decode errors

For a detected 8b/10b decode error, the PHY places an EDB (EnD Bad) symbol in the data stream in place of the bad byte, and encodes RXSTATUS with a decode error during the clock cycle when the effected byte is transferred across the parallel interface. In Figure 11 the receiver is receiving a stream of bytes Rx-a through Rx-z, and byte Rx-c has an 8b/10b decode error. In place of that byte, the PHY places an EDB on the parallel interface, and sets RXSTATUS to the 8b/10b decode error code. Note that a byte that cannot be decoded may also have bad disparity, but the 8b/10b error has precedence.

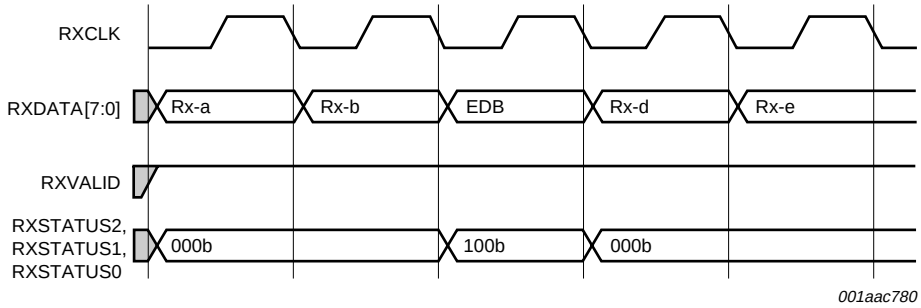


Fig 11. 8b/10b decode errors

8.10.2 Disparity errors

For a detected disparity error, the PHY asserts RXSTATUS with the disparity error code during the clock cycle when the effected byte is transferred across the parallel interface. In Figure 12 the receiver detected a disparity error on Rx-c data byte, and indicates this with the assertion of RXSTATUS.

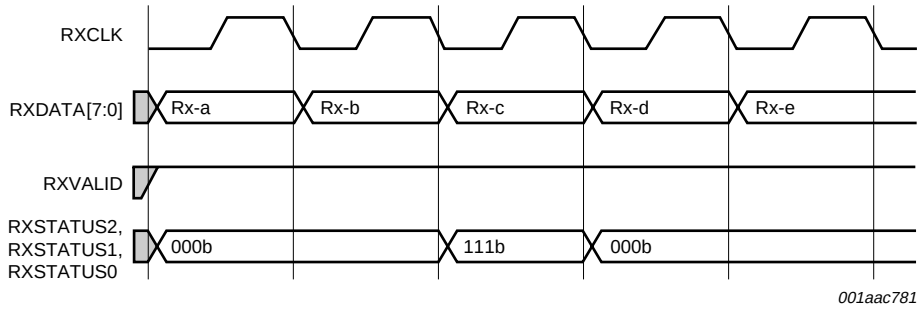


Fig 12. Disparity errors

8.10.3 Elastic buffer

For elastic buffer errors, an underflow is signaled during the clock cycle when the spurious symbol is moved across the parallel interface. The symbol moved across the interface is the EDB symbol. In the timing diagram Figure 13, the PHY is receiving a repeating set of symbols Rx-a through Rx-z. The elastic buffer underflow causing the EDB symbol to be inserted between the Rx-c and Rx-d symbols. The PHY drives RXSTATUS to indicate buffer underflow during the clock cycle when the EDB is presented on the parallel interface.

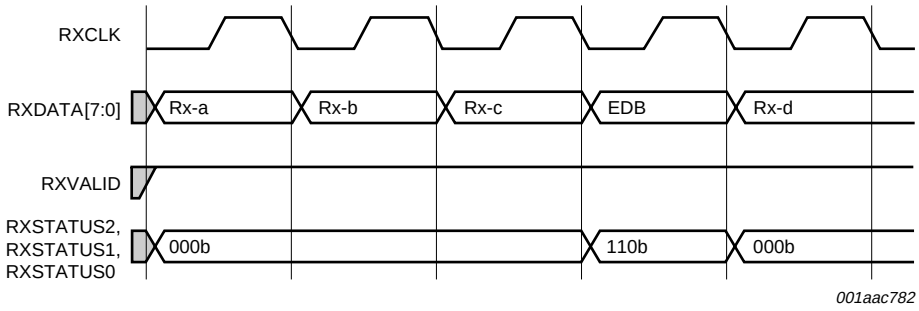


Fig 13. Elastic buffer underflow

For an elastic buffer overflow, the overflow is signaled during the clock cycle where the dropped symbol would have appeared in the data stream. In the timing diagram of Figure 14, the PHY is receiving a repeating set of symbols Rx-a through Rx-z. The elastic buffer overflows causing the symbol Rx-d to be discarded. The PHY drives RXSTATUS to indicate buffer overflow during the clock cycle when Rx-d would have appeared on the parallel interface.

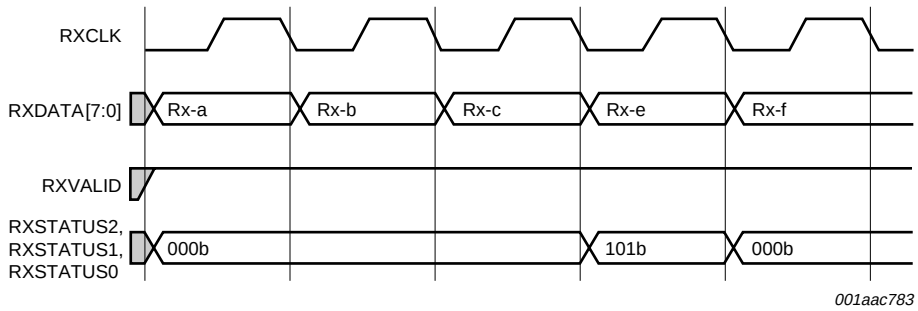


Fig 14. Elastic buffer overflow

8.11 Polarity inversion

To support lane polarity inversion, the PHY inverts received data when RXPOL is asserted. The PHY begins data inversion within 20 symbols after RXPOL is asserted.

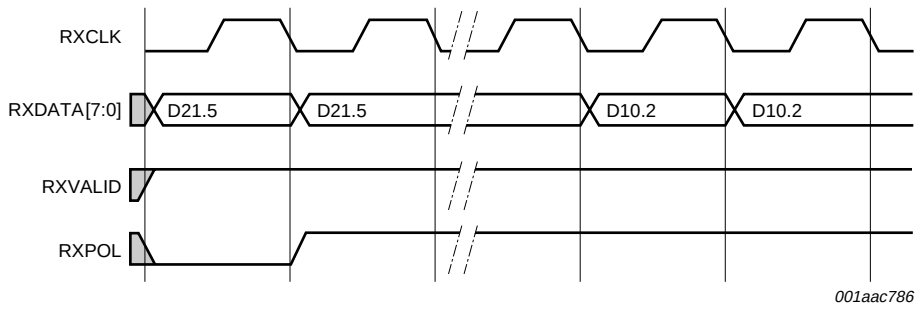


Fig 15. Polarity inversion

8.12 Setting negative disparity

To set the running disparity to negative, the MAC asserts TXCOMP for one clock cycle that matches with the data that is to be transmitted with negative disparity.

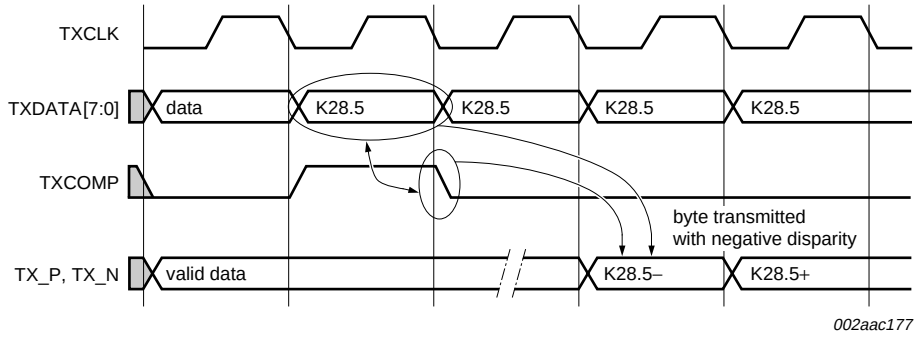


Fig 16. Setting negative disparity

8.13 JTAG boundary scan interface

Joint Test Action Group (JTAG) or IEEE 1149.1 is a standard, specifying how to control and monitor the pins of compliant devices on a printed-circuit board. This standard is commonly known as ‘JTAG Boundary Scan’.

This standard defines a 5-pin serial protocol for accessing and controlling the signal levels on the pins of a digital circuit, and has some extensions for testing the internal circuitry on the chip itself, which is beyond the scope of this data sheet.

Access to the JTAG interface is provided to the customer for the sole purpose of using boundary scan for interconnect test verification between other compliant devices that may reside on the board. Using JTAG for purposes other than boundary scan may produce undesired effects.

The JTAG interface is a 3.3 V CMOS signaling. JTAG TRST_N must be asserted LOW for normal device operation. If JTAG is not planned to be used, it is recommended to pull down TRST_N to V_{SS}.

9. Limiting values

Table 16. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDD1}	digital supply voltage 1	for JTAG I/O		–0.5	+4.6	V
V_{DDD2}	digital supply voltage 2	for SSTL_2 I/O		–0.5	+3.75	V
V_{DDD3}	digital supply voltage 3	for core		–0.5	+1.7	V
V_{DD}	supply voltage	for high-speed serial I/O and PVT		–0.5	+1.7	V
V_{DDA1}	analog supply voltage 1	for serializer		–0.5	+1.7	V
V_{DDA2}	analog supply voltage 2	for serializer		–0.5	+4.6	V
V_{esd}	electrostatic discharge voltage	HBM	[1]	-	2000	V
		CDM	[2]	-	500	V
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–55	+125	°C
T_{amb}	ambient temperature	operating				
		commercial		0	+70	°C
		industrial		–40	+85	°C

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged Device Model: ANSI/EOS/ESD-S5.3.1-1999, standard for ESD sensitivity testing, Charged Device Model - component level; Electrostatic Discharge Association, Rome, NY, USA.

10. Thermal characteristics

Table 17. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	44	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air	[1]	10	K/W

[1] Significant variations can be expected due to system variables, such as adjacent devices, or actual air flow across the package.

11. Characteristics

Table 18. PCI Express PHY characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDD1}	digital supply voltage 1	for JTAG I/O	3.0	3.3	3.6	V
V_{DDD2}	digital supply voltage 2	for SSTL_2 I/O	2.3	2.5	2.7	V
V_{DDD3}	digital supply voltage 3	for core	1.2	1.25	1.3	V
V_{DD}	supply voltage	for high-speed serial I/O and PVT	1.15	1.2	1.25	V
V_{DDA1}	analog supply voltage 1	for serializer	1.2	1.25	1.3	V
V_{DDA2}	analog supply voltage 2	for serializer	3.0	3.3	3.6	V
I_{DDD1}	digital supply current 1	for I/O	0.1	1	2	mA
I_{DDD2}	digital supply current 2	for SSTL_2; no load	10	18	25	mA
I_{DDD3}	digital supply current 3	for core	5	10	15	mA
I_{DD}	supply current	for high-speed serial I/O and PVT	15	20	25	mA
I_{DDA1}	analog supply current 1	for serializer	15	20	25	mA
I_{DDA2}	analog supply current 2	for serializer	7	10	15	mA
Receiver						
UI	unit interval		399.88	400	400.12	ps
$V_{RX\_DIFFp\text{-}p}$	differential input peak-to-peak voltage		0.175	-	1.2	V
$t_{RX\_MAX\_JITTER}$	maximum receiver jitter time		-	-	0.6	UI
$V_{IDLE\_DET\_DIFFp\text{-}p}$	electrical idle detect threshold		65	-	175	mV
Z_{RX_DC}	DC input impedance		40	50	60	Ω
$Z_{RX\_HIGH\_IMP\_DC}$	powered-down DC input impedance		200	-	-	kΩ
RL_{RX_DIFF}	differential return loss		15	-	-	dB
RL_{RX_CM}	common mode return loss		6	-	-	dB
$f_{clk(ref)}$	reference clock frequency		99.97	100	100.03	MHz
$\Delta f_{mod(clk)(ref)}$	reference clock modulation frequency range		–0.5	-	+0	%
$f_{mod(clk)(ref)}$	reference clock modulation frequency		30	-	33	kHz
$V_{IH(se)REFCLK}$	REFCLK single-end HIGH-level input voltage		-	0.7	-	V
$V_{IL(se)REFCLK}$	REFCLK single-end LOW-level input voltage		-	0	-	V
$t_{lock(CDR)(ref)}$	CDR lock time (reference loop)		-	-	50	µs
$t_{lock(CDR)(data)}$	CDR lock time (data loop)		-	-	2.5	µs
$t_{RX\_latency}$	receiver latency	1 clock cycle is 4 ns	6	-	13	clock cycle

Table 18. PCI Express PHY characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transmitter						
UI	unit interval		399.88	400	400.12	ps
$V_{TX\_DIFFp\text{-}p}$	differential peak-to-peak output voltage		0.8		1.2	V
$t_{TX\_EYE\_m\text{-}mJITTER}$	maximum time between the jitter median and maximum deviation from the median		-	40	60	ps
$t_{TX\_JITTER\_MAX}$	maximum transmitter jitter time		-	70	120	ps
$V_{TX\_DE\_RATIO}$	de-emphasized differential output voltage ratio		–3.0		–4.0	dB
t_{TX_RISE}	D+/D– TX output rise time		60	70	80	ps
t_{TX_FALL}	D+/D– TX output fall time		60	70	80	ps
$V_{TX\_CM\_ACp}$	RMS AC peak common mode output voltage		-	-	20	mV
$\Delta V_{CM\_DC\_ACT\_IDLE}$	absolute delta of DC common mode voltage during L0 and electrical idle		0	-	100	mV
$\Delta V_{CM\_DC\_LINE}$	absolute delta of DC common mode voltage between D+ and D–		0	-	25	mV
$V_{TX\_CM\_DC}$	TX DC common mode voltage		0	-	3.6	V
I_{TX_SHORT}	TX short-circuit current limit		-	20	90	mA
RL_{TX_DIFF}	differential return loss		12	-	-	dB
RL_{TX_CM}	common mode return loss		6	-	-	dB
Z_{TX_DC}	transmitter DC impedance		40	50	60	Ω
C_{TX}	AC coupling capacitor		75	100	200	nF
$t_{lock(PLL)}$	PLL lock time		-	-	50	µs
$t_{TX\_latency}$	transmitter latency	1 clock cycle is 4 ns	4	-	9	clock cycle
$t_{P0s\_exit\_latency}$	P0s state exit latency		-	-	2.5	µs
$t_{P1\_exit\_latency}$	P1 state exit latency		-	-	64	µs
$t_{RESET\text{-}PHYSTATUS}$	RESET_N HIGH to PHYSTATUS LOW time		-	-	64	µs

Table 19. PXPIPE characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RXCLK}	RXCLK frequency		249.925	250	250.075	MHz
f_{TXCLK}	TXCLK frequency		249.925	250	250.075	MHz
V_{VREFS}	voltage on pin VREFS	[1]	-	1.25	-	V
$V_{OH(SSTL2)}$	SSTL_2 HIGH-level output voltage	V_{TT} = 1.25 V	1.82	-	-	V
$V_{OL(SSTL2)}$	SSTL_2 LOW-level output voltage	V_{TT} = 1.25 V	-	-	0.68	V
$V_{IH(SSTL2)}$	SSTL_2 HIGH-level input voltage	V_{TT} = 1.25 V	1.63	-	-	V
$V_{IL(SSTL2)}$	SSTL_2 LOW-level input voltage	V_{TT} = 1.25 V	-	-	0.87	V
Input signals; measured with respect to TXCLK						
$t_{su(TX)(PXPIPE)}$	setup time of PXPIPE input signal	see Figure 17	500	-	-	ps
$t_{h(TX)(PXPIPE)}$	hold time of PXPIPE input signal	see Figure 17	500	-	-	ps
Output signals; measured with respect to RXCLK						
$t_{su(RX)(PXPIPE)}$	setup time of PXPIPE output signal	see Figure 17	1500	-	-	ps
$t_{h(RX)(PXPIPE)}$	hold time of PXPIPE output signal	see Figure 17	1500	-	-	ps

[1] Reference voltage for SSTL_2 class I I/O.

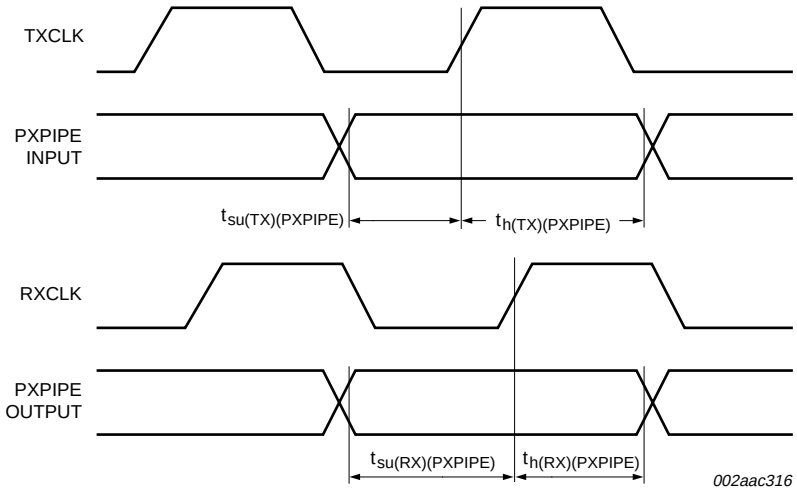
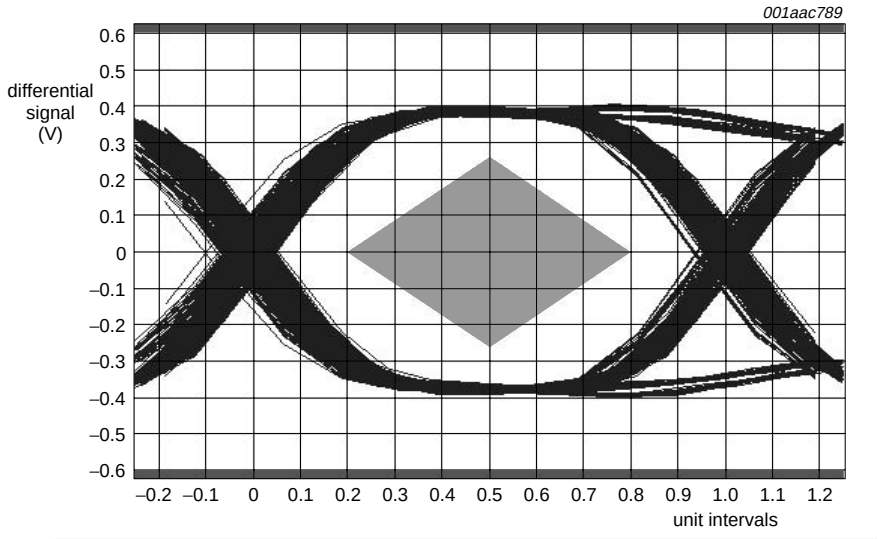
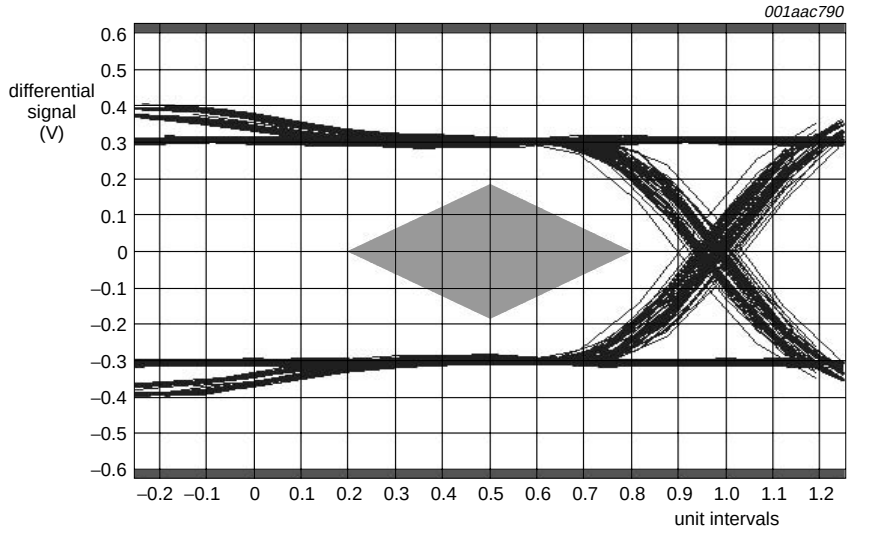


Fig 17. Definition of PXPIPE timing



T_{amb} = 25 °C; nominal V_{DD}

Fig 18. Transition eye

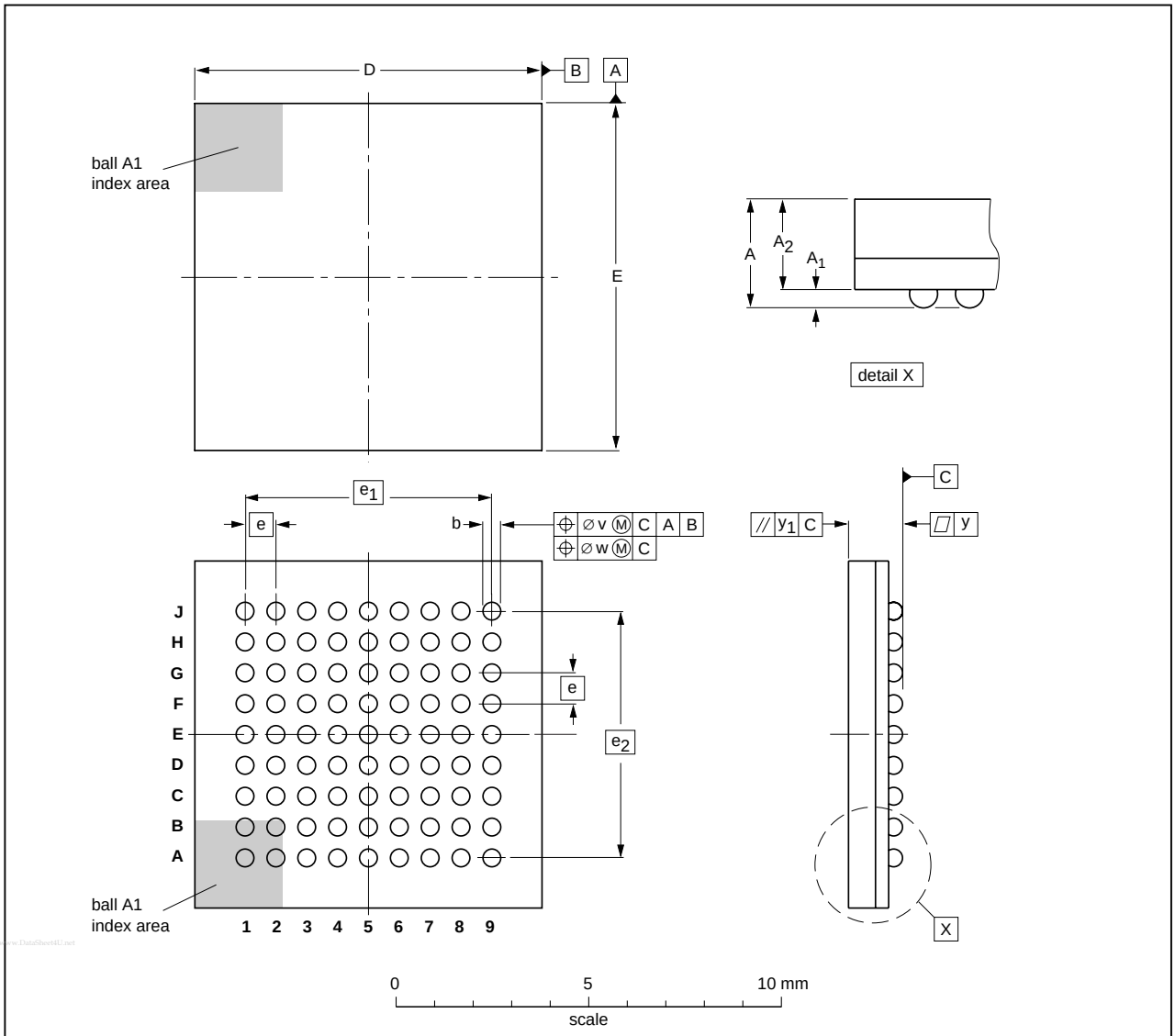


T_{amb} = 25 °C; nominal V_{DD}

Fig 19. Non transition eye

12. Package outline

LFBGA81: plastic low profile fine-pitch ball grid array package; 81 balls; body 9 x 9 x 1.05 mm **SOT643-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.6	0.4 0.3	1.20 0.95	0.5 0.4	9.1 8.9	9.1 8.9	0.8	6.4	6.4	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT643-1		MO-205	- - -			~~00-11-01~~ 02-03-28

Fig 20. Package outline SOT643-1 (LFBGA81)

13. Soldering

13.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 20. SnPb eutectic process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	240 °C + 0/–5 °C	225 °C + 0/–5 °C
≥ 2.5 mm	225 °C + 0/–5 °C	225 °C + 0/–5 °C

Table 21. Pb-free process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 350 to 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

- larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.5 Package related soldering information

Table 22. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Abbreviations

Table 23. Abbreviations

Acronym	Description
BER	Bit Error Rate
BIST	Built-In Self Test
CMOS	Complementary Metal Oxide Semiconductor
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FPGA	Field Programmable Gate Array
LTSSM	Link Training and Status State Machine
MAC	Media Access Control
P2S	Parallel to Serial
PCI	Peripheral Component Interconnect
PCS	Physical Coding Sub-layer
PHY	PHYsical layer
PLL	Phase-Locked Loop
PIPE	PHY Interface for the PCI Express
PVT	Process Voltage Temperature
S2P	Serial to Parallel
SerDes	Serializer and De-serializer
SKP	SKiP
SSTL_2	Stub Series Terminated Logic for 2.5 Volts

15. References

[1] PCI Express Base Specification — Rev. 1.0a - PCISIG

[2] PHY Interface for the PCI Express Architecture (PIPE) Specification Version 1.00 — Intel Corporation

16. Revision history

Table 24. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PX1011A_PX1012A_2	20060518	Product data sheet	-	PX1011A-EL1_1

Modifications:

- changed data sheet status from “Preliminary data sheet” to “Product data sheet”
- Added basic part type PX1012A-EL1
- letter symbols and parameter descriptions modified to harmonize with Philips Semiconductors new presentation and information standard
- Section 1 “General description”:
  - added “single-lane” to first sentence
  - added new second sentence
  - third sentence: added ‘clock and data recovery (CDR)’
  - 3rd paragraph: added second sentence.
- Section 2.1 “PCI Express interface”:
  - first bullet: changed “Specification 1.0a” to “Specification 1.1”
  - split (old) 4th bullet
  - added (new) 7th and 8th bullets
- Section 2.2 “PHY/MAC interface”:
  - deleted (old) 3rd and 4th bullets
  - (new) 4th bullet changed from “SSTL_2 signaling” to “2.5 V SSTL_2 class I signaling
- Section 2.5 “Clock”, 1st bullet: added “with ±300 ppm tolerance”
- Added Section 2.6 “Miscellaneous”
- Table 1 “Quick reference data”:
  - Parameter description for V_{DDD1} modified (added “JTAG”)
  - Min and Max values for V_{DD4} added; deleted Table note [1]; changed symbol to “V_{DD}”
  - added condition “operating” for T_{amb}
  - added industrial temperature range
- Table 2 “Ordering information”: added Type numbers PX1011A-EL1/G, PX1012A-EL1, PX1012A-EL1/G; added industrial temperature range Type numbers PX1011AI-EL1 and PX1012AI-EL1; added column “Soldering compound”
- Figure 1 “Block diagram” modified: changed “PX1011A-EL1” to “PCI Express PHY”
- Table 3:
  - title changed from “Marking” to “Leaded package marking”
  - Line C marking changed from “2Pyyww” to “2PNyyww” (N = leaded)
- Added (new) Table 4 “Lead-free package marking”
- Figure 2 “Pin configuration” modified (added new type numbers)
- changed (old) Table 5 “Pin allocation table” to Figure 3 “Ball mapping” for reader clarity; changed the following pin names:
  - from “V_{DD1}” to “V_{DDD1}”
  - from “V_{DD2}” to “V_{DDD2}”
  - from “V_{DD3}” to “V_{DDD3}”
  - from “V_{DD4}” to “V_{DD}”
- Table 5 “PCI Express serial data lines”: added “with 50 Ω on-chip termination” to descriptions; added Type and Signaling columns
- Table 6 through Table 9: modified titles and added Type and Signaling columns

Table 24. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
PX1011A_PX1012A_2	20060518	Product data sheet	-	PX1011A-EL1_1

Modifications: (continued)

- Table 8 “PXPIPE interface command signals”: modified descriptions for pins RXDET_LOOPB, TXIDLE, TXCOMP, and RXPOL
- Table 9 “PXPIPE interface status signals”: modified all descriptions
- Table 10 “Clock and reference signals”: modified all descriptions
- Table 11: title changed (added “3.3 V”); added Type and Signaling columns
- Table 12 “PCI Express PHY power supplies”: added Type and Signaling columns; descriptions modified
- Section 8 “Functional description”:
  - 1st paragraph re-written
  - (old) 2nd, 4th, 5th and 6th paragraphs deleted
  - (new) 2nd paragraph modified from “The PX1011A-EL1 interface between the MAC and PHY ...” to “The PXPIPE interface between the MAC and PX1011A/1012A ...”
  - (new) 3rd paragraph added
  - removed “(×1 configuration)” from last paragraph
- Section 8.1 “Receiving data”:
  - 1st paragraph, 2nd sentence: deleted phrase “before they go into the SerDes”
  - 2nd paragraph: changed “valid data stream” to “valid stream of data”
- Section 8.2 “Transmitting data”:
  - 1st paragraph: 3rd sentence re-written
  - 2nd paragraph: last sentence re-written
  - 3rd paragraph rewritten
  - deleted (old) 4th, 5th, and 6th paragraphs
- Section 8.3 “Clocking”: re-written
- Figure 4 “Reset” modified
- Section 8.5 “Power management”:
  - 1st paragraph, 1st sentence: changed “minimize power consumption” to “manage power consumption”
  - 3rd paragraph: added (new) last sentence.
  - Table 13 replaced in its entirety
- Section 8.6 “Receiver detect”:
  - 1st paragraph, 1st sentence: changed “is not actively transmitting” to “is in the P1 state”
  - 1st paragraph: 3rd and 4th sentences re-written.
  - Figure 5 “Receiver detect - receiver present” modified
- Section 8.7 “Loopback” moved forward
  - first sentence re-written
  - 3rd and 4th bullets, and 3rd paragraph: changed “parallel interface” to “PXPIPE interface”
  - Figure 6 “Loopback start” modified
  - 7th paragraph deleted
- added new Section 8.8 “Electrical idle”
- Section 8.9 “Clock tolerance compensation”:
  - 1st paragraph, 5th sentence: changed “using the RXSTATUS2 to RXSTATUS0 signals” to “using the RXSTATUS signals”
  - added 3rd paragraph and Figure 10 “Clock correction - remove a SKP”

Table 24. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
PX1011A_PX1012A_2	20060518	Product data sheet	-	PX1011A-EL1_1
Modifications: (continued)	• Section 8.10 “Error detection”: – 1st paragraph, 2nd sentence: changed “signals (RXSTATIS2 to RXSTATUS0).” to “signals RXSTATUS.” – 2nd paragraph: changed from “... at the point in the data stream across the parallel interface closest ... ” to “... at the point closest ... “ • Section 8.10.1 “8b/10b decode errors”, 1st paragraph, 1st sentence: changed “EDB symbol” to “EDB (EnD Bad) symbol” • Section 8.11 “Polarity inversion”, 2nd sentence: changed “... 20 symbols of when RXPOL is asserted.” to “... 20 symbols after RXPOL is asserted.” • Section 8.13 “JTAG boundary scan interface”: deleted sentence 2 of 3rd paragraph; added (new) 1st sentence of 4th paragraph and deleted (old) 2nd sentence; in last sentence, changed “recommended to tie” to “recommended to pull down” • Table 16 “Limiting values”: – parameter description for V_{DDD2} modified (appended “I/O”) – symbol and parameter description for V_{DD4} changed from “V_{DD4}, supply voltage for serial I/O” to “V_{DD}, supply voltage”; moved “for high-speed serial I/O and PVT” to Conditions column – changed $T_{j(max)}$ from “+150 °C” to “+125 °C” – added commercial and industrial ratings for T_{amb} • Table 18 “PCI Express PHY characteristics”: – under subsection “Supplies”, added Min and Max values for V_{DDD2}, I_{DDD1}, I_{DDD2}, I_{DDD3}, I_{DD}, I_{DDA1}, I_{DDA2}; added condition “no load” to I_{DDD2}; changed typical value for I_{DDD1} from 2 mA to 1 mA; changed typical value for I_{DDD2} from 70 mA to 18 mA; changed maximum value for I_{DDA2} from 13 mA to 15 mA – removed subsection “General” – “Receiver” and “Transmitter” sections re-written – deleted Table note [1] • Table 19 “PXPIPE characteristics”: added characteristics f_{RXCLK}, f_{TXCLK}, V_{VREFS}, $V_{OH(SSTL2)}$, $V_{OL(SSTL2)}$, $V_{IH(SSTL2)}$, and $V_{IL(SSTL2)}$		
PX1011A-EL1_1 (9397 750 14914)	20050519	Preliminary data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Philips Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Philips Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

17.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, Philips Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — Philips Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Philips Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a Philips Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Philips Semiconductors accepts no liability for inclusion and/or use of Philips Semiconductors products in such equipment or applications and therefore such inclusion and/or use is for the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — Philips Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.semiconductors.philips.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by Philips Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

19. Contents

For more information, please visit: http://www.semiconductors.philips.com.
For sales office addresses, email to: sales.addresses@www.semiconductors.philips.com.

Date of release: 18 May 2006

Document identifier: PX1011A_PX1012A_2