Rockchip PX2 Datasheet

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Chapter 1 Introduction

1.1 Overview

Rockchip PX2 is a low power, high performance processor for auto audio equipments, building intercom, POS device and other industry users, and integrates dual-core Cortex-A9 with separately NEON and FPU coprocessor.

Embedded 3D GPU makes RK PX2 completely compatible with OpenGL ES2.0 and 1.1, OpenVG 1.1. Special 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK PX2 supports almost full-format video decoder by 1080p@60fps, also support H.264/MVC/VP8 encoder by 1080p@30fps, high-quality JPEG encoder/decoder, special image preprocessor and postprocessor .

RK PX2 has high-performance external memory interface (DDR3/LPDDR2/ LVDDR3) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

This document will provide guideline on how to use RK PX2 correctly and efficiently. The document will introduce block diagram, the features, signal descriptions and system usage of RK PX2.

1.2 Features

1.2.1 MicroProcessor

- Dual-core ARM Cortex-A9 MPCore processor, a high-performance, low-power and cached application processor
- SCU ensures memory coherency between the two CPUs
- Integrated 32KB L1 instruction cache , 32KB L1 data cache with 4-way set associative
- Trustzone technology support
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction, 8-stage pipeline
- Include VFPv3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
- 4 separate power domain to support internal power switch and externally turn on/off based on different application scenario
  - PD_A9_0: 1st Cortex-A9 + Neon + FPU + L1 I/D Cache
  - PD_A9_1: 2nd Cortex-A9 + Neon + FPU + L1 I/D Cache
  - PD_DBG: CoreSight-DK for Cortex-A9
  - PD_SCU: SCU + L2 Cache controller
- Full coresight debug solution
  - Debug and trace visibility of whole systems
  - Invasive and non-invasive debug
  - ETM trace support
- 512KB unified L2 Cache
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- One isolated voltage domain to support DVFS
- Integrated timer and watchdog timer per CPU

1.2.2 Memory Organization

- Internal on-chip memory
  - 10KB BootRom
  - 64KB internal SRAM for security and non-security access, detailed size is programmable
  - 256KB or 512KB internal SRAM shared with L2 Cache Memory

- External off-chip memory①
  - DDR3-1066, 16/32bits data widths, 2 ranks, totally 2GB(max) address space, maximum address space for one rank is also 2GB.
  - LPDDR2-1066, 32bits data width, 2 ranks, totally 2GB(max) address space, maximum address space for one rank is also 2GB.
  - LPDDR-400, 32bits data width, 2 ranks, totally 2GB(max) address space, maximum address space for one rank is also 2GB.
  - Sync ONFI Nand Flash , 8bits data width, 8 banks, 60bits ECC
  - Async Nand Flash(include LBA Nand), 8/16bits data width,8 banks,60bits ECC

1.2.3 Internal Memory

- Internal BootRom
  - Size : 10KB
  - Support system boot from the following device :
    - 8bits ONFI Nand Flash
    - SPI0 interface
    - eMMC interface
  - Support system code download by the following interface:
    - USB OTG interface
    - UART0 Interface
- Internal SRAM
  - Size : 64KB
  - Support security and non-security access
  - Security or non-security space is software programmable
  - Security space can be 0KB,4KB,8KB,12KB,16KB,…,60KB,64KB continuous size
- 256KB or 512KB internal SRAM shared with L2 Cache for Cortex-A9, size is configurable by software.

1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/LPDDR/LPDDR2)
  - Compatible with JEDEC standard DDR3/LPDDR/LPDDR2 SDRAM
  - Data rates up to 1066Mbps(533MHz) for DDR3/LPDDR2 and up to 400Mbps(200MHz) for LPDDR
  - Support up to 2 ranks (chip selects), totally 2GB(max) address space, maximum address space for one rank is also 2GB, which is software-configurable.
  - 16bits/32bits data width is software programmable
  - 5 host ports with 64bits AXI bus interface for system access, AXI bus clock is asynchronous with DDR clock
  - Programmable timing parameters to support DDR3/LPDDR/LPDDR2 SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDR3/LPDDR/LPDDR2 SDRAM; clock stop and deep power-down for LPDDR/LPDDR2 SDRAM
  - Compensation for board delays and variable latencies through programmable pipelines
  - Embedded dynamic drift detection in the PHY to get dynamic drift compensation with the controller
  - Programmable output and ODT impedance with dynamic PVT compensation
  - Support one low-power work mode: power down DDR PHY and most of DDR IO except two cs and two cke output signals , make SDRAM still in self-refresh state to prevent data missing.

- Nand Flash Interface
  - Support 8bits/16bits async nand flash, up to 8 banks
  - Support 8bits sync DDR nand flash, up to 8 banks

- Support LBA nand flash in async or sync mode
- Up to 60bits hardware ECC
- For DDR nand flash, support DLL bypass and 1/4 or 1/8 clock adjust, maximum clock rate is 75MHz
- For async nand flash, support configurable interface timing , maximum data rate is 16bit/cycle
- Embedded special DMA interface to do data transfer

Also support data transfer together with general DMAC1 in SoC system

- eMMC Interface
  - Compatible with standard iNAND interface
  - Support MMC4.41 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - 8bits data bus width

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.41
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - Data bus width is 4bits

1.2.5 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK PX2
  - One oscillator with 24MHz clock input and 4 embedded PLLs
  - Up to 1.4GHz clock output for all PLLs
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components

- PMU(power management unit)
  - 7 work modes(slow mode, normal mode, idle mode, deep-idle mode, stop mode, sleep mode, power-off mode) to save power by different frequency or automatical clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - 3 separate voltage domains
  - 9 separate power domains, which can be power up/down by software based on different application scenes

- PWM
  - Four on-chip PWMs with interrupt-based operation
  - Programmable 4-bit pre-scalar from apb bus clock
  - Embedded 32-bit timer/counter facility
  - Support single-run or continuous-run PWM mode
  - Provides reference mode and output various duty-cycle waveform

- Interrupt Controller
  - Support 3 PPI interrupt source and 76 SPI interrupt sources input from different components inside RK PX2
  - Support 16 softwre-triggered interrupts

- Input interrupt level is fixed , only high-level sensitive
- Two interrupt outputs (nFIQ and nIRQ) separately for each Cortex-A9, both are low-level sensitive
- Support different interrupt priority for each interrupt source, and they are always software-programmable

- Timer
  - 3 on-chip 32bits Timers in SoC with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input

- Bus Architecture
  - 64-bit multi-layer AXI/AHB/APB composite bus architecture
  - 5 embedded AXI interconnect
    - CPU interconnect with three 64-bits AXI masters, two 64-bits AXI slaves, one 32-bits AHB master and lots of 32-bits AHB/APB slaves
    - PERI interconnect with two 64-bits AXI masters, one 64-bits AXI slave, one 32-bits AXI slave, four 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - Display interconnect with six 64-bits AXI masters and one 32-bits AHB slave
    - GPU interconnect with one 128-bits AXI master and one 32-bits APB slave ,they are point-to-point AXI-lite architecture
    - VCODEC interconnect also with one 64-bits AXI master and one 32-bits AHB slave ,they are point-to-point AXI-lite architecture
  - Flexible different QoS solution to improve the utility of bus bandwidth
  - For each interconnect with AXI/AHB/APB composite bus, clocks for AXI/AHB/APB domains are always synchronous, and different integer ratio is supported for them.

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - Two embedded DMA controller , DMAC0 is for cpu system, DMAC1 is for peri system
  - DMAC0 features:
    - 6 channels totally
    - 11 hardware request from peripherals
    - 2 interrupt output
    - Dual APB slave interface for register config, designated as secure and non-secure
    - Support trustzone technology and programmable secure state for each DMA channel
  - DMAC1 features:
    - 7 channels totally
    - 13 hardware request from peripherals
    - 2 interrupt output
    - Not support trustzone technology

- Security system
  - Support trustzone technology for the following components inside RK PX2
    - Cortex-A9, support security and non-security mode, switch by software
    - DMAC0, support some dedicated channels work only in security mode

- eFuse, only accessed by Cortex-A9 in security mode
- Internal memory , part of space is addressed only in security mode, detailed size is software-programmable together with TZMA(trustzone memory adapter) and TZPC(trustzone protection controller)

- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from apb bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

1.2.6 Video CODEC

- Shared internal memory and bus interface for video decoder and encoder②
- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,H.263, H.264 , AVS , VC-1 , RV , VP6/VP8 , Sorenson Spark, MVC
  - Error detection and concealment support for all video formats
  - Output data format is YUV420 semi-planar, and YUV400(monochrome) is also supported for H.264
  - H.264 up to HP level 4.2 : 1080p@60fps (1920x1088)③
  - MPEG-4 up to ASP level 5 : 1080p@60fps (1920x1088)
  - MPEG-2 up to MP : 1080p@60fps (1920x1088)
  - MPEG-1 up to MP : 1080p@60fps (1920x1088)
  - H.263 : 576p@60fps (720x576)
  - Sorenson Spark : 1080p@60fps (1920x1088)
  - VC-1 up to AP level 3 : 1080p@30fps (1920x1088)
  - RV8/RV9/RV10 : 1080p@60fps (1920x1088)
  - VP6/VP8 : 1080p@60fps (1920x1088)
  - AVS : 1080p@60fps (1920x1088)
  - MVC : 1080p@60fps (1920x1088)
  - For AVS, 4:4:4 sampling not supported
  - For H.264, Image cropping not supported
  - For MPEG-4,GMC(global motion compensation) not supported
  - For VC-1, upscaling and range mapping are supported in image post-processor
  - For MPEG-4 SP/H.263/Sorenson spark, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

1.2.7 Video Encoder

- Support video encoder for H.264 (BP@level4.0, MP@level4.0, HP@level4.0), MVC and VP8
- Only support I and P slices, not B slices
- Support error resilience based on constrained intra prediction and slices
- Input data format :
  - YCbCr 4:2:0 planar
  - YCbCr 4:2:0 semi-planar
  - YCbYCr 4:2:2
  - CbYCrY 4:2:2 interleaved
  - RGB444 and BGR444
  - RGB555 and BGR555
  - RGB565 and BGR565
  - RGB888 and BRG888

- RGB101010 and BRG101010
- Image size is from 96x96 to 1920x1088(Full HD)
- Maximum frame rate is up to 30fps@1920x1080[8]
- Bit rate supported is from 10Kbps to 20Mbps

1.2.8 JPEG CODEC

- JPEG encoder
  - Input raw image :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32
  - Maximum data rate[4] up to 90million pixels per second

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Maximum data rate[4] is up to 76million pixels per second

1.2.9 Image Enhancement

- Video stabilization
  - Work in combined mode with HD video encoder inside RK PX2 and stand-alone mode
  - Adaptive motion compensation filter
  - Support scene detection from video sequence, encodes key frame when scene change noticed

- Image pre-processor
  - Only used together with HD video encoder inside RK PX2 , not support stand-alone mode
  - Provides RGB to YCbCr 4:2:0 color space conversion, compatible with BT.601 , BT.709 or user defined coefficients
  - Provides YCbCr4:2:2 to YCbCr4:2:0 color space conversion
  - Support cropping operation from 8192x8192 to any supported encoding size
  - Support rotation with 90 or 270 degrees

- Image post-processor(embedded inside video decoder)
  - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
  - Also work as a stand-alone mode, its input data is from a camera interface or other image data stored in external memory
  - Input data format :
    - any format generated by video decoder in combined mode
    - YCbCr 4:2:0 semi-planar
    - YCbCr 4:2:0 planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2

- Ouput data format:
  - YCbCr 4:2:0 semi-planar
  - YCbYCr 4:2:2
  - YCrYCb 4:2:2
  - CbYCrY 4:2:2
  - CrYCbY 4:2:2
  - Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888,RGB565,ARGB4444 etc.
- Input image size:
  - Combined mode : from 48x48 to 8176x8176 (66.8Mpixels)
  - Stand-alone mode : width from 48 to 8176,height from 48 to 8176, and maximum size limited to 16.7Mpixels
  - Step size is 16 pixels
- Output image size: from 16x16 to 1920x1088 (horizontal step size 8,vertical step size 2)
- Support image up-scaling :
  - Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Maximum output width is 3x input width
  - Maximum output height is 3x input height
- Support image down-scaling:
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Unlimited down-scaling ratio
- Support YUV to RGB color conversioin, compatible with BT.601-5, BT.709 and user definable conversion coefficient
- Support dithering (2x2 ordered spatial dithering for 4,5,6bit RGB channel precision
- Support programmable alpha channel and alpha blending operation with the following overlay input formats:
  - 8bit alpha +YUV444, big endian channel order with AYUV8888
  - 8bit alpha +24bit RGB, big endian channel order with ARGB8888
- Support deinterlacing with conditional spatial deinterlace filtering, only compatible with YUV420 input format
- Support RGB image contrast / brightness / color saturation adjustment
- Support image cropping & digital zoom only for JPEG or stand-alone mode
- Support picture in pcture
- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)

- Image Post-Processor (IPP)(standalone)
  - memory to memory mode
  - input data format and size
    - RGB888 : 16x16 to 8191x8191
    - RGB565 : 16x16 to 8191x8191
    - YUV422/YUV420 : 16x16 to 8190x8190
    - YUV444 : 16x16 to 8190x8190
  - pre scaler
    - integer down-scaling(ratio: 1/2,1/3,1/4,1/5,1/6,1/7,1/8) with linear filter
    - deinterlace(up to 1080i) to support YUV422&YUV420 input format
  - post scaler
    - down-scaling with 1/2 ~ 1 arbitary non-integer ratio
    - up-scaling with 1~4 arbitary non-integer ratio
    - 4-tap vertical, 2-tap horizontal filter
    - The max output image width of post scaler is 4096
  - Support rotation with 90/180/270 degrees and x-mirror,y-mirror

1.2.10 Graphics Engine

- 3D Graphics Engine :

- ARM Mali-400 MP4 GPU
- High performance OpenGL ES1.1 and 2.0, OpenVG1.1 etc.
- Embedded 4 shader cores with shared hierarchical tiler
- Separate vertex(geometry) and fragment(pixel) processing for maximum parallel throughput
- Provide MMU and L2 Cache with 128KB size

- 2D Graphics Engine :
  - Pixel rate: 300M pixel/s without scale, 150M pixel/s with bilinear scale, 75M pixel/s with bicubic scale.
  - Bit Blit with Strength Blit, Simple Blit and Filter Blit
  - Color fill with gradient fill, and pattern fill
  - Line drawing with anti-aliasing and specified width
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - ROP2, ROP3, ROP4 full alpha blending and transparency
  - Alpha blending modes including Java 2 Porter-Duff compositing blending rules , chroma key, and pattern mask
  - 8K x 8K raster 2D coordinate system
  - Arbitrary degrees rotation with anti-aliasing on every 2D primitive
  - Programmable bicubic filter to support image scaling
  - Blending, scaling and rotation are supported in one pass for stretch blit
  - Source formats :
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar
    - YUV422 planar, YUV422 semi-planar
    - BPP8, BPP4, BPP2, BPP1
  - Destination formats :
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar only in filter and pre-scale mode
    - YUV422 planar, YUV422 semi-planar only in filter and pre-scale mode

- HDMI TX Interface
  - HDMI version 1.4a, HDCP revision 1.4 and DVI version 1.0 compliant transmitter
  - Supports DTV from 480i to 1080i/p HD resolution, and PC from VGA to UXGA by LCDC0 or LCDC1 in RK PX2
  - Supports 3D and 2k x 4k video resolution output
  - Programmable 2-way color space converter
  - Compliant with EIA/CEA-861D
  - Deep color supported up to 12bit per pixel.
  - xvYCC Enhanced Colorimetry
  - Gamut Metadata transmission
  - Supports RGB, YCbCr digital video input format includes ITU.656
  - 36bit RGB/YCbCr 4:4:4
    16/20/24bit YCbCr 4:2:2
    8/10/12bit YCbCr 4:2:2 (ITU.601 and 656)
  - Supports standard SPDIF for stereo or compressed audio up to 192KHz by SPDIF controller in RK PX2
  - Support PCM, Dolby digital, DTS digital audio transmission through 8ch I2S controller in RK PX2
  - Wide range channel speed up to 2.2Gbps

1.2.11 Video IN/OUT

- Camera Interface
  - 2 independent camera interface controller
  - Support up to 5M pixels
  - 8bits CCIR656(PAL/NTSC) interface
  - 8bits/10bits/12bits raw data interface
  - YUV422 data input format with adjustable YUV sequence
  - YUV422,YUV420 output format with separately Y and UV space
  - Support picture in picture (PIP)
  - Support simple image effects such as Arbitrary(sepia), Negative, Art freeze, Embossing etc.
  - Support static histogram statistics and white balance statistics
  - Support image crop with arbitrary windows
  - Support scale up/down from 1/8 to 8 with arbitrary non-integer ratio

- Display Interface
  - 2 independent display controller
  - Support LCD or TFT interfaces up to 1920x1080
  - Support HDMI 1.4a output up to 1080p@30fps
  - Support TV interface with ITU-R BT.656 (8bits, 480i/576i/1080i)
  - Parallel RGB LCD Interface : RGB888(24bits),RGB666(18bits),RGB565(15bits)
  - Serial RGB LCD Interface: 3x8bits with RGB delta support, 3x8bits followed by dummy data, 16bits followed by 8bits
  - MCU LCD interface : i-8080 with up to 24bits RGB
  - 5 display layers :
    - One background layer with programmable 24bits color
    - One video layer (win0)
      - RGB888, ARGB888, RGB565, YUV422, YUV420, AYUV
      - maximum resolution is 1920x1080
      - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
      - 256 level alpha blending
      - Support transparency color key
      - Support 3D display
    - One video layer (win1)
      - RGB888, ARGB888, RGB565, YUV422, YUV420,AYUV
      - maximum resolution is 1920x1080
      - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
      - 256 level alpha blending
      - Support transparency color key
    - One OSD layer(win2)
      - RGB888, ARGB888, RGB565, 1/2/4/8BPP
      - 256 level alpha blending
      - transparency color key
    - Hardware cursor(win3)
      - 2BPP
      - Maximum resolution 64x64
      - 3-color and transparent mode
      - 2-color + transparency + tran_invert mode
      - 16 level alpha blending
  - Support 180 rotation in combined mode with LCDC or separately mode
  - 3 x 256 x 8 bits display LUTs
  - Win0 and Win1 layer overlay exchangeable
  - Support color space conversion : YUV2RGB(rec601-mpeg/rec601-jpeg/rec709) and RGB2YUV
  - Deflicker support for interlace output
  - Support replication(16bits to 24bits) and dithering(24bits to 16bits/ 18bits) operation

1.2.12 Audio Interface

- I2S/PCM with 2ch
  - 2 independent I2S/PCM interface with 2 channels
  - Up to 2 channels (2xTX, 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal , left-justified , right-justified)
  - Support 4 PCM formats(early , late1 , late2 , late3)
  - I2S and PCM mode cannot be used at the same time

- I2S/PCM with 8ch
  - Up to 8 channels (4xTX , 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal , left-justified , right-justified)
  - Support 4 PCM formats(early , late1 , late2 , late3)
  - I2S and PCM mode cannot be used at the same time

- SPDIF
  - Audio resolution : 16bits/20bits/24bits
  - Software configurable sample rates (48KHz, 44.1KHz, 32KHz)
  - Stereo voice replay with 2 channels

1.2.13 Connectivity

- USB Host2.0
  - Compatible with USB Host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- USB OTG2.0
  - Compatible with USB OTG2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Endpoints 8/9 can be used as data OUT and IN endpoint
  - Provides 9 host mode channels

- SDIO interface
  - Compatible with SDIO 2.0 protocol
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - 4bits data bus widths

- I2C controller
  - 5 on-chip I2C controller in RK PX2
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s

in the standard mode

- High-speed ADC & TS stream interface
  - Support single-channel 8bits/10bits interface
  - DMA-based and interrupt-based operation
  - Support 8bits TS stream interface
  - Support PID filter operation
    - Combined with high-speed ADC interface to implement filter from original TS data
    - Provide PID filter up to 64 channels PID simultaneously
    - Support sync-byte detection in transport packet head
    - Support packet lost mechanism in condition of limited bandwidth

- SPI Controller
  - 2 on-chip SPI controller inside RK PX2
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode

- Uart Controller
  - 4 on-chip uart controller inside RK PX2
  - DMA-based or interrupt-based operation
  - For UART1/UART2/UART3, Embedded two 32Bytes FIFO for TX and RX operation respectively
  - For UART0, two 64Bytes FIFOs are embedded for TX/RX operation
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start,stop and parity
  - Support different input clock for uart operation to get up to 4Mbps or other special baud rate
  - Support non-integer clock divides for baud clock generation
  - Auto flow control mode is only for UART0, UART1, UART2

- GPIO
  - 6 groups of GPIO (GPIO0~GPIO4, GPIO6) , 32 GPIOs per group in GPIO0~GPIO4, and 16 GPIOs in GPIO6, totally have 176 GPIOs
  - All of GPIOs can be used to generate interrupt to Cortex-A9
  - GPIO6 can be used to wakeup system from stop/sleep/power-off mode
  - All of pullup GPIOs are software-programmable for pullup resistor or not
  - All of pulldown GPIOs are software-programmable for pulldown resistor or not
  - All of GPIOs are always in input direction in default after power-on-reset

- MAC 10/100M Ethernet Controller
  - IEEE802.3u compliant Ethernet Media Access Controller(MAC)
  - Support only RMII(Reduced MII) mode
  - 10Mbps and 100Mbps compatible
  - Automatic retry and automatic collision frame deletion
  - Full duplex support with flow-control
  - Address filtering(broadcast, multicast, logical, physical)
  - Clock can be from RK PX2 or external ethernet PHY

1.2.14 Others

- eFuse
  - 256bits (32x8) high-density electrical Fuse
  - Programming condition：VDDQ must be 2.5V(±10%)
  - Program time is about 10us(±1us)
  - Read condition：VDDQ must be 0V or floating

- Support power-down and standby mode

- Temperature Sensor
  - 2 bipolar-based temperature-sensing cell embedded
  - 2-channel 12-bits SAR ADC
  - Temperature accuracy sensed is ±5 degree
  - SAR-ADC clock must be less than 50KHz
  - Standby Current is about 180uA for analog and 40uA for digital logic
  - Power Down Current is about 1uA for anolog and 5uA for digital logic

- SAR-ADC(Successive Approximation Register)
  - 4-channel single-ended 10-bit SAR analog-to-digital converter
  - Conversion speed range is up to 1 MSPS
  - SAR-ADC clock must be less than 1MHz
  - DNL is less than ±1 LSB , INL is less than ±2.0 LSB
  - Power down current is about 0.5uA for analog and digital logic
  - Power supply is 2.5V (±10%) for analog interface

Notes : ① *DDR3/LPDDR/LPDDR2 are not used simultaneously as well as async and sync ddr nand flash*
② *In RK PX2, Video decoder and encoder are not used simultaneously because of shared internal buffer*
③ *Actual maximum frame rate will depend on the clock frequency and system bus performance*
④ *Actual maximum data rate will depend on the clock frequency and JPEG compression rate*

1.3 Block Diagram

The following diagram shows the basic block diagram for RK PX2.

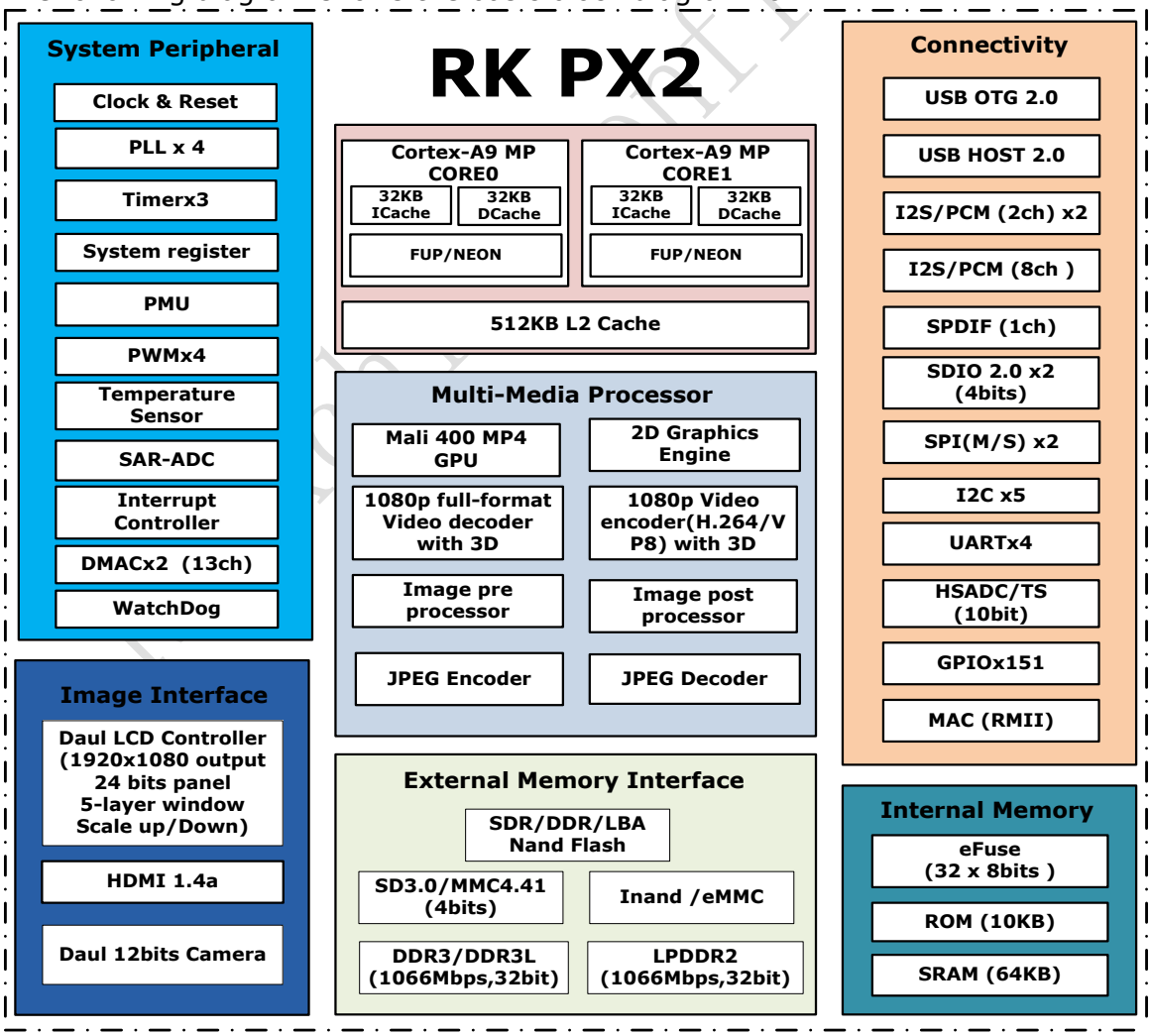


Fig.1-1 RK PX2 Block Diagram

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package Qty	Device special feature
RKPX2	Pb-Free	TFBGA453LD	700pcs	Dual core A9 AP

2.2 Dimension

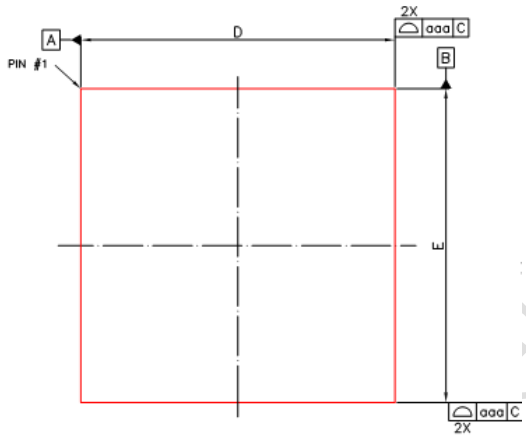


Fig.2-1 RK PX2 TFBGA453 Package Top View

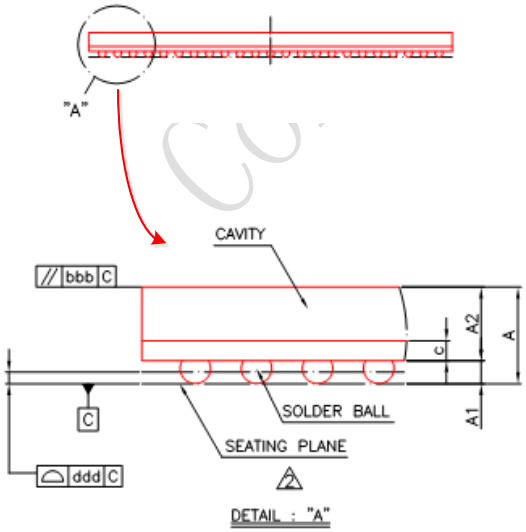


Fig.3-2 RK PX2 TFBGA453 Package Side View

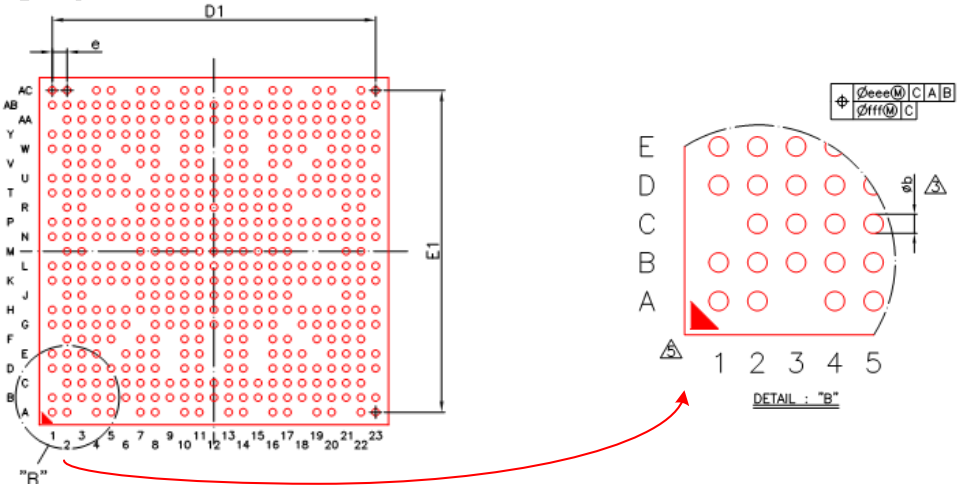


Fig.4-3 RK PX2 TFBGA453 Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
b	0.35	0.40	0.45	0.014	0.016	0.018
c	0.22	0.26	0.30	0.009	0.010	0.012
D	18.90	19.00	19.10	0.744	0.748	0.752
E	18.90	19.00	19.10	0.744	0.748	0.752
D1	---	17.60	---	---	0.693	---
E1	---	17.60	---	---	0.693	---
e	---	0.80	---	---	0.031	---
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.15			0.006		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	23/23			23/23		

Fig.5-4 RK PX2 TFBGA453 Package Dimension

2.3 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12
A	HDMI_TX2	HDMI_TX1	NP	HDMI_TX0	HDMI_TXC	NP	MDQ27	MDQS_B3	NP	MDQ10	MDQS_B1	NP
B	HDMI_TX2N	HDMI_TX1N	HDMI_AVSS	HDMI_TX0N	HDMI_TXCN	HDMI_AVSS	MDQ26	MDQS_3	MDQ8	MDQ11	MDQS_1	MDQ15
C	NP	LCD0_D2	LCD0_D1	LCD0_D0	HDMI_AVSS	HDMI_REXT	MDQ24	MDQ31	MDM1	MDQ9	MDQ14	MRESET
D	LCD0_D4	LCD0_D6	LCD0_D3	LCD0_DEN	LCD0_VSYNC	LCD0_HSYNC	MDQ25	MDQ29	NP	MDQ12	MCKE1/A15 *	NP
E	LCD0_D12	LCD0_D10	LCD0_D9	LCD0_D7	NP	LCD0_DCLK	MDM3	MDQ28	NP	MDQ30	MDQ13	NP
F	NP	LCD0_D16	LCD0_D11	LCD0_D8	LCD0_D5	NP	HDMIVDD_1V1	HDMIAVDD_2V5	NP	MVDD	MVDD	NP
G	LCD0_D19	LCD0_D18	LCD0_D17	LCD0_D14	LCD0_D13	LCD0_D15	NP	HDMI_AVSS	HDMI_AVSS	MVDD	CVDD_1V1	VSS
H	GPIO2_A2/LCD1_D2/SMC_A6	LCD0_D22	LCD0_D21	LCD0_D20	LCD0_D23	GPIO2_A0/LCD1_D0/SMC_A4	CVDD_1V1	VSS	VSS	VSS	VSS	VSS
J	NP	GPIO2_A1/LCD1_D1/SMC_A5	GPIO2_B5/LCD1_D13/SMC_A17/TS_VALID	NP	NP	NP	LCD0_VCC1	VSS	VSS	VSS	VSS	VSS
K	GPIO2_C4/LCD1_D20/SPI1_CSN0/TS_D1	GPIO2_C3/LCD1_D19/SPI1_CLK/TS_D0	GPIO2_C2/LCD1_D18/SMC_BIS_N1/TS_D5	GPIO2_C1/LCD1_D17/SMC_BIS_N0/TS_D6	GPIO2_B7/LCD1_D15/SMC_A19/TS_D7	GPIO2_B6/LCD1_D14/SMC_A18/TS_SYNC	LCD0_VCC0	VSS	VSS	VSS	VSS	VSS
L	GPIO2_C5/LCD1_D21/SPI1_TXD/TS_D2	GPIO2_C6/LCD1_D22/SPI1_RXD/TS_D3	GPIO2_C7/LCD1_D23/SPI1_CSN1/TS_D4	CIF0_D3	GPIO2_C0/LCD1_D16/GPS_CLK/TS_CLKO	CIF0_D2	LCD1_VCC	VSS	VSS	VSS	VSS	VSS
M	NP	CIF0_D5	CIF0_D4	NP	NP	NP	CIF0_VCC	VSS	VSS	VSS	VSS	VSS
N	CIF0_D6	CIF0_D7	CIF0_D8	CIF0_VSYNC	AVDD	CIF1_VCC	CVDD_1V1	VSS	VSS	VSS	VSS	VSS
P	CIF0_D9	CIF0_HREF	CIF0_CLKIN	GPIO1_B5/CIF0_D1	AVDD	AVDD	VSS	VSS	VSS	VSS	VSS	VSS
R	NP	GPIO1_B3/CIF0_CLKO	GPIO1_B4/CIF0_D0	NP	NP	NP	VSS	VSS	VSS	VSS	VSS	VSS
T	GPIO1_B6/CIF0_D10	GPIO1_B7/CIF0_D11	GPIO3_A2/I2C3_SDA	GPIO1_C4/CIF1_D6/RMII_RX_ERR	AVDD	AVDD	VSS	VSS	VSS	VSS	AVSS_APLL	AVSS_DPLL
U	GPIO3_A3/I2C3_SCL	GPIO1_C0/CIF1_D2/RMII_CLKO	GPIO1_C1/CIF1_D3/RMII_TX_EN	GPIO1_C5/CIF1_D7/RMII_CRS_DVALID	AVDD	AVDD	NP	AVDD	AVDD	APLL_1V1	DPLL_1V1	C/GPLL_1V1

V	NP	GPIO1_C2/CIF1_D4/RMII_TXD1	GPIO1_C3/CIF1_D5/RMII_TXD0	GPIO1_C7/CIF1_D9/RMII_RXD0	AVDD	NP	AVDD	AVDD	NP	AVDD_COM	ADCVDD_2V5	NP
W	GPIO1_C6/CIF1_D8/RMII_RXD1	GPIO1_D0/CIF1_VSYNC/MII_MD	GPIO1_D1/CIF1_HREF/MII_MDCLK	GPIO1_D2/CIF1_CLKIN	NP	ADC_IN0	ADC_IN2	ADC_IN1	NP	GPIO6_B0	GPIO6_A0	NP
Y	GPIO1_D7/CIF1_CLKO	GPIO1_D6/CIF1_D11	GPIO3_A5/I2C4_SCL	GPIO3_A4/I2C4_SDA	GPIO6_A4	GPIO6_A5	NPOR	GPIO6_A6	NP	GPIO3_C6/SDMMC1_DET	GPIO1_A1/UART0_TX	NP
AA	NP	GPIO6_B2	GPIO6_A1	CLK32K_IN	GPIO6_A3	OTG_RKELVIN	GPIO1_A4/UART1_RX/SPI0_CSN0	GPIO3_D2/SDMMC1_INT	GPIO3_C3/SDMMC1_D2	GPIO3_C4/SDMMC1_D3	GPIO1_A2/UART0_CTSN	GPIO3_C5/SDMMC1_CLKO
AB	CPU_PWROFF	GPIO6_B1	GPIO6_A2	OTG_ID	OTG_VBUS	GPIO1_A6/UART1_CTSN/SPI0_RXD	GPIO1_A7/UART1_RTSN/SPI0_TXD	GPIO3_C0/SDMMC1_CMD	GPIO3_C2/SDMMC1_D1	VSS	XOUT24M	GPIO1_A0/UART0_RX
AC	CORE_PWROFF	GPIO6_B3	NP	GPIO6_A7	GPIO1_A5/UART1_TX/SPI0_CLK	NP	GPIO4_B7/SPI0_CSN1	GPIO3_C1/SDMMC1_D0	NP	GPIO1_A3/UART0_RTSN	XIN24M	NP
	1	2	3	4	5	6	7	8	9	10	11	12

	13	14	15	16	17	18	19	20	21	22	23
A	MCKE0	MBA0	NP	MCK_N	MA1	NP	MA7	MA11	NP	MDQS_B2	MDQ20
B	MCSN0	MBA1	MA0	MCK	MA4	MA6	MA8	MODT0	MDQ16	MDQS_2	MDQ21
C	MWEN	MBA2	MA3	VSS	MA5	MA9	MA13	MODT1	MDM2	MDQ17	NP
D	MCASN	MRASN	NP	MA14	MDQ19	MA10	MA12	VSS	MDQ22	MDQ23	MDM0
E	MCSN1	MA2	NP	MDQ18	MDQ0	MDQ3	NP	MDQ2	MDQ1	MDQS_0	MDQS_B0
F	MVREF	MVDD	NP	MVDD	MVDD	NP	MDQ4	MDQ7	MDQ5	MDQ6	NP
G	MVDD	MVDD	MPZQ	CVDD_1V1	NP	GPIO2_D5/I2C0_SCL	GPIO2_D4/I2C0_SDA	TRSTN	TMS/PLL_BYPASS	TDI/CPR_BYPASS	GPIO6_B4
H	VSS	VSS	VSS	VSS	VCCIO1	GPIO0_A6/HOST_DRV_VBUS	GPIO0_A2/HDMI_I2C_SDA	PWM2/GPIO0_D6	PWM1/GPIO0_A4	TDO	TCK/HSSCAN_SHIFT_CLOCK
J	VSS	VSS	VSS	VSS	CVDD_1V1	NP	NP	NP	PWM3/GPIO0_D7	GPIO0_A5/OTG_DRV_VBUS	NP
K	VSS	VSS	VSS	VSS	VCCIO0	GPIO3_D5/UART3_CTSN	GPIO3_D4/UART3_TX	GPIO3_B5/SDMMC0_D3	GPIO0_B4/I2S0_SDO0	GPIO2_D7/I2C1_SCL	GPIO3_A0/I2C2_SDA
L	VSS	VSS	VSS	VSS	CVDD_1V1	GPIO3_D6/UART3_RTSN	GPIO3_D3/UART3_RX	GPIO3_B6/SDMMC0_DET	GPIO0_A7/I2S0_SDI	GPIO1_B2/SPDIF_TX	GPIO2_D6/I2C1_SDA

M	VSS	VSS	VSS	VSS	VSS	NP	NP	NP	GPIO3_B2/SDMMC0_D0	GPIO0_B7/I2S0_SDO3	NP
N	VSS	VSS	VSS	VSS	FLASH_VCC	GPIO4_B0/FLASH_CSN1	GPIO3_B7/SDMMC0_WP	FLASH_RDN	GPIO3_D7/FLASH_DQS/EMMC_CLKO	GPIO1_B0/UART2_RX	GPIO0_B6/I2S0_SDO2
P	VSS	VSS	VSS	VSS	CVDD_1V1	FLASH_D0/EMMC_D0	GPIO0_D0/I2S2_CLK/SMC_CSN0	GPIO0_D1/I2S2_SCLK/SMC_WEN	GPIO4_B2/FLASH_CSN3/EMMC_RSTNO	GPIO3_B1/SDMMC0_CMD	GPIO0_B5/I2S0_SDO1
R	VSS	VSS	VSS	VSS	SMC_VCC	NP	NP	NP	GPIO0_B3/I2S0_LRCK_TX	GPIO0_B2/I2S0_LRCK_RX	NP
T	AVSS_C/GPLL	VSS	VSS	VSS	CVDD_1V1	GPIO0_C6/TRACE_CLK/SMC_A2	GPIO4_C3/SMC_D3/TRACE_D3	FLASH_ALE	GPIO3_B4/SDMMC0_D2	GPIO0_B0/I2S0_CLK	GPIO0_B1/I2S0_SCLK
U	PVDD_1V1	USBVDD_1V1	USBVDD_2V5	AP0_VCC	NP	GPIO4_D4/SMC_D12/TRACE_D12	GPIO4_C5/SMC_D5/TRACE_D5	FLASH_RDY	GPIO4_B1/FLASH_CSN2/EMMC_CMD	GPIO3_B0/SDMMC0_CLKO	GPIO3_B3/SDMMC0_D1
V	PVCC_3V3	USBVDD_3V3	NP	AP1_VCC	GPIO4_C4/SMC_D4/TRACE_D4	NP	GPIO4_C6/SMC_D6/TRACE_D6	FLASH_D5/EMMC_D5	GPIO0_D4/I2S2_SDI/SMC_A0	GPIO3_A7/SDMMC0_PWREN	NP
W	HOST_RKELVIN	EFUSE	NP	GPIO4_C2/SMC_D2/TRACE_D2	GPIO4_C1/SMC_D1/TRACE_D1	GPIO4_C7/SMC_D7/TRACE_D7	NP	GPIO4_D2/SMC_D10/TRACE_D10	GPIO0_D3/I2S2_LRCK_TX/SMC_ADVN	FLASH_D3/EMMC_D3	GPIO3_A6/SDMMC0_RSTNO
Y	GPIO3_D0/SDMMC1_PWREN	GPIO0_C4/I2S1_SDI	NP	GPIO0_A1/HDMI_I2C_SCL	GPIO4_C0/SMC_D0/TRACE_D0	GPIO4_D0/SMC_D8/TRACE_D8	GPIO3_A1/I2C2_SCL	GPIO4_D6/SMC_D14/TRACE_D14	GPIO0_D2/I2S2_LRCK_RX/SMC_OEN	FLASH_D4/EMMC_D4	FLASH_CSN0
AA	GPIO3_C7/SDMMC1_WP	GPIO3_D1/SDMMC1_BACKEND	PWM0/GPIO0_A3	VSS	VSS	GPIO4_D1/SMC_D9/TRACE_D9	GPIO0_A0/HDMI_HPD	GPIO4_D7/SMC_D15/TRACE_D15	FLASH_D1/EMMC_D1	FLASH_D6/EMMC_D6	NP
AB	GPIO0_C1/I2S1_SCLK	GPIO0_C3/I2S1_LRCK_TX	GPIO0_C5/I2S1_SDO	OTG_DM	HOST_DM	GPIO4_D3/SMC_D11/TRACE_D11	GPIO1_B1/UART2_TX	GPIO0_C7/TRACE_CTL/SMC_A3	FLASH_D2/EMMC_D2	FLASH_D7/EMMC_D7	FLASH_WP/EMMC_PWREN
AC	GPIO0_C0/I2S1_CLK	GPIO0_C2/I2S1_LRCK_RX	NP	OTG_DP	HOST_DP	NP	GPIO4_D5/SMC_D13/TRACE_D13	GPIO0_D5/I2S2_SDO/SMC_A1	NP	FLASH_CLE	FLASH_WRN
	13	14	15	16	17	18	19	20	21	22	23

Fig.6-5 RK PX2 Ball Mapping Diagram

2.4 Power/ground PIN descriptions

Table 2 -1 RK PX2 Power/Ground IO information

Group	Ball #	Descriptions
AVDD	N5,P5,P6,T5,T6,U5, U6,V5,U8,U9,V7,V8	Internal CPU Core Power
CVDD	G11,G16,H7,J17, L17,N7,P17,T17	Internal Core Power, include GPU and Logic w/o CPU and PMU logic
PVDD	U13	Internal PMU Domain Power
PVCC	V13	Digital GPIO Power for PMU Domain
VDDIO0	K17	Digital GPIO Power
VDDIO1	H17	
LCD0_VCC0	K7	LCDC0 Digital IO Power

LCD0_VCC1	J7	
LCD1_VCC	L7	LCDC1 Digital IO Power
CIF0_VCC	M7	Camera0 Digital IO Power
CIF1_VCC	N6	Camera1 Digital IO Power
SMC_VCC	R17	SMC Digital IO Power
FLASH_VCC	N17	Nand Flash Digital IO Power
AP0_VCC	U16	I2S1/UART0/SDIO Digital IO Power
AP1_VCC	V16	SPI0/UART1 Digital IO Power
MVDD	F10,F11,F14,F16,F17,G10,G13,G14	DDR3 Digital IO Power LVDDR3 Digital IO Power LPDDR2 Digital IO Power
AVSS_APLL	T11	ARM PLLAnalog Ground
AVDD_APLL	U10	ARM PLL Analog Power
AVSS_DPLL	T12	DDR PLL Analog Ground
AVDD_DPLL	U11	DDR PLLAnalog Power
AVSS_CGPLL	T13	CODEC/GENERAL PLL Analog Ground
AVDD_CGPLL	U12	CODEC/GENERAL PLL Analog Power
VDDA_SARADC VDDA_TSADC	V11	SAR-ADC/TS-ADC Analog Power
OTG_DVDD HOST_DVDD	U14	USB OTG2.0/Host2.0 Digital Power
OTG_VDD25 HOST_VDD25	U15	USB OTG2.0/Host2.0 Analog Power
OTG_VDD33 HOST_VDD33	V14	USB OTG2.0/Host2.0 Analog Power
EFUSE_VDDQ	W14	Program Power Supply for eFuse Read Power Supply for eFuse
HDMI_AVSS	B3,B6,C5,G8,G9	HDMI Analog Ground
HDMI_AVDD	F8	HDMI Analog Power Supply
HDMI_VDD	F7	HDMI Analog Power Supply
GND	H8,H9,H10,H11,H12,H13,H14,H15, H16,J8,J9,J10,J11,J12,J13,J14,J15, J16,K8,K9,K10,K11,K12,K13,K14,K15, K16,L8,L9,L10,L11,L12,L13,L14,L15, L16,M8,M9,M10,M11,M12,M13,M14, M15,M16,N8,N9,N10,N11,N12,N13, N14,N15,N16,P8,P9,P10,P11,P12,P13, P14,P15,P16,R8,R9,R10,R11,R12,R13, R14,R15,R16,T8,T9,T10,P7,R7,T7,T14, T15,T16,G12,G16,M17,D20, AB10,AA16,AA17	Internal Core Ground and Digital IO Ground

2.5 Function IO descriptions

Table 2-2 RK PX2 IO descriptions

Pin Name	Ball #	func0	func1	func2	func3	Pad bype①	Drive ②	pull up/ down	Reset State③	Power supply⑤
Left Side④										
LCDC0_DATA[7]	E4	LCDC0_DATA[7]				I/O	8	N/A	I	LCD0_VCC0 LCD0_VCC1
LCDC0_DATA[8]	F4	LCDC0_DATA[8]				I/O	8	N/A	I	
LCDC0_DATA[9]	E3	LCDC0_DATA[9]				I/O	8	N/A	I	
LCDC0_DATA[10]	E2	LCDC0_DATA[10]				I/O	8	N/A	I	
LCDC0_DATA[11]	F3	LCDC0_DATA[11]				I/O	8	N/A	I	
LCDC0_DATA[12]	E1	LCDC0_DATA[12]				I/O	8	N/A	I	
LCDC0_DATA[13]	G5	LCDC0_DATA[13]				I/O	8	N/A	I	
LCDC0_DATA[14]	G4	LCDC0_DATA[14]				I/O	8	N/A	I	
LCDC0_DATA[15]	G6	LCDC0_DATA[15]				I/O	8	N/A	I	
LCDC0_DATA[16]	F2	LCDC0_DATA[16]				I/O	8	N/A	I	
LCDC0_DATA[17]	G3	LCDC0_DATA[17]				I/O	8	N/A	I	
LCDC0_DATA[18]	G2	LCDC0_DATA[18]				I/O	8	N/A	I	
LCDC0_DATA[19]	G1	LCDC0_DATA[19]				I/O	8	N/A	I	
LCDC0_DATA[20]	H4	LCDC0_DATA[20]				I/O	8	N/A	I	
LCDC0_DATA[21]	H3	LCDC0_DATA[21]				I/O	8	N/A	I	
LCDC0_DATA[22]	H2	LCDC0_DATA[22]				I/O	8	N/A	I	
LCDC0_DATA[23]	H5	LCDC0_DATA[23]				I/O	8	N/A	I	
GPIO2_A[0]	H6	GPIO2_A[0]	lcdc1_data0	smc_addr4		I/O	8	down	I	LCD1_VCC
GPIO2_A[1]	J2	GPIO2_A[1]	lcdc1_data1	smc_addr5		I/O	8	down	I	
GPIO2_A[2]	H1	GPIO2_A[2]	lcdc1_data2	smc_addr6		I/O	8	down	I	
GPIO2_B[5]	J3	GPIO2_B[5]	lcdc1_data13	smc_addr17	hsadc_data8	I/O	8	down	I	
GPIO2_B[6]	K6	GPIO2_B[6]	lcdc1_data14	smc_addr18	ts_sync	I/O	8	down	I	
GPIO2_B[7]	K5	GPIO2_B[7]	lcdc1_data15	smc_addr19	hsadc_data7	I/O	8	down	I	
GPIO2_C[0]	L5	GPIO2_C[0]	lcdc1_data16	gps_clk	hsadc_clkout	I/O	8	down	I	

GPIO2_C[1]	K4	GPIO2_C[1]	lcdc1_data17	smc_bls_n0	hsadc_data6	I/O	8	down	I	
GPIO2_C[2]	K3	GPIO2_C[2]	lcdc1_data18	smc_bls_n1	hsadc_data5	I/O	8	down	I	
GPIO2_C[3]	K2	GPIO2_C[3]	lcdc1_data19	spi1_clk	hsadc_data0	I/O	8	down	I	
GPIO2_C[4]	K1	GPIO2_C[4]	lcdc1_data20	spi1_csn0	hsadc_data1	I/O	8	down	I	
GPIO2_C[5]	L1	GPIO2_C[5]	lcdc1_data21	spi1_txd	hsadc_data2	I/O	8	down	I	
GPIO2_C[6]	L2	GPIO2_C[6]	lcdc1_data22	spi1_rxd	hsadc_data3	I/O	8	down	I	
GPIO2_C[7]	L3	GPIO2_C[7]	lcdc1_data23	spi1_csn1	hsadc_data4	I/O	8	down	I	
CIF0_DATAIN[2]	L6	CIF0_DATAIN[2]				I	8	down	I	CIF0_VCC
CIF0_DATAIN[3]	L4	CIF0_DATAIN[3]				I	8	down	I	
CIF0_DATAIN[4]	M3	CIF0_DATAIN[4]				I	8	down	I	
CIF0_DATAIN[5]	M2	CIF0_DATAIN[5]				I	8	down	I	
CIF0_DATAIN[6]	N1	CIF0_DATAIN[6]				I	8	down	I	
CIF0_DATAIN[7]	N2	CIF0_DATAIN[7]				I	8	down	I	
CIF0_DATAIN[8]	N3	CIF0_DATAIN[8]				I	8	down	I	
CIF0_DATAIN[9]	P1	CIF0_DATAIN[9]				I	8	down	I	
CIF0_VSYNC	N4	CIF0_VSYNC				I	8	down	I	
CIF0_HREF	P2	CIF0_HREF				I	8	down	I	
CIF0_CLKIN	P3	CIF0_CLKIN				I	8	down	I	
GPIO1_B[3]	R2	GPIO1_B[3]	cif0_clkout			I/O	4	down	I	
GPIO1_B[4]	R3	GPIO1_B[4]	cif0_data0			I/O	8	down	I	
GPIO1_B[5]	P4	GPIO1_B[5]	cif0_data1			I/O	8	down	I	
GPIO1_B[6]	T1	GPIO1_B[6]	cif0_data10			I/O	8	down	I	
GPIO1_B[7]	T2	GPIO1_B[7]	cif0_data11			I/O	8	down	I	
GPIO3_A[2]	T3	GPIO3_A[2]	i2c3_sda			I/O	8	up	I	
GPIO3_A[3]	U1	GPIO3_A[3]	i2c3_scl			I/O	8	up	I	
GPIO1_C[0]	U2	GPIO1_C[0]	cif1_data2	rmii_clkout	rmii_clkin	I/O	4	down	I	CIF1_VCC
GPIO1_C[1]	U3	GPIO1_C[1]	cif1_data3	rmii_tx_en		I/O	4	down	I	
GPIO1_C[2]	V2	GPIO1_C[2]	cif1_data4	rmii_txd1		I/O	4	down	I	
GPIO1_C[3]	V3	GPIO1_C[3]	cif1_data5	rmii_txd0		I/O	4	down	I	
GPIO1_C[4]	T4	GPIO1_C[4]	cif1_data6	rmii_rx_err		I/O	8	down	I	

GPIO1_C[5]	U4	GPIO1_C[5]	cif1_data7	rmii_crs_dvalid		I/O	8	down	I	
GPIO1_C[6]	W1	GPIO1_C[6]	cif1_data8	rmii_rxd1		I/O	8	down	I	
GPIO1_C[7]	V4	GPIO1_C[7]	cif1_data9	rmii_rxd0		I/O	8	down	I	
GPIO1_D[0]	W2	GPIO1_D[0]	cif1_vsync	mii_md		I/O	8	down	I	
GPIO1_D[1]	W3	GPIO1_D[1]	cif1_href	mii_mdclk		I/O	8	down	I	
GPIO1_D[2]	W4	GPIO1_D[2]	cif1_clkin			I/O	8	down	I	
GPIO1_D[7]	Y1	GPIO1_D[7]	cif1_clkout			I/O	4	down	I	
GPIO1_D[6]	Y2	GPIO1_D[6]	cif1_data11			I/O	8	down	I	
GPIO3_A[4]	Y4	GPIO3_A[4]	i2c4_sda			I/O	8	up	I	
GPIO3_A[5]	Y3	GPIO3_A[5]	i2c4_scl			I/O	8	up	I	
Bottom Side										
ARMP_power_feedback	V10	1.1V				P	N/A	N/A	N/A	
VDDA_SARADC	V11	2.5V				AP	N/A	N/A	N/A	SARADC Domain
SARADC_AIN[2]	W7	SARADC_AIN[2]				A	N/A	N/A	N/A	
SARADC_AIN[1]	W8	SARADC_AIN[1]				A	N/A	N/A	N/A	
SARADC_AIN[0]	W6	SARADC_AIN[0]				A	N/A	N/A	N/A	
AVSS_CGPLL	T13	Analog Ground				AG	N/A	N/A	N/A	PLL Domain
AVDD_CGPLL	U12	1.1V				AP	N/A	N/A	N/A	
AVSS_APLL	T11	Analog Ground				AG	N/A	N/A	N/A	
AVDD_APLL	U10	1.1V				AP	N/A	N/A	N/A	
AVDD_DPLL	U11	1.1V				AP	N/A	N/A	N/A	
AVSS_DPLL	T12	Analog Ground				AG	N/A	N/A	N/A	
CPU_PWROFF	AB1	CPU_PWROFF				O	8	down	O	PVCC
CORE_PWROFF	AC1	CORE_PWROFF				O	8	down	O	
GPIO6_B[0]	W10	GPIO6_B[0]				I/O	8	down	I	
GPIO6_B[1]	AB2	GPIO6_B[1]				I/O	8	down	I	
GPIO6_B[2]	AA2	GPIO6_B[2]				I/O	8	down	I	
GPIO6_B[3]	AC2	GPIO6_B[3]				I/O	8	down	I	
GPIO6_A[0]	W11	GPIO6_A[0]				I/O	8	up	I	

GPIO6_A[1]	AA3	GPIO6_A[1]				I/O	8	up	I	
GPIO6_A[2]	AB3	GPIO6_A[2]				I/O	8	up	I	
GPIO6_A[3]	AA5	GPIO6_A[3]				I/O	8	up	I	
GPIO6_A[4]	Y5	GPIO6_A[4]				I/O	8	up	I	
GPIO6_A[5]	Y6	GPIO6_A[5]				I/O	8	up	I	
CLK32K	AA4	CLK32K				I	N/A	down	I	
XIN24M	AC11	XIN24M				I	N/A	N/A	I	
XOUT24M	AB11	XOUT24M				O	N/A	N/A	O	
GPIO6_A[6]	Y8	GPIO6_A[6]				I/O	8	up	I	
GPIO6_A[7]	AC4	GPIO6_A[7]				I/O	8	up	I	
NPOR	Y7	NPOR				I	8	N/A	I	
OTG_DVDD	U14	OTG_DVDD				DP	N/A	N/A	N/A	USB Domain
OTG_ID	AB4	OTG_ID				A	N/A	N/A	N/A	
OTG_VBUS	AB5	OTG_VBUS				A	N/A	N/A	N/A	
OTG_VDD33	V14	OTG_VDD33				AP	N/A	N/A	N/A	
OTG_DP	AC16	OTG_DP				A	N/A	N/A	N/A	
OTG_DM	AB16	OTG_DM				A	N/A	N/A	N/A	
OTG_RKELVIN	AA6	OTG_RKELVIN				A	N/A	N/A	N/A	
OTG_VDD25	U15	OTG_VDD25				AP	N/A	N/A	N/A	
HOST_DP	AC17	HOST_DP				A	N/A	N/A	N/A	
HOST_DM	AB17	HOST_DM				A	N/A	N/A	N/A	
HOST_RKELVIN	W13	HOST_RKELVIN				A	N/A	N/A	N/A	
EFUSE_VDDQ	W14	EFUSE_VDDQ				AP	N/A	N/A	N/A	EFUSE Domain
GPIO1_A[4]	AA7	GPIO1_A[4]	uart1_sin	spi0_csn0		I/O	8	up	I	AP1_VCC
GPIO1_A[5]	AC5	GPIO1_A[5]	uart1_sout	spi0_clk		I/O	8	down	I	
GPIO1_A[6]	AB6	GPIO1_A[6]	uart1_cts_n	spi0_rxd		I/O	8	up	I	
GPIO1_A[7]	AB7	GPIO1_A[7]	uart1_rts_n	spi0_txd		I/O	8	up	I	
GPIO4_B[7]	AC7	GPIO4_B[7]	spi0_csn1			I/O	8	up	I	
GPIO3_D[2]	AA8	GPIO3_D[2]	sdmmc1_int_n			I/O	8	up	I	AP0_VCC

GPIO3_C[0]	AB8	GPIO3_C[0]	sdmmc1_cmd			I/O	4	up	I	
GPIO3_C[1]	AC8	GPIO3_C[1]	sdmmc1_data0			I/O	4	up	I	
GPIO3_C[2]	AB9	GPIO3_C[2]	sdmmc1_data1			I/O	4	up	I	
GPIO3_C[3]	AA9	GPIO3_C[3]	sdmmc1_data2			I/O	4	up	I	
GPIO3_C[4]	AA10	GPIO3_C[4]	sdmmc1_data3			I/O	4	up	I	
GPIO3_C[5]	AA12	GPIO3_C[5]	sdmmc1_clkout			I/O	4	down	I	
GPIO3_C[6]	Y10	GPIO3_C[6]	sdmmc1_detect_n			I/O	8	up	I	
GPIO3_C[7]	AA13	GPIO3_C[7]	sdmmc1_write_prt			I/O	8	down	I	
GPIO3_D[0]	Y13	GPIO3_D[0]	sdmmc1_pwr_en			I/O	8	down	I	
GPIO3_D[1]	AA14	GPIO3_D[1]	sdmmc1_backend_pwr			I/O	8	down	I	
GPIO0_C[4]	Y14	GPIO0_C[4]	i2s1_sdi			I/O	8	down	I	
Right Side										
GPIO0_C[0]	AC13	GPIO0_C[0]	i2s1_clk			I/O	4	down	I	
GPIO0_C[1]	AB13	GPIO0_C[1]	i2s1_sclk			I/O	4	down	I	
GPIO0_C[2]	AC14	GPIO0_C[2]	i2s1_lrck_rx			I/O	4	down	I	
GPIO0_C[3]	AB14	GPIO0_C[3]	i2s1_lrck_tx			I/O	4	down	I	
GPIO0_C[5]	AB15	GPIO0_C[5]	i2s1_sdo			I/O	4	down	I	AP0_VCC
GPIO1_A[0]	AB12	GPIO1_A[0]	uart0_sin			I/O	8	up	I	
GPIO1_A[1]	Y11	GPIO1_A[1]	uart0_sout			I/O	8	down	I	
GPIO1_A[2]	AA11	GPIO1_A[2]	uart0_cts_n			I/O	8	up	I	
GPIO1_A[3]	AC10	GPIO1_A[3]	uart0_rts_n			I/O	8	up	I	
GPIO4_C[0]	Y17	GPIO4_C[0]	smc_data0	trace_data0		I/O	4	up	I	
GPIO4_C[1]	W17	GPIO4_C[1]	smc_data1	trace_data1		I/O	4	up	I	
GPIO4_C[2]	W16	GPIO4_C[2]	smc_data2	trace_data2		I/O	4	up	I	
GPIO4_C[3]	T19	GPIO4_C[3]	smc_data3	trace_data3		I/O	4	up	I	
GPIO4_C[4]	V17	GPIO4_C[4]	smc_data4	trace_data4		I/O	4	up	I	SMC_VCC
GPIO4_C[5]	U19	GPIO4_C[5]	smc_data5	trace_data5		I/O	4	up	I	
GPIO4_C[6]	V19	GPIO4_C[6]	smc_data6	trace_data6		I/O	4	down	I	
GPIO4_C[7]	W18	GPIO4_C[7]	smc_data7	trace_data7		I/O	4	down	I	
GPIO4_D[0]	Y18	GPIO4_D[0]	smc_data8	trace_data8		I/O	4	down	I	

GPIO4_D[1]	AA18	GPIO4_D[1]	smc_data9	trace_data9		I/O	4	down	I	
GPIO4_D[2]	W20	GPIO4_D[2]	smc_data10	trace_data10		I/O	4	down	I	
GPIO4_D[3]	AB18	GPIO4_D[3]	smc_data11	trace_data11		I/O	4	down	I	
GPIO4_D[4]	U18	GPIO4_D[4]	smc_data12	trace_data12		I/O	4	down	I	
GPIO4_D[5]	AC19	GPIO4_D[5]	smc_data13	trace_data13		I/O	4	down	I	
GPIO4_D[6]	Y20	GPIO4_D[6]	smc_data14	trace_data14		I/O	4	down	I	
GPIO4_D[7]	AA20	GPIO4_D[7]	smc_data15	trace_data15		I/O	4	down	I	
GPIO0_C[7]	AB20	GPIO0_C[7]	trace_ctl	smc_addr3		I/O	4	down	I	
GPIO0_C[6]	T18	GPIO0_C[6]	trace_clk	smc_addr2		I/O	4	down	I	
GPIO0_D[5]	AC20	GPIO0_D[5]	i2s2_sdo	smc_addr1		I/O	4	down	I	
GPIO0_D[4]	V21	GPIO0_D[4]	i2s2_sdi	smc_addr0		I/O	4	down	I	
GPIO0_D[3]	W21	GPIO0_D[3]	i2s2_lrck_tx	smc_adv_n		I/O	4	up	I	
GPIO0_D[2]	Y21	GPIO0_D[2]	i2s2_lrck_rx	smc_oe_n		I/O	4	up	I	
GPIO0_D[0]	P19	GPIO0_D[0]	i2s2_clk	smc_csn0		I/O	4	up	I	
GPIO0_D[1]	P20	GPIO0_D[1]	i2s2_sclk	smc_we_n		I/O	4	up	I	
FLASH_DATA[0]	P18	FLASH_DATA[0]	emmc_data0			I/O	8	down	I	
FLASH_DATA[1]	AA21	FLASH_DATA[1]	emmc_data1			I/O	8	down	I	
FLASH_DATA[2]	AB21	FLASH_DATA[2]	emmc_data2			I/O	8	down	I	
FLASH_DATA[3]	W22	FLASH_DATA[3]	emmc_data3			I/O	8	down	I	
FLASH_DATA[4]	Y22	FLASH_DATA[4]	emmc_data4			I/O	8	down	I	
FLASH_DATA[5]	V20	FLASH_DATA[5]	emmc_data5			I/O	8	down	I	
FLASH_DATA[6]	AA22	FLASH_DATA[6]	emmc_data6			I/O	8	down	I	
FLASH_DATA[7]	AB22	FLASH_DATA[7]	emmc_data7			I/O	8	down	I	FLASH_VCC
FLASH_RDY	U20	FLASH_RDY				I/O	8	up	I	
FLASH_ALE	T20	FLASH_ALE				O	4	down	O	
FLASH_CLE	AC22	FLASH_CLE				O	4	down	O	
FLASH_RDN	N20	FLASH_RDN				O	8	up	O	
FLASH_WRN	AC23	FLASH_WRN				O	8	up	O	
FLASH_WP	AB23	FLASH_WP	emmc_pwr_en			O	4	down	O	
FLASH_CSN0	Y23	FLASH_CSN0				O	4	up	O	

GPIO4_B[0]	N18	GPIO4_B[0]	flash_csn1			I/O	4	up	I	
GPIO4_B[1]	U21	GPIO4_B[1]	flash_csn2	emmc_cmd		I/O	4	up	I	
GPIO4_B[2]	P21	GPIO4_B[2]	flash_csn3	emmc_rstn_out		I/O	4	up	I	
GPIO3_D[7]	N21	GPIO3_D[7]	flash_dqs	emmc_clkout		I/O	8	up	I	
GPIO3_B[6]	L20	GPIO3_B[6]	sdmmc0_detect_n			I/O	8	up	I	
GPIO3_B[7]	N19	GPIO3_B[7]	sdmmc0_write_prt			I/O	8	down	I	
GPIO3_A[6]	W23	GPIO3_A[6]	sdmmc0_rstn_out			I/O	8	up	I	
GPIO3_A[7]	V22	GPIO3_A[7]	sdmmc0_pwr_en			I/O	8	down	I	
GPIO3_B[0]	U22	GPIO3_B[0]	sdmmc0_clkout			I/O	4	down	I	
GPIO3_B[1]	P22	GPIO3_B[1]	sdmmc0_cmd			I/O	4	up	I	
GPIO3_B[2]	M21	GPIO3_B[2]	sdmmc0_data0			I/O	4	up	I	
GPIO3_B[3]	U23	GPIO3_B[3]	sdmmc0_data1			I/O	4	up	I	
GPIO3_B[4]	T21	GPIO3_B[4]	sdmmc0_data2			I/O	4	up	I	
GPIO3_B[5]	K20	GPIO3_B[5]	sdmmc0_data3			I/O	4	up	I	
GPIO0_A[7]	L21	GPIO0_A[7]	i2s0_sdi			I/O	8	down	I	
GPIO0_B[0]	T22	GPIO0_B[0]	i2s0_clk			I/O	4	down	I	
GPIO0_B[1]	T23	GPIO0_B[1]	i2s0_sclk			I/O	4	down	I	VCCIO0
GPIO0_B[2]	R22	GPIO0_B[2]	i2s0_lrck_rx			I/O	4	down	I	VCCIO1
GPIO0_B[3]	R21	GPIO0_B[3]	i2s0_lrck_tx			I/O	4	down	I	
GPIO0_B[4]	K21	GPIO0_B[4]	i2s0_sdo0			I/O	4	down	I	
GPIO0_B[5]	P23	GPIO0_B[5]	i2s0_sdo1			I/O	4	down	I	
GPIO0_B[6]	N23	GPIO0_B[6]	i2s0_sdo2			I/O	4	up	I	
GPIO0_B[7]	M22	GPIO0_B[7]	i2s0_sdo3			I/O	4	up	I	
GPIO1_B[2]	L22	GPIO1_B[2]	spdif_tx			I/O	4	down	I	
GPIO1_B[0]	N22	GPIO1_B[0]	uart2_sin			I/O	8	up	I	
GPIO1_B[1]	AB19	GPIO1_B[1]	uart2_sout			I/O	8	down	I	
GPIO2_D[6]	L23	GPIO2_D[6]	i2c1_sda			I/O	8	up	I	
GPIO2_D[7]	K22	GPIO2_D[7]	i2c1_scl			I/O	8	up	I	
GPIO3_A[0]	K23	GPIO3_A[0]	i2c2_sda			I/O	8	up	I	
GPIO3_A[1]	Y19	GPIO3_A[1]	i2c2_scl			I/O	8	up	I	

GPIO3_D[3]	L19	GPIO3_D[3]	uart3_sin			I/O	8	up	I	
GPIO3_D[4]	K19	GPIO3_D[4]	uart3_sout			I/O	8	down	I	
GPIO3_D[5]	K18	GPIO3_D[5]	uart3_cts_n			I/O	8	up	I	
GPIO3_D[6]	L18	GPIO3_D[6]	uart3_rts_n			I/O	8	up	I	
GPIO0_A[0]	AA19	GPIO0_A[0]	hdmi_hot_plug_in			I/O	8	down	I	
GPIO0_A[1]	Y16	GPIO0_A[1]	hdmi_i2c_scl			I/O	8	up	I	
GPIO0_A[2]	H19	GPIO0_A[2]	hdmi_i2c_sda			I/O	8	up	I	
GPIO0_A[3]	AA15	GPIO0_A[3]	pwm0			I/O	8	down	I	
GPIO0_A[4]	H21	GPIO0_A[4]	pwm1			I/O	8	down	I	
GPIO0_A[5]	J22	GPIO0_A[5]	otg_drv_vbus			I/O	8	down	I	
GPIO0_A[6]	H18	GPIO0_A[6]	host_drv_vbus			I/O	8	down	I	
GPIO0_D[6]	H20	GPIO0_D[6]	pwm2			I/O	8	down	I	
GPIO0_D[7]	J21	GPIO0_D[7]	pwm3			I/O	8	down	I	
TDO	H22	TDO				O	8	N/A	O	
TCK	H23	TCK				I	8	up	I	
TRST_N	G20	TRST_N				I	8	down	I	
TDI	G22	TDI				I	8	up	I	
TMS	G21	TMS				I/O	8	up	I	
GPIO2_D[4]	G19	GPIO2_D[4]	i2c0_sda			I/O	8	up	I	
GPIO2_D[5]	G18	GPIO2_D[5]	i2c0_scl			I/O	8	up	I	
GPIO6_B[4]	G23	GPIO6_B[4]				I/O	8	up	I	
Top Side										
DQ[7]	F20	DQ[7]				I/O	N/A	N/A	I	MVDD
DQ[6]	F22	DQ[6]				I/O	N/A	N/A	I	
DQ[5]	F21	DQ[5]				I/O	N/A	N/A	I	
DQ[4]	F19	DQ[4]				I/O	N/A	N/A	I	
DQS[0]	E22	DQS[0]				I/O	N/A	N/A	I	
DQS_B[0]	E23	DQS_B[0]				I/O	N/A	N/A	I	
DQ[3]	E18	DQ[3]				I/O	N/A	N/A	I	
DQ[2]	E20	DQ[2]				I/O	N/A	N/A	I	

DQ[1]	E21	DQ[1]				I/O	N/A	N/A	I	
DQ[0]	E17	DQ[0]				I/O	N/A	N/A	I	
DM[0]	D23	DM[0]				I/O	N/A	N/A	I	
VREF	F13	VREF				P	N/A	N/A	N/A	
DQ[23]	D22	DQ[23]				I/O	N/A	N/A	I	
DQ[22]	D21	DQ[22]				I/O	N/A	N/A	I	
DQ[21]	B23	DQ[21]				I/O	N/A	N/A	I	
DQ[20]	A23	DQ[20]				I/O	N/A	N/A	I	
DQS[2]	B22	DQS[2]				I/O	N/A	N/A	I	
DQS_B[2]	A22	DQS_B[2]				I/O	N/A	N/A	I	
DQ[19]	D17	DQ[19]				I/O	N/A	N/A	I	
DQ[18]	E16	DQ[18]				I/O	N/A	N/A	I	
DQ[17]	C22	DQ[17]				I/O	N/A	N/A	I	
DQ[16]	B21	DQ[16]				I/O	N/A	N/A	I	
DM[2]	C21	DM[2]				I/O	N/A	N/A	I	
ZQ_PIN	G15	ZQ_PIN				I/O	N/A	N/A	I	
ODT[1]	C20	ODT[1]				O	N/A	N/A	O	
ODT[0]	B20	ODT[0]				O	N/A	N/A	O	
A[14]	D16	A[14]				O	N/A	N/A	O	
A[13]	C19	A[13]				O	N/A	N/A	O	
A[12]	D19	A[12]				O	N/A	N/A	O	
A[11]	A20	A[11]				O	N/A	N/A	O	
A[10]	D18	A[10]				O	N/A	N/A	O	
A[9]	C18	A[9]				O	N/A	N/A	O	
A[8]	B19	A[8]				O	N/A	N/A	O	
A[7]	A19	A[7]				O	N/A	N/A	O	
A[6]	B18	A[6]				O	N/A	N/A	O	
A[5]	C17	A[5]				O	N/A	N/A	O	
CK	B16	CK				O	N/A	N/A	O	
CK_B	A16	CK_B				O	N/A	N/A	O	

A[4]	B17	A[4]				O	N/A	N/A	O	
A[3]	C15	A[3]				O	N/A	N/A	O	
A[2]	E14	A[2]				O	N/A	N/A	O	
A[1]	A17	A[1]				O	N/A	N/A	O	
A[0]	B15	A[0]				O	N/A	N/A	O	
BA[2]	C14	BA[2]				O	N/A	N/A	O	
BA[1]	B14	BA[1]				O	N/A	N/A	O	
BA[0]	A14	BA[0]				O	N/A	N/A	O	
RAS_B	D14	RAS_B				O	N/A	N/A	O	
CAS_B	D13	CAS_B				O	N/A	N/A	O	
WE_B	C13	WE_B				O	N/A	N/A	O	
CS_B[1]	E13	CS_B[1]				O	N/A	N/A	O	
CS_B[0]	B13	CS_B[0]				O	N/A	N/A	O	
CKE1	D11	CKE1				O	N/A	N/A	O	
CKE0	A13	CKE0				O	N/A	N/A	O	
RESET	C12	RESET				O	N/A	N/A	O	
DQ[15]	B12	DQ[15]				I/O	N/A	N/A	I	
DQ[14]	C11	DQ[14]				I/O	N/A	N/A	I	
DQ[13]	E11	DQ[13]				I/O	N/A	N/A	I	
DQ[12]	D10	DQ[12]				I/O	N/A	N/A	I	
DQS[1]	B11	DQS[1]				I/O	N/A	N/A	I	
DQS_B[1]	A11	DQS_B[1]				I/O	N/A	N/A	I	
DQ[11]	B10	DQ[11]				I/O	N/A	N/A	I	
DQ[10]	A10	DQ[10]				I/O	N/A	N/A	I	
DQ[9]	C10	DQ[9]				I/O	N/A	N/A	I	
DQ[8]	B9	DQ[8]				I/O	N/A	N/A	I	
DM[1]	C9	DM[1]				I/O	N/A	N/A	I	
DQ[31]	C8	DQ[31]				I/O	N/A	N/A	I	
DQ[30]	E10	DQ[30]				I/O	N/A	N/A	I	
DQ[29]	D8	DQ[29]				I/O	N/A	N/A	I	

DQ[28]	E8	DQ[28]				I/O	N/A	N/A	I	
DQS[3]	B8	DQS[3]				I/O	N/A	N/A	I	
DQS_B[3]	A8	DQS_B[3]				I/O	N/A	N/A	I	
DQ[27]	A7	DQ[27]				I/O	N/A	N/A	I	
DQ[26]	B7	DQ[26]				I/O	N/A	N/A	I	
DQ[25]	D7	DQ[25]				I/O	N/A	N/A	I	
DQ[24]	C7	DQ[24]				I/O	N/A	N/A	I	
DM[3]	E7	DM[3]				I/O	N/A	N/A	I	
HDMI_VDDLA	F7	1.1V				AP	N/A	N/A	N/A	HDMI Domain
HDMI_PVDD	F8	2.5V				AP	N/A	N/A	N/A	
HDMI_REXT	C6	HDMI_REXT				A	N/A	N/A	N/A	
HDMI_TXC_N	B5	HDMI_TXC_N				A	N/A	N/A	N/A	
HDMI_TXC	A5	HDMI_TXC				A	N/A	N/A	N/A	
HDMI_AVDD25	F8	2.5V				AP	N/A	N/A	N/A	
HDMI_TX0_N	B4	HDMI_TX0_N				A	N/A	N/A	N/A	
HDMI_TX0	A4	HDMI_TX0				A	N/A	N/A	N/A	
HDMI_TX1_N	B2	HDMI_TX1_N				A	N/A	N/A	N/A	
HDMI_TX1	A2	HDMI_TX1				A	N/A	N/A	N/A	
HDMI_TX2_N	B1	HDMI_TX2_N				A	N/A	N/A	N/A	
HDMI_TX2	A1	HDMI_TX2				A	N/A	N/A	N/A	
LCDC0_HSYNC	D6	LCDC0_HSYNC				I/O	4	N/A	I	LCD0_VCC0
LCDC0_DCLK	E6	LCDC0_DCLK				I/O	12	N/A	I	
LCDC0_VSYNC	D5	LCDC0_VSYNC				I/O	4	N/A	I	
LCDC0_DEN	D4	LCDC0_DEN				I/O	4	N/A	I	
LCDC0_DATA[0]	C4	LCDC0_DATA[0]				I/O	8	N/A	I	
LCDC0_DATA[1]	C3	LCDC0_DATA[1]				I/O	8	N/A	I	
LCDC0_DATA[2]	C2	LCDC0_DATA[2]				I/O	8	N/A	I	
LCDC0_DATA[3]	D3	LCDC0_DATA[3]				I/O	8	N/A	I	
LCDC0_DATA[4]	D1	LCDC0_DATA[4]				I/O	8	N/A	I	
LCDC0_DATA[5]	F5	LCDC0_DATA[5]				I/O	8	N/A	I	

LCDC0_DATA[6]	D2	LCDC0_DATA[6]				I/O	8	N/A	I	

Notes :

①: *Pad types : I = input , O = output , I/O = input/output (bidirectional) ,*
AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

②: *Output Drive Unit is mA , only Digital IO have drive value*

③: *Reset state : I = input without any pull resistor , O = output without any pull resistor ,*

④: *It is die location. For examples, "Left side" means that all the related IOs are always in left side of die*

⑤: *Power supply means that all the related IOs is in these IO power domain. If multiple powers is included, they are connected together in one IO power ring*

2.6 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2 -3 RK PX2 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	CLK32K	I	Clock input of 32.768KHz
	CPU_PWROFF	O	Request signal to external PMIC for power down CPU subsystem with dual-core Cortex-A9
	CORE_PWROFF	O	Request signal to external PMIC for SoC Core logic w/o Cortex-A9 subsystem and PMU logic
	BTMODE	I	Chip boot device select (BootRom)
	NPOR	I	Power on reset for chip

Interface	Pin Name	Direction	Description
Debug	TRST_N	I	JTAG interface reset input
	TCK	I	JTAG interface clock input/SWD interface clock input
	TDI	I	JTAG interface TDI input
	TMS	I/O	JTAG interface TMS input/SWD interface data out
	TDO	O	JTAG interface TDO output

Interface	Pin Name	Direction	Description
ETM Trace	trace_clk	O	Cortex-A8 ETM trace port clk
	trace_ctl	O	Cortex-A8 ETM trace port control
	trace_data*i*(*i*=0~15)	O	Cortex-A8 ETM trace port data

Interface	Pin Name	Direction	Description
USB OTG 2.0	OTG_DM	N/A	USB OTG 2.0 Data signal DM
	OTG_RKELVIN	N/A	USB OTG 2.0 Transmitter Kelvin Connection to Resistor Tune Pin
	OTG_DP	N/A	USB OTG 2.0 Data signal DP
	OTG_VBUS	N/A	USB OTG 2.0 5-V power supply pin
	otg_drv_vbus	O	USB OTG 2.0 drive VBUS

Interface	Pin Name	Direction	Description
USB Host 2.0	HOST_DM	N/A	USB HOST 2.0 Data signal DM
	HOST_RKELVIN	N/A	USB HOST 2.0 Transmitter Kelvin Connection to Resistor Tune Pin
	HOST_DP	N/A	USB HOST 2.0 Data signal DP
	HOST_VBUS	N/A	USB HOST 2.0 5-V power supply pin
	host_drv_vbus	O	USB HOST 2.0 drive VBUS

Interface	Pin Name	Direction	Description
SD/MMC Host Controller	sdmmc_clkout	O	sdmmc card clock.
	sdmmc_cmd	I/O	sdmmc card command output and reponse input.
	sdmmc_data*i* (*i*=0~3)	I/O	sdmmc card data input and output.
	sdmmc_detect_n	I	sdmmc card detect signal, a 0 represents presence of card.
	sdmmc_write_prt	I	sdmmc card write protect signal, a 1 represents write is protected.
	sdmmc_rstn_out	O	sdmmc card reset signal
	sdmmc_pwr_en	O	sdmmc card power-enable control signal

Interface	Pin Name	Direction	Description
NandC	FLASH_WP	O	Flash write-protected signal
	FLASH_ALE	O	Flash address latch enable signal
	FLASH_CLE	O	Flash command latch enable signal
	FLASH_WRN	O	Flash write enable and clock signal
	FLASH_RDN	O	Flash read enable and write/read signal
	FLASH_DATA[*i*](*i*=0~7)	I/O	Low 8bits of flash data inputs/outputs signal
	flash_data*i*(*i*=8~15)	I/O	High 8bits of flash data inputs/outputs signal
	flash_dqs	I/O	Flash data strobe signal
	FLASH_RDY	I	Flash ready/busy signal
	FLASH0_CSN	O	Flash chip enable signal for chip 0
	flash_csn*i*(*i*=1~7)	O	Flash chip enable signal for chip i, i=1~7

Interface	Pin Name	Direction	Description
SDIO Host Controller	sdio_clkout	O	sdio card clock.
	sdio_cmd	I/O	sdio card command output and reponse input.
	sdio_data*i* (*i*=0~3)	I/O	sdio card data input and output.
	sdio_detect_n	I	sdio card detect signal, a 0 represents presence of card.
	sdio_write_prt	I	sdio card write protect signal, a 1 represents write is protected.
	sdio_pwr_en	O	sdio card power-enable control signal
	sdio_int_n	O	sdio card interrupt indication
	sdio_backend	O	the back-end power supply for embedded device

Interface	Pin Name	Direction	Description
I2C	i2c0_sda	I/O	I2C0 data
	i2c0_scl	I/O	I2C0 clock
	i2c1_sda	I/O	I2C1 data
	i2c1_scl	I/O	I2C1 clock
	i2c2_sda	I/O	I2C2 data

	i2c2_scl	I/O	I2C2 clock
	i2c3_sda	I/O	I2C3 data
	i2c3_scl	I/O	I2C3 clock
	i2c4_sda	I/O	I2C4 data
	i2c4_scl	I/O	I2C4 clock

Interface	Pin Name	Direction	Description
eMMC Interface	emmc_clkout	O	emmc card clock.
	emmc_cmd	I/O	emmc card command output and reponse input.
	emmc_data*i* (*i*=0~7)	I/O	emmc card data input and output.
	emmc_pwr_en	O	emmc card power-enable control signal
	emmc_rstn_out	O	emmc card reset signal

Interface	Pin Name	Direction	Description
HSADC Interface	hsadc_clkout	O	hsadc/tsi/gps reference clock
	hsadc_data*i* (*i*=0~9)	I	hsadc(i=0~9)/tsi(i=0~7)/gps data(i=0,1)
	ts_sync	I	ts synchronizer signal

Interface	Pin Name	Direction	Description
DMC	CK	O	Active-high clock signal to the memory device.
	CK_B	O	Active-low clock signal to the memory device.
	CKE*i* (*i*=0,1)	O	Active-high clock enable signal to the memory device for two chip select.
	CS_B*i* (*i*=0,1)	O	Active-low chip select signal to the memory device. AThere are two chip select.
	RAS_B	O	Active-low row address strobe to the memory device.
	CAS_B	O	Active-low column address strobe to the memory device.
	WE_B	O	Active-low write enable strobe to the memory device.
	BA[2:0]	O	Bank address signal to the memory device.
	A[15:0]	O	Address signal to the memory device.
	DQ[31:0]	I/O	Bidirectional data line to the memory device.
	DQS[3:0]	I/O	Active-high bidirectional data strobes to the memory device.
	DQS_B[3:0]	I/O	Active-low bidirectional data strobes to the memory device.
	DM[3:0]	O	Active-low data mask signal to the memory device.
	ODT*i* (*i*=0,1)	O	On-Die Termination output signal for two chip select.
	RET_EN	I	Active-low retention latch enable input
	RESET	O	DDR3 reset signal to the memory device

	VREF*i* (*i*=0,1,2,3)	I/O	Reference Voltage input for three regions of DDR IO
	ZQ_PIN	I/O	ZQ calibration pad which connects 240ohm±1% resistor

Interface	Pin Name	Direction	Description
SMC	smc_oe_n	O	SMC output enable signal.
	smc_bls_n*i* (*i*=0,1)	O	SMC byte lane strobe signal for two bytes.
	smc_we_n	O	SMC write enable signal.
	smc_csn*i* (*i*=0,1)	O	SMC chip enable signal.
	smc_adv_n	O	SMC address valid signal in shared mode
	smc_addr*i* (*i*=0~19)	O	SMC address signal.
	smc_data*i* (*i*=0~15)	I/O	SMC directional data line to memory device.

Interface	Pin Name	Direction	Description
I2S/PCM0 Controller (8 channel)	i2s0_clk	O	I2S/PCM0 clock source
	i2s0_sclk	I/O	I2S/PCM0 serial clock
	i2s0_lrck_rx	I/O	I2S/PCM0 left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s0_sdi	I	I2S/PCM0 serial data input
	i2s0_sdo*i* *(i=0,1,2,3)*	O	I2S/PCM0 serial data ouput
	i2s0_lrck_tx	I/O	I2S/PCM0 left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode *(i=0)* and the beginning of a group of left & right channels in PCM mode *(i=0,1)*

Interface	Pin Name	Direction	Description
I2S/PCM1 Controller (2 channel)	i2s1_clk	O	I2S/PCM1 clock source
	i2s1_sclk	I/O	I2S/PCM1 serial clock
	i2s1_lrck_rx	I/O	I2S/PCM1 left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s1_sdi	I	I2S/PCM1 serial data input
	i2s1_sdo	O	I2S/PCM1 serial data ouput
	i2s1_lrck_tx	I/O	I2S/PCM1 left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode

Interface	Pin Name	Direction	Description
I2S/PCM2 Controller (2 channel)	i2s2_clk	O	I2S/PCM2 clock source
	i2s2_sclk	I/O	I2S/PCM2 serial clock
	i2s2_lrck_rx	I/O	I2S/PCM2 left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s2_sdi	I	I2S/PCM2 serial data input
	i2s2_sdo	O	I2S/PCM2 serial data ouput
	i2s2_lrck_tx	I/O	I2S/PCM2 left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode

Interface	Pin Name	Direction	Description
SPDIF transmitter	spdif_tx	O	spdif biphase data ouput

Interface	Pin Name	Direction	Description
SPI Controller	spi*x*_clk*(x=0,1)*	I/O	spi serial clock
	spi*x*_csn*y* *(x=0,1)(y=0,1)*	I/O	spi chip select signal,low active
	spi*x*_txd*(x=0,1)*	O	spi serial data output
	spi*x*_rxd*(x=0,1)*	I	spi serial data input

Interface	Pin Name	Direction	Description
PWM	pwm3	O	Pulse Width Modulation output
	pwm2	O	Pulse Width Modulation output
	pwm1	O	Pulse Width Modulation output
	pwm0	O	Pulse Width Modulation output

Interface	Pin Name	Direction	Description
UART	uart0_sin	I	UART0 searial data input
	uart0_sout	O	UART0 searial data output
	uart0_cts_n	I	UART0 clear to send
	uart0_rts_n	O	UART0 request to send
	uart1_sin	I	UART1 searial data input
	uart1_sout	O	UART1 searial data output
	uart1_cts_n	O	UART1 clear to send
	uart1_rts_n	I	UART1 request to send
	uart2_sin	I	UART2 searial data input
	uart2_sout	O	UART2 searial data output
	uart3_sin	I	UART3 searial data input
	uart3_sout	O	UART3 searial data output
	uart3_cts_n	I	UART3 clear to send
	uart3_rts_n	O	UART3 request to send

Interface	Pin Name	Direction	Description
LCDC0	LCDC0_DCLK	O	LCDC0 RGB interface display clock out, MCU i80 interface RS signal
	LCDC0_VSYNC	O	LCDC0 RGB interface vertival sync pulse, MCU i80 interface CSN signal
	LCDC0_HSYNC	O	LCDC0 RGB interface horizontial sync pulse, MCU i80 interface WEN signal
	LCDC0_DEN	O	LCDC0 RGB interface data enable, MCU i80 interface REN signal
	LCDC0_DATA[23:0]	I/O	LCDC0 data output/input

Interface	Pin Name	Direction	Description

LCDC1	lcdc1_dclk	O	LCDC1 RGB interface display clock out, MCU i80 interface RS signal
	lcdc1_vsync	O	LCDC1 RGB interface vertival sync pulse, MCU i80 interface CSN signal
	lcdc1_hsync	O	LCDC1 RGB interface horizontial sync pulse, MCU i80 interface WEN signal
	lcdc1_den	O	LCDC1 RGB interface data enable, MCU i80 interface REN signal
	lcdc1_data[23:0]	I/O	LCDC1 data output/input

Interface	Pin Name	Direction	Description
Camera IF0	CIF0_CLKIN	I	Camera0 interface input pixel clock
	cif0_clkout	O	Camera0 interface output work clock
	CIF0_VSYNC	I	Camera0 interface vertical sync signal
	CIF0_HREF	I	Camera0 interface horizontial sync signal
	cif0_data[1:0]	I	Camera0 interface low 2-bit input pixel data
	CIF0_DATAIN[9:2]	I	Camera0 interface middle 8-bit input pixel data
	cif0_data[11:10]	I	Camera0 interface high 2-bit input pixel data

Interface	Pin Name	Direction	Description
Camera IF1	cif1_clkin	I	Camera1 interface input pixel clock
	cif1_clkout	O	Camera1 interface output work clock
	cif1_vsync	I	Camera1 interface vertical sync signal
	cif1_href	I	Camera1 interface horizontial sync signal
	cif1_data[11:0]	I	Camera1 interface 12-bit input pixel data

Interface	Pin Name	Direction	Description
RMII	rmii_clkout	O	RMII REC_CLK output
	rmii_clkin	I	RMII REF_CLK input
	rmii_tx_en	O	rmii transfer enable
	rmii_txd1	O	rmii transfer data
	rmii_txd0	O	rmii transfer data
	rmii_rx_err	I	rmii receive error
	rmii_crs_dvalid	I	rmii carrier sense / receive data valid input
	rmii_rxd1	I	rmii receive data
	rmii_rxd0	I	rmii receive data
	mii_md	I/O	mii management interface data
	mii_mdclk	O	mii management interface clock

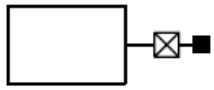
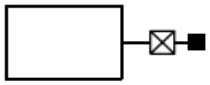
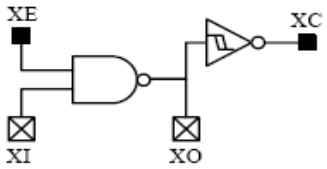
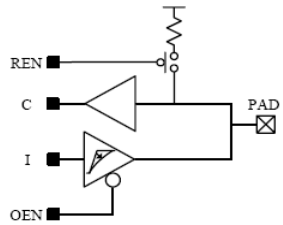
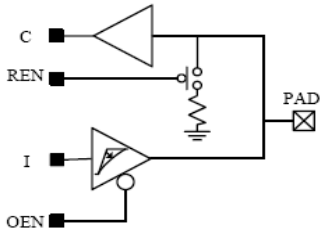
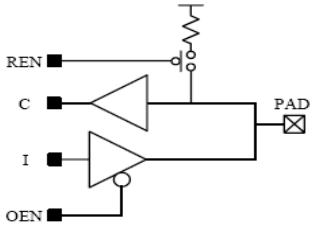
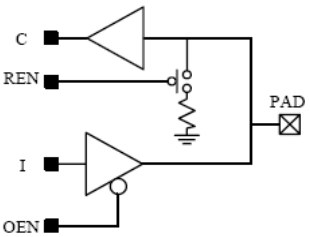
Interface	Pin Name	Direction	Description
SAR-ADC	SARADC_AIN[i] (i=0~3)	N/A	SAR-ADC input signal for 4 channel

Interface	Pin Name	Direction	Description
eFuse	EFUSE_VDDQ	N/A	eFuse program and sense power

2.7 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO .

Table 2-4 RK PX2 IO Type List

Type	Diagram	Description	Pin Name
A		Analog IO Cell with IO voltage	EFUSE_VDDQ
B		Dedicated Power supply to Internal Macro with IO voltage	SARADC_AIN[3:0]
C		Crystal Oscillator with high enable	XIN24M/XOUT24M
D		Tri-state output pad with input, limited slew rate and enable controlled pull-up	Part of digital GPIO
E		Tri-state output pad with input, limited slew rate and enable controlled pull-down	Part of digital GPIO
F		Tri-state output pad with input, and enable controlled pull-up	Part of digital GPIO
G		Tri-state output pad with input, and enable controlled pull-down	Part of digital GPIO

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 RK PX2 absolute maximum ratings

Paramerters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	AVDD, CVDD, PVDD, OTG_DVDD, HOST_DVDD	1.5	V
DC supply voltage for Digital GPIO (except for SAR-ADC, TS-ADC, PLL, USB, DDR IO)	LCD0_VCC0,LCD0_VCC1, LCD1_VCC, CIF0_VCC,CIF1_VCC, PVCC, AP0_VCC,AP1_VCC, SMC_VCC,FLASH_VCC, VCCIO_0,VCCIO_1	3.6	V
DC supply voltage for DDR IO	MVDD	1.65	V
DC supply voltage for Analog part of SAR-ADC/TS-ADC	VDDA_SARADC, VDDA_TSADC	2.75	V
DC supply voltage for Analog part of PLL	AVDD_APLL,AVDD_DPLL, AVDD_CGPLL	1.21	V
DC supply voltage for Analog part of USB OTG/Host2.0	OTG_VDD25,HOST_VDD25 OTG_VDD33,HOST_VDD33	2.75 3.63	V
DC supply voltage for Analog part of HDMI	HDMIVDD HDMIAVDD	1.21 2.75	V
DC supply voltage for Analog part of EFUSE	EFUSE_VDDQ	2.75	V
Analog Input voltage for SAR-ADC		2.75	V
Analog Input voltage for TS-ADC		2.75	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5	V
Analog input voltage for RKELVIN/ID of USB OTG/Host2.0		2.75	V
Digital input voltage for input buffer of GPIO		3.6	V
Digital output voltage for output buffer of GPIO		3.6	V
Storage Temperature		125	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Conditions

Table 3-2 RK PX2 recommended operating conditions

Parameters	Symbol	Min	Typ	Max	Units
Internal digital logic Power （except USB OTG)	AVDD, CVDD, PVDD	0.99	1.10	**1.45**	V
eFuse Power(3.3V)	EFUSE_VDDQ	3	3.3	3.6	V

Digital GPIO Power(3.3V/1.8V)	VCCIO0,VCCIO1, LCD0_VCC0, LCD0_VCC1, LCD1_VCC, SMC_VCC, CIF0_VCC,CIF1_VCC, PVCC, FLASH_VCC, AP0_VCC, AP1_VCC	3 1.62	3.3 1.8	3.6 1.98	V
DDR IO (DDR3 mode) Power	MVDD	1.425	1.5	1.575	V
DDR IO (LPDDR2 mode) Power	MVDD	1.14	1.2	1.30	V
DDR IO (LVDDR3 mode) Power	MVDD	1.28	1.35	1.45	V
DDR reference supply (VREF) Input	VREF	0.49*MVDD	0.5*MVDD	0.51*MVDD	V
DDR External termination voltage		VREF - 40mV	VREF	VREF + 40mV	V
PLLAnalog Power	AVDD_APLL, AVDD_DPLL, AVDD_CGPLL	0.99	1.1	1.21	V
SAR-ADC Analog Power	VDDA_SARADC	2.25	2.5	2.75	V
TS-ADC Analog Power	VDDA_TSADC	2.25	2.5	2.75	V
USB OTG/Host2.0 Digital Power	OTG_DVDD, HOST_DVDD	1.023	1.1	1.21	V
USB OTG/Host2.0 Analog Power(2.5V)	OTG_VDD25,HOST_VDD25	2.325	2.5	2.75	V
USB OTG/Host2.0 Analog Power(3.3V)	OTG_VDD33,HOST_VDD33	3.069	3.3	3.63	V
USB OTG/Host2.0 external resistor	REXT	42.768	43.2	43.632	Ohm
CPU Core Max frequency			1.4G		Hz
PLL input clock frequency		N/A	24	N/A	MHz
Operating Temperature		-40	25	85	℃

3.3 DC Characteristics

Table 3-3 RK PX2 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	V_{il}	-0.3	0	0.8	V
	Input High Voltage	V_{ih}	2	3.3	3.6	V
	Output Low Voltage	V_{ol}	N/A	0	0.4	V
	Output High Voltage	V_{oh}	2.4	3.3	N/A	V
	Threshold Point	V_t	1.34	1.46	1.6	V
	Threshold Point with Pullup Resistor Enabled	V_{tpu}	1.2	1.31	1.45	V
	Threshold Point with Pulldown Resistor Enabled	V_{tpd}	1.71	1.84	1.97	V
	Pullup Resistor	R_{pu}	41	60	91	Kohm
	Pulldown Resistor	R_{pd}	43	63	103	Kohm

Digital GPIO @1.8V	Input Low Voltage	V_{il}	-0.3	0	0.63	V
	Input High Voltage	V_{ih}	1.17	1.8	3.6	V
	Output Low Voltage	V_{ol}	N/A	0	0.45	V
	Output High Voltage	V_{oh}	1.35	1.8	N/A	V
	Threshold Point	V_t	0.77	0.84	0.92	V
	Threshold Point with Pullup Resistor Enabled	V_{tpu}	0.77	0.84	0.91	V
	Threshold Point with Pulldown Resistor Enabled	V_{tpd}	0.77	0.85	0.92	V
	Pullup Resistor	R_{pu}	79	129	218	Kohm
	Pulldown Resistor	R_{pd}	73	127	233	Kohm
DDR IO @DDR3 mode	Input High Voltage	V_{ih_ddr}	VREF + 0.1	N/A	MVDD	V
	Input Low Voltage	V_{il_ddr}	-0.3	N/A	VREF - 0.1	V
	Output High Voltage	V_{oh_ddr}	0.8 * MVDD	N/A	N/A	V
	Output Low Voltage	V_{ol_ddr}	N/A	N/A	0.2 * MVDD	V
	Input termination resistance(ODT) to VDDIO_BLi/2 (i=0~3)	R_{tt}	100 54 36	120 60 40	140 66 44	Ohm
DDR IO @LPDDR2 mode	Input High Voltage	V_{ih_ddr}	VREF + 0.13	N/A	MVDD	V
	Input Low Voltage	V_{il_ddr}	-0.3	N/A	VREF- 0.13	V
	Output High Voltage	V_{oh_ddr}	0.9 * MVDD	N/A	N/A	V
	Output Low Voltage	V_{ol_ddr}	N/A	N/A	0.1 * MVDD	V

3.4 Electrical Characteristics for General IO

Table 3-5 RK PX2 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Input leakage current	I_i	Vin = 3.3V or 0V	-10	N/A	10	uA
	Tri-state output leakage current	I_{oz}	Vout = 3.3V or 0V	-10	N/A	10	uA
	High level input current	I_{ih}	Vin = 3.3V, pulldown disabled	TBD	N/A	TBD	uA
			Vin = 3.3V, pulldown enabled	32	52	77	uA
	Low level input current	I_{il}	Vin = 0V, pullup disabled	TBD	N/A	TBD	uA
			Vin = 0V, pullup enabled	36	55	80	uA
Digital GPIO @1.8V	Input leakage current	I_i	Vin = 1.8V or 0V	-10	N/A	10	uA
	Tri-state output leakage current	I_{oz}	Vout = 1.8V or 0V	-10	N/A	10	uA
	High level input current	I_{ih}	Vin = 1.8V, pulldown disabled	TBD	N/A	TBD	uA
			Vin = 1.8V, pulldown enabled	7.7	14	25	uA
	Low level input current	I_{il}	Vin = 0V, pullup disabled	TBD	N/A	TBD	uA
			Vin = 0V, pullup enabled	8.3	14	23	uA

3.5 Electrical Characteristics for PLL

Table 3-6 RK PX2 Electrical Characteristics for PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Input clock frequency	F_{in}	$F_{in} = F_{ref} * NR$① @1.1V	0.183	24	1400	MHz
Comparison frequency	F_{ref}	$F_{ref} = F_{in} / NR$ @1.1V	0.183	N/A	1400	MHz
VCO operating range	F_{VCO}	$F_{VCO} = F_{ref} * NF$① @1.1V	300	N/A	1400	MHz
Output clock frequency	F_{out}	$F_{out} = F_{VCO} / NO$① @1.1V	18.75	N/A	1400	MHz
Lock time	T_{lt}	(NR * 500)/ F_{in} @1.1V	N/A	N/A	N/A	N/A
Power consumption	N/A	F_{out} = 750MHz, NO = 1 @1.1V	N/A	3	N/A	mA

Notes : ①: *NR is the input divider value;*
NF is the feedback divider value;
NO is the output divider value

3.6 Electrical Characteristics for SAR-ADC

Table 3-7 RK PX2 Electrical Characteristics for SAR-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution	N		N/A	10	N/A	bits
Analog Supply Voltage	VDDIO		2.25	2.5	2.75	V
Digital Supply Voltage	VDDCore		1.0	1.1	1.2	V
Conversion speed	F_S	The duty cycle should be between 40%~60%	N/A	N/A	1	MSPS
Analog Supply Current	IAVDD		N/A	200	N/A	uA
Digital Supply Current	IDVDD		N/A	50	N/A	uA
Number of Channels	NCH AVDD		N/A	8	N/A	N/A
Differential Non Linearity	DNL		N/A	±1	N/A	LSB
Integral Non Linearity	INL		N/A	±2	N/A	LSB
Gain Error	E_{gain}		-8	N/A	8	LSB
Offset Error	E_{offset}		-8	N/A	8	mV
Power Down Current	ISHDN	From AVDD	N/A	0.5	N/A	uA
		From DVDD	N/A	0.5	N/A	uA
Power up time			N/A	7	N/A	$1/F_S$

3.7 Electrical Characteristics for TS-ADC

Table 3-8 RK PX2 Electrical Characteristics for TS-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Analog Supply Voltage	AVDD		2.25	2.5	2.75	V
Digital Supply Voltage	DVDD		1.0	1.1	1.2	V
TSADC Accuracy			N/A	N/A	±5	C
Quiescent Current	IQ	From AVDD	N/A	180	N/A	uA
		From DVDD	N/A	40	N/A	uA
Power Down Current	ISHDN	From AVDD	N/A	1	N/A	uA
		From DVDD	N/A	5	N/A	uA
Number of Channels (Differential)		7 external, 1 internal	N/A	8	N/A	N/A

Clock Frequency	F_{clk}		N/A	N/A	50.0	KHz
Power up time			N/A	N/A	7	TCLK
Latency			N/A	N/A	1	TCLK

3.8 Electrical Characteristics for USB OTG/Host2.0 Interface

Table 3-9 RK PX2 Electrical Characteristics for USB OTG/Host2.0 Interface

Parameters		Test condition	Min	Typ	Max	Units
HS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_DVDD	75℃ , OTG_VDD25 = HOST_VDD25 = 2.5V, OTG_VDD33 = HOST_VDD33 = 3.3V, OTG_DVDD = HOST_DVDD = 1.1V , 15-cm USB cable attached to DP/DM	N/A	5.35	N/A	mA
	Current From OTG_VDD33		N/A	2.50	N/A	mA
	Current From OTG_VDD25		N/A	21.2	N/A	mA
HS transmit, minimum transition density (all 1's data in DP/DM)	Current From OTG_DVDD		N/A	4.07	N/A	mA
	Current From OTG_VDD33		N/A	2.25	N/A	mA
	Current From OTG_VDD25		N/A	17	N/A	mA
HS idle mode	Current From OTG_DVDD		N/A	5.4	N/A	mA
	Current From OTG_VDD33		N/A	2.22	N/A	mA
	Current From OTG_VDD25		N/A	6.23	N/A	mA
FS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_DVDD		N/A	3.25	N/A	mA
	Current From OTG_VDD33		N/A	16.5	N/A	mA
	Current From OTG_VDD25		N/A	6.47	N/A	mA
LS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_DVDD		N/A	3.62	N/A	mA
	Current From OTG_VDD33		N/A	16.9	N/A	mA
	Current From OTG_VDD25		N/A	6.39	N/A	mA
Suspend mode	Current From OTG_DVDD		N/A	61.2	N/A	uA
	Current From OTG_VDD33		N/A	0.1	N/A	uA
	Current From OTG_VDD25		N/A	17.0	N/A	uA
Sleep mode	Current From OTG_DVDD		N/A	0.2	N/A	mA
	Current From OTG_VDD33		N/A	0.1	N/A	uA
	Current From OTG_VDD25		N/A	0.348	N/A	mA

3.9 Electrical Characteristics for DDR IO

Table 3-10 RK PX2 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
DDR IO @DDR3 mode	DDR IO power standby current, ODT OFF		@ 1.5V , 125℃	N/A	0.02	14.47	uA
	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	N/A	0.02	5.06	uA
DDR IO @LPDDR2 mode	Input leakage current		@ 1.2V , 125℃	N/A	0.01	4.51	uA
	VDD quiescent current		@ 1.1V , 125℃	N/A	0.02	4.21	uA
	DDR IO power quiescent current		@ 1.2V , 125℃	N/A	0.02	12.31	uA

3.10 Electrical Characteristics for eFuse

Table 3-11 RK PX2 Electrical Characteristics for eFuse

	Parameters	Symbol	Test condition	Min	Typ	Max	Units
Active mode	read current for eFuse digital core logic(1.1V)	I_{load_vdd}	STROBE high	2.537	4.049	5.695	mA
	read current for eFuse digital core logic (1.1V)	I_{active_vdd}	normal read 10MHz	1.498	2.368	3.308	mA
standby mode	standby current for eFuse digital core logic (1.1V)	$I_{standby\_vdd}$		0.057	0.255	0.492	uA

3.11 Electrical Characteristics for HDMI

Table 3-12 RK PX2 Electrical Characteristics for HDMI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
2.5V Supply Voltage	VDDH	2.5±10%	2.25	2.5	2.75	V
1.1V Supply Voltage	VDDL	1.1±10%	0.99	1.0	1.21	V
REXT Resistance Error	DREXT	470ohms	-1	0	1	%
D2-0[9:0] Setup Time	TSU	To TMDS_CK	700	N/A	N/A	ps
D2-0[9:0] Hold Time	THLD	To TMDS_CK	700	N/A	N/A	ps
MSENS detect voltage for monitor connection	VCNCT	(VTXC+VTXC_N) / 2	2	N/A	N/A	V
MSENS detect voltage for monitor disconnection	VDISC	(VTXC+VTXC_N) / 2	N/A	N/A	0.4	V
MSENS response time	TMSENS		3	N/A	15	us
OSC minimum oscillation frequency when f(IDCK)=0Hz	FMINDDC	IDCK=L	20	30	40	MHz
Supply Current (2.5V)	IDDH		N/A	N/A	TBD	mA
Supply Current (1.1V)	IDDL		N/A	N/A	TBD	mA
Activation Time From Sleep	TACT		N/A	N/A	1	ms

Chapter 4 Hardware Guideline

4.1 Reference design for RK PX2 oscillator PCB connection

RK PX2 only uses one oscillator, and its typical clock frequency is 24MHz. The oscillator will provide input clock to four on-chip PLLs.

- External reference circuit for oscillators with 24MHz input

In the following diagram , the value for Rf,Rd,C1,C2 must be adjusted a little to improve performance of oscillator based on real crystal model . Especially C1 and C2 value is advised to meet formula (C1 * C2)/(C1+C2) = ~8pF

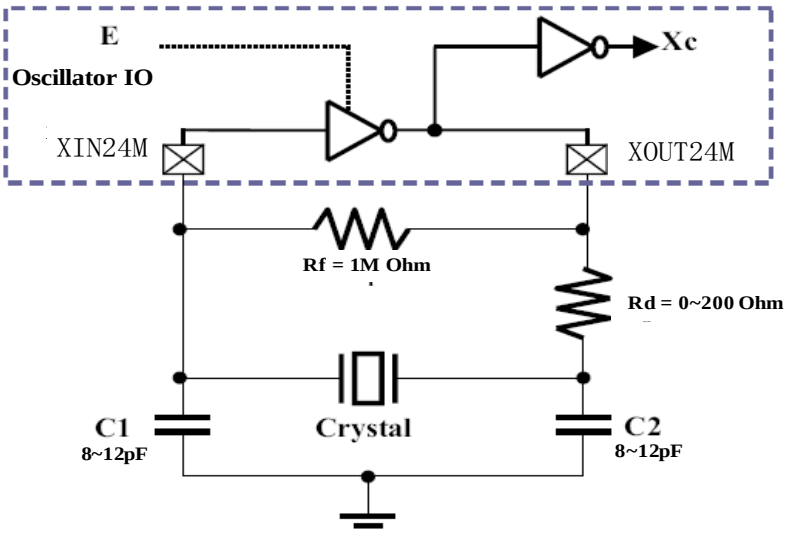


Fig.4 -1 RK PX2 Ball Mapping Diagram

4.2 Reference design for PLL PCB connection

The following reference design is suitable for PLL in RK PX2.

The PLL's two analog supplies should be filtered with two series ferrite beads and two shunt 0.1uF and 0.01uF capacitors. The ferrite on VSS is preferred but optional. Adding the ferrite on VSS converts supply noise to substrate noise as seen by the PLL. The PLLs are designed to be relatively insensitive to supply and substrate noise, so the presence of this ferrite is a second order issue.

The VDD/VSS is mapped to VDD_APLL/VSS_APLL, VDD_DPLL/VSS_DPLL and VDD_CGPLL/VSS_CGPLL.

The AVDD/AVSS is mapped to AVDD_APLL/AVSS_APLL, AVDD_DPLL/ AVSS_DPLL and AVDD_CGPLL/AVSS_CGPLL.

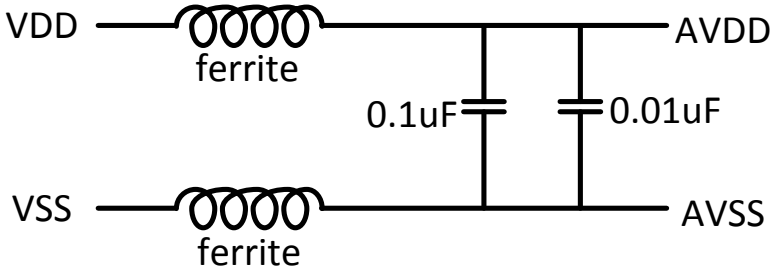


Fig. 4-2 External reference circuit for PLL

The ferrite beads should be similar one of the following from Murata:

Table 4-1 Ferrite Bead Selection

Part number	R@DC	Z@10MHz	Z@100MHz	size
BLM18EG601SN1	0.35	200	600	0603
BLM18PG471SN1	0.2	130	470	0603
BLM18KG601SN1	0.15	160	600	0603
BLM18AG601SN1	0.38	180	600	0603
BLM18AG102SN1	0.5	280	1000	0603
BLM18TG601TN1	0.45	190	600	0603
BLM15AG601SN1	0.6	200	600	0402
BLM15AX601SN1	0.34	190	600	0402
BLM15AX102SN1	0.49	250	1000	0402
BLM03AX601SN1	0.85	120	600	0201

Similar ferrite beads are also available from Panasonic. The keycharacteristics to select are:

- DC resistance less than 0.40 ohms
- impedance at 10MHz equal to or greater 180 ohms
- impedance at 100MHz equal to or greater than 600 ohms

The capacitors should be mounted as close to the package balls aspossible.

4.3 Reference design for USB OTG/Host2.0 connection

In RK PX2 there are USB OTG and USB Host2.0 interface, in fact, same interface is for them.The following diagram shows external reference design. Of course, for USB Host2.0some signals can be removed based on different application.

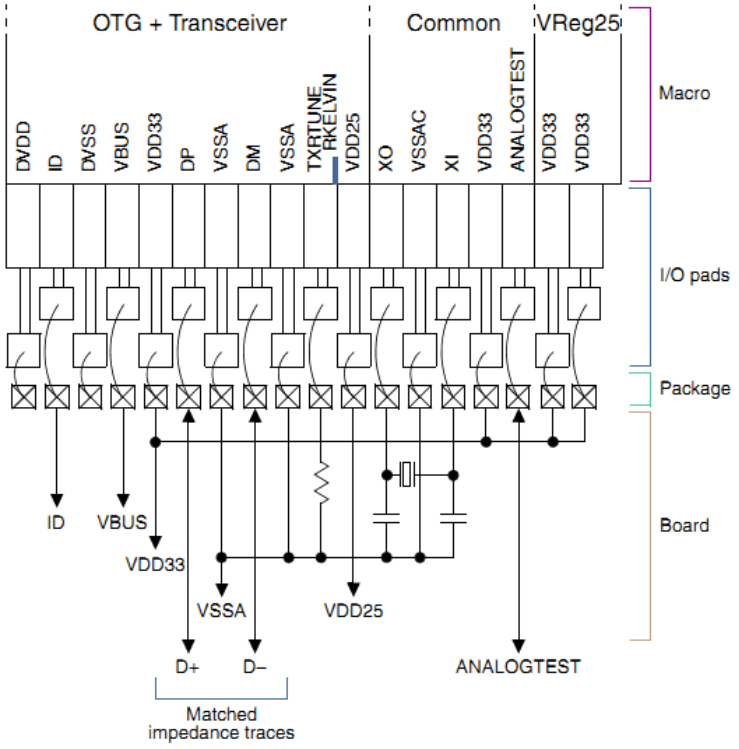


Fig. 4-3 RK PX2 USB OTG/Host2.0 interface reference connection

4.4 Power up/down sequence requirement

For all of the power supply in RK PX2, there is no any specific requirement of power up/down sequence except power supply between core logic and DDR3/LPDDR2 IO or digital GPIO , between USB OTG/Host2.0 power supply .

- Power supply sequence for core logic(CVDD/AVDD/PVDD) and DDR3/LPDDR2 IO (MVDD)

It is generally recommended that the core logic and DDR IO be powered-up together, and it is also acceptable for core logic supply to power-up a very short time before the DDR IO supply. If DDR IO supply must power-up before the core logic supply, it is advised to keep the time between these two events less than 100ms to limit excessive DDR IO current draws.

- Power supply sequence for core logic(CVDD/AVDD/PVDD) and digital GPIO power①

It is generally recommended that "turn on the higher GPIO voltage first and then the lower core voltage" so that the crowbar current would not occur on the power-up stage.

Also it is acceptable that "turn on the lower core voltage first and then higher GPIO voltage" only if the GPIO control pins are set to a fixed state. However, the ramp-up time for them can not be less than 10us.

There is no requirement on the power-down sequence for two above groups. Customers can decide which voltage to be down first based on the application need.

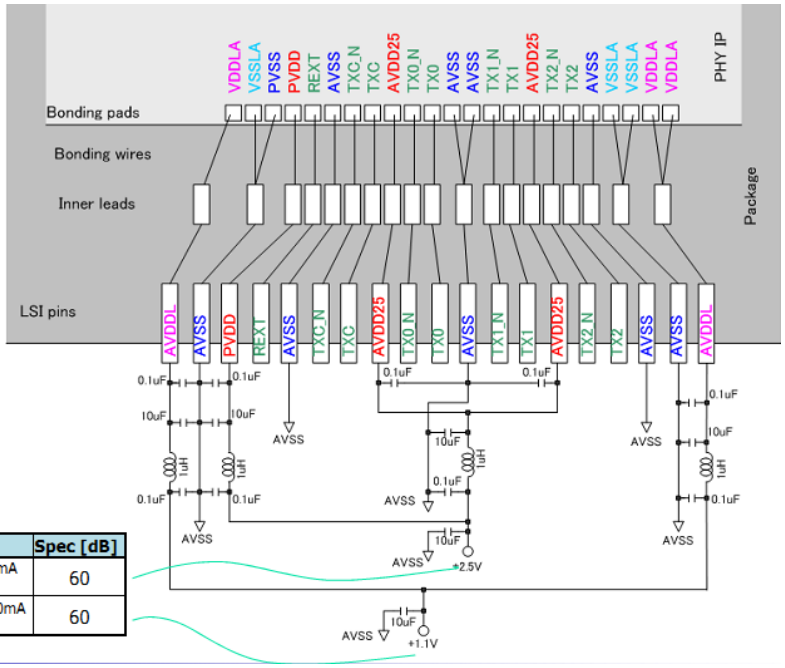
- Power supply sequence for USB OTG/Host2.0

There is no requirement on the power-up and power-down sequence for the USB power supply USBDVDD_1V1(1.1V), USBVDD_1V8(1.8V) and USBVDD_3V3(3.3V). Customers can decide which voltage to be up and down first based on the application, it is recommended that the time duration between supply ramps be kept as short as possible.

Notes :①: digital GPIO power include LCD0_VCCj, LCD1_VCC, CIFj_VCC, PVCC, APj_VCC, SMC_VCC, FLASH_VCC, VCCIOj.

4.5 Reference design for HDMI Tx PHY connection

In RK PX2, the following diagram shows external PCB reference design for HDMI Tx PHY.



Following table is the recommended supply power specifications.

PSRR (Ripple Rejection)

Power Supply	Conditions	Spec [dB]
+2.5V Power	Vin = 2.5V, Iload = 20mA f = 1KHz	60
+1.1V Power	Vin = 2.5V, Iload = 100mA f = 1KHz	60

Fig. 4-3 RK PX2 HDMI interface reference connection

4.6 Power on reset descriptions

The following figure shows power-on-reset sequence. External power-on-reset input signal NPOR is released after stabilization of oscillator input clock XIN24M. Internal signal sysrstn is

generated after NPOR is filtered glitch , which can filter out 5 clock cycles(24MHz) for low pulse of NPOR, so 208ns low pulse of NPOR will not be recognized as valid power-on-reset signal for RK PX2.

To make PLLs work normally, the internal power down signal(pllpd) for PLLs must be high after power-on-reset, and maintains high level for more than 1us after sysrstn is deasserted. Then PLL reset signals(pllrstn) are asserted for about 10.6us, and PLLs start to lock when pllrstn deassert, and consume about to 1330us to lock.

So the system will wait about 1330us, then deactive internal reset signal chiprstn, which is used to control generation logic of all the clock inside CRU.

After 256 cycles or about 10.7us , rstn_pre for reset signal of all internal IPs will be deasserted , in other words, about 10.7us of clock has been generated before reset of every internal module is released.

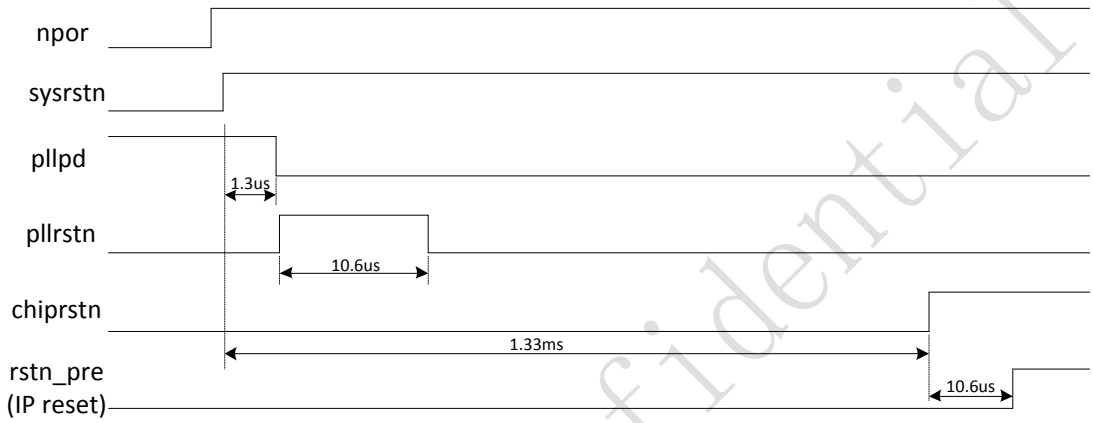


Fig. 4-4 RK PX2 reset signals sequence

Chapter 5 Thermal Management

5.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RKPX2 has to be below 110ºC.

Depending on the thermal mechanical design (Smartphone, Tablet, Personal Navigation Device, etc), the system thermal management software and worst case thermal applications, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level (Smartphone, Tablet, Personal Navigation Device, etc) with the measured power of the worst case UC of the device.

5.2 Package Thermal Characteristics

Table 5-1 provides the thermal resistance characteristics for the package used on this device，

Table 5-13 Thermal Resistance Characteristics

PACKAGE	POWER(W)	$\theta_{JA}(℃/W)$	$\theta_{Jb}(℃/W)$	$\theta_{Jc}(℃/W)$
RKPX2	3.73	16.1	9.2	5.1

Note: The testing PCB is base on 6 layers, 90mmX90mm, 1 mm Thickness the max Tj is 125 ºC and ambient temperature of 65 ºC