primarion

An Infineon Technologies Company

Sychronous Rectified Buck MOSFET Driver IC

PX3515

Datasheet

Applications

- Core power regulation for Intel® and AMD® µprocessors
- High current DC-DC converters
- POL power converters for memory, DSP, FPGA, ASIC

Features

- Dual MOSFET driver for synchronous rectified bridge converters
- Adjustable high-side and low-side MOSFET gate drive voltages for optimal efficiency
  - High-side VCC (7V to 12V)
  - Low-side PVCC (5V to 12V)
- Integrated bootstrap diode for reduced part count
- Adaptive gate drive control prevents cross-conduction
- Fast rise and fall times supports switching rates of up to 2MHz
- Capable of sinking more than 4A peak current for low switching losses
- Three-state PWM input for output stage shutdown
- VCC under-voltage protection
- Lead-free (RoHS compliant) SOIC and DFN packages

Ordering Information

Part Number	Ambient	Package
PX3515BDDG	0 to 85°C	10-lead DFN

Description

The PX3515 is a dual high speed driver designed to drive a wide range of high-side and low-side power N-channel MOSFETs in synchronous rectified buck converters. When combined with the Primarion PX35XX family of Digital Multi-phase Controllers or PX75XX Digital Point of Load (Di-POL™) Controllers and N-channel MOSFETs, the PX3515 forms a complete core-voltage regulator solution for advanced micro and graphics processors as well as point-of-load applications.

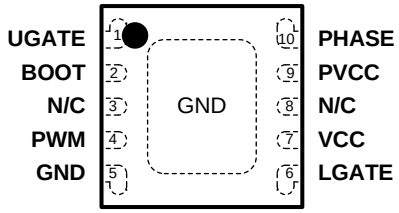
The PX3515 provides the capability of driving the high-side gate and low-side gate with independent drive voltages over a range from 7V to 12V (high-side VCC) and 5V to 12V (low-side PVCC). This provides the flexibility necessary to optimize applications involving trade-offs between gate charge and conduction losses.

Adaptive zero shoot-through protection is integrated into the IC which prevents both upper and lower MOSFETs from conducting simultaneously and to minimize dead time. The PX3515 has small propagation delay from input to output with fast rise and fall times.

The PX3515 drivers also feature a three-state PWM input which, when used together with Primarion's Digital Controllers, eliminates the need for Schottky diodes that are often used in systems to protect the load from reversed output voltage events.

PX3515 DFN Package

10-pin DFN (TOP VIEW)



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Functional Block Diagram

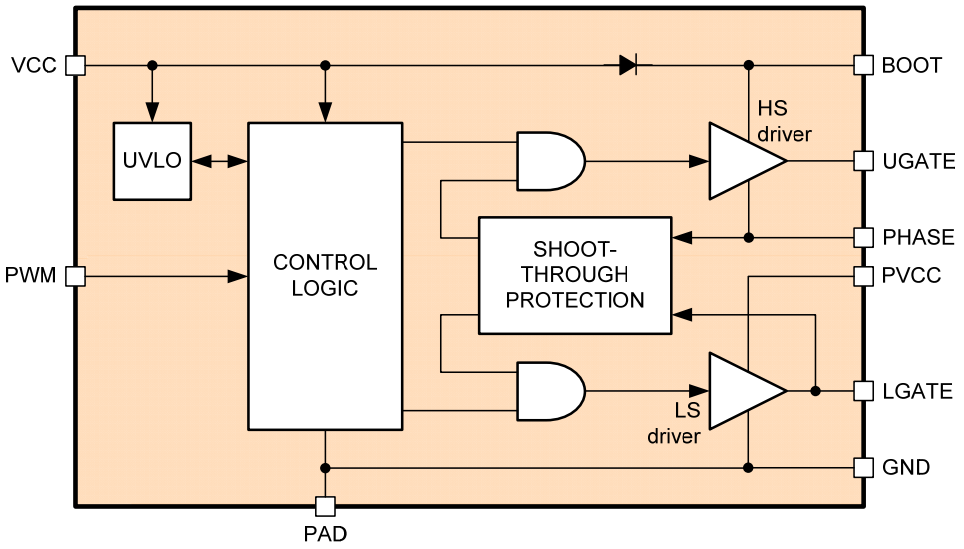


Figure 1. Block Diagram

Typical Application

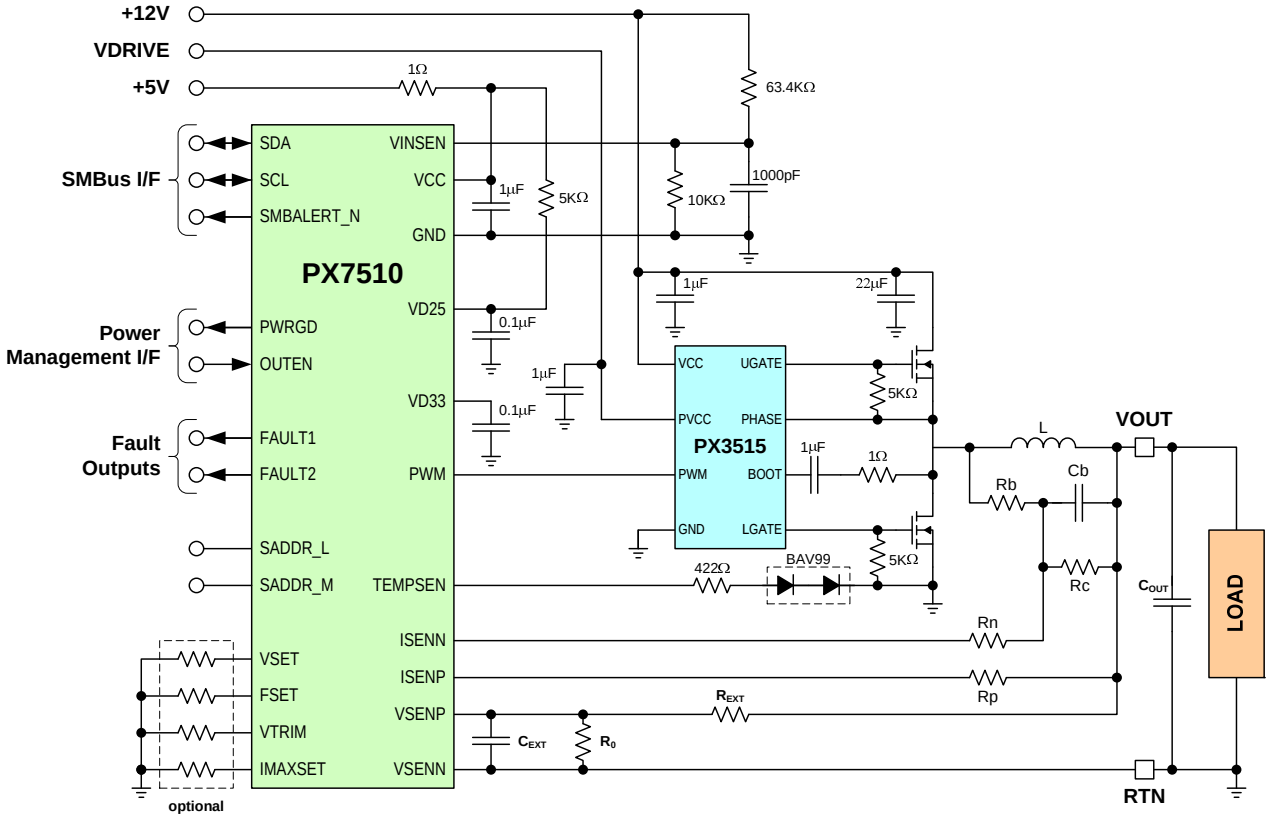


Figure 2. Single-Phase Application with PX7510 DiPOL Controller

Absolute Maximum Ratings

Stresses above those listed in Table 1 “Absolute Maximum Ratings” may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this specification.

Table 1. Absolute Maximum Ratings[1]

Symbol	Description	Min	Max	Units	Conditions
V_{VCC}	VCC supply voltage (DC)	-0.3	25	V	
V_{PVCC}	PVCC supply voltage (DC)	-0.3	25	V	
V_{BOOT}	BOOT voltage	-0.3	45	V	Referenced to GND
V_{BOOT} - V_{PHASE}	BOOT to PHASE voltage	-0.3	25	V	Referenced to PHASE
V_{PHASE}	PHASE voltage, DC	-1	25	V	DC
V_{PHASE}	PHASE voltage, pulsed	-20	30	V	Pulsed (500ns, 2% max duty cycle)
V_{PWM}	Input voltage	-0.3	6.3	V	
	UGATE	V_{PHASE} – 0.3	V_{BOOT} + 0.3	V	
	LGATE	-0.3	V_{PVCC} + 0.3	V	
	ESD, Human Body Model	4000		V	JEDEC JESD22-A114-E
	ESD, Charged Device Model	1000		V	JEDEC JESD22-C101-C
	ESD, Machine Model	300		V	JEDEC JESD22-A115-A
T_J	Junction temperature	-25	150	°C	
T_{STG}	Storage temperature	-55	150	°C	

Notes:

1. At T_J = 25°C, unless otherwise specified

Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Symbol	Description	Min	Nom	Max	Units
V_{VCC}	VCC supply voltage	+7.0	+12.0	+13.2	V
V_{PVCC}	PVCC supply voltage	+4.5	+12.0	+13.2	V
f_{PWM}	PWM signal transition frequency	0.1		2	MHz
T_J	Junction temperature	0		125	°C
$T_{AMBIENT}$	Operating ambient temperature	0		85	°C
$\theta_{JA(0)}$	Thermal resistance, junction-to-air, note 2		48		°C/W
θ_{JC}	Thermal resistance, junction-to-case, note 3		7		°C/W

Notes:

2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air
3. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the underside of the package

Electrical Characteristics

Operating conditions: VCC = +12.0V, PVCC = +12.0V, T_A = 25°C, unless otherwise specified.

Table 3. Electrical Characteristics

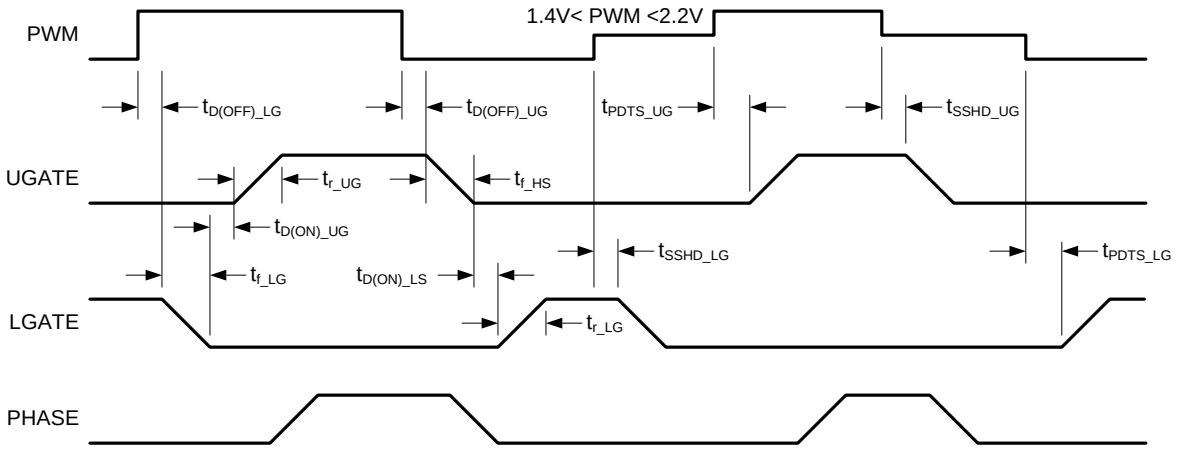
Parameter	Conditions	Symbol	Min	Typ	Max	Units
Supply Characteristics						
VCC supply current	f_{PWM} = 1MHz, no load	I_{VCC}		6		mA
PVCC supply current	f_{PWM} = 1MHz, no load	I_{PVCC}		5.5		mA
Quiescent current	$1.4 \le V_{PWM} \le 2.2$	$I_{PVCCQ}+I_{VCCQ}$		1.9		mA
VCC rising threshold	dv/dt < 2.5 kV/s			6.2	6.7	V
VCC falling threshold			4.8	5.6		V
VCC hysteresis			400	650	950	mV
PWM Input						
Input current	V_{PWM} = +3.3V	I_{PWM_H}		450		µA
	V_{PWM} = 0V	I_{PWM_L}		-530		µA
Sink/source impedance		R_{PWM}		3.5		kΩ
Shutdown window (3-state)	minimum pulse of 25ns	V_{PWM_SD}	1.4		2.2	V
PWM open threshold		V_{PWM_O}	1.6	1.8	2.0	V
PWM rising threshold		V_{PWM_H}	2.6			V
PWM falling threshold		V_{PWM_L}			1.0	V
PWM input slew rate		SR_{PWM}	5			V/µs
Minimum pulse width high side	pulse width on PWM	t_{min_PWM}		40		ns
Upper Gate (UGATE) Output						
Shutdown hold off time	Note 4, 3nF load	t_{PDTS_UG}		25	40	ns
UGATE rise time	Note 4, 3nF load	t_{r_UG}		20		ns
UGATE fall time	Note 4, 3nF load	t_{f_UG}		15		ns
3-state rising propagation delay	Note 4, 3nF load	t_{TSSHD_UG}		25	45	ns
UGATE turn-on propagation delay	Note 4, 3nF load	$t_{D(ON)\_UG}$		25		ns
UGATE turn-off propagation delay	Note 4, 3nF load	$t_{D(OFF)\_UG}$		25		ns
Lower Gate (LGATE) Output						
Shutdown hold-off time	Note 4, 3nF load	t_{PDTS_LG}		20	35	ns
LGATE rise time	Note 4, 3nF load	t_{r_LG}		20		ns
LGATE fall time	Note 4, 3nF load	t_{f_LG}		15		ns
3-state rising propagation delay	Note 4, 3nF load	t_{TSSHD_LG}		20	45	ns
LGATE turn-on propagation delay	Note 4, 3nF load	$t_{D(ON)\_LG}$		20		ns
LGATE turn-off propagation delay	Note 4, 3nF load	$t_{D(OFF)\_LG}$		20		ns
Output Characteristics (note 3)						
Upper drive source current	current pulse < 20ns	I_{SRC_UG}	4			A
Upper drive source impedance	Note 5, I_{SRC_UG} = 2A	R_{SRC_UG}		1		Ω
Upper drive sink current	current pulse < 20ns	I_{SNK_UG}	4			A
Upper drive sink impedance		R_{SNK_UG}		0.9	1.3	Ω
Lower drive source current	current pulse < 40ns	I_{SRC_LG}	4			A
Lower drive source impedance	Note 6, I_{SRC_UG} = 2A	R_{SRC_LG}		1.4		Ω
Lower drive sink current	current pulse < 40ns	I_{SNK_LG}	4			A
Lower drive sink impedance		R_{SNK_LG}	-	0.9	1.3	Ω

Notes:
4. Guaranteed by design, verified during characterization
5. Incremental resistance $V_{BOOT} – V_{UG}$ = 4.3V @ I_{SRC} = 2A
6. Incremental resistance $V_{VCC} – V_{BG}$ = 4.4V @ I_{SRC} = 2A

Table 4. Pin Function Description

Pin #	Name	Description
1	UGATE	Upper gate drive output. Connect to the gate of high-side power N-channel MOSFET
2	BOOT	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section herein for guidance in choosing the capacitor value.
3	N/C	No connection
4	PWM	The PWM signal is the control input for the driver and is to be connected to the PWM output of the controller. The PWM signal can enter three distinct states during operation. See the 3-state PWM input section herein for further details.
5	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver.
6	LGATE	Lower gate drive output. Connect to the gate of the low-side power N-channel MOSFET
7	VCC	This pin supplies power to the upper gate , Its operating range is +6V to +12V. Place a high quality low ESR ceramic capacitor from this pin to GND.
8	N/C	No connection
9	PVCC	This pin supplies power to the lower gate , Its operating range is +6.7V to +12V. Place a high quality low ESR ceramic capacitor from this pin to GND.
10	PHASE	Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate drive.
Die paddle		Connect pad to the power circuit board power ground plane (GND), use thermal vias

Timing Diagram



Layout Considerations

The parasitic inductances of the PCB and of the power devices' packaging (both upper and lower MOSFETs) can cause serious ringing, exceeding absolute maximum rating of the devices. Careful layout can help minimize such unwanted stress. The following advice is meant to lead to an optimized layout:

- Keep decoupling loops (PVCC-GND and BOOT-PHASE) as short as possible.
- Minimize trace inductance, especially on low-impedance lines. All power traces (UGATE, PHASE, LGATE, GND, PVCC) should be short and wide, as much as possible.
- Minimize the inductance of the PHASE node. Ideally, the source of the upper and the drain of the lower MOSFET should be as close as thermally allowable.
- Minimize the current loop of the output and input power trains. Short the source connection of the lower MOSFET to ground as close to the transistor pin as feasible. Input capacitors (especially ceramic decoupling) should be placed as close to the drain of upper and source of lower MOSFETs as possible.

To optimize heat spreading, copper should be placed directly underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried copper plane(s) with thermal vias. This combination of vias for vertical heat escape, extended copper plane, and buried planes for heat spreading allows the IC to achieve its full thermal potential

Physical Characteristics (10-lead 3mm x 3mm DFN package)

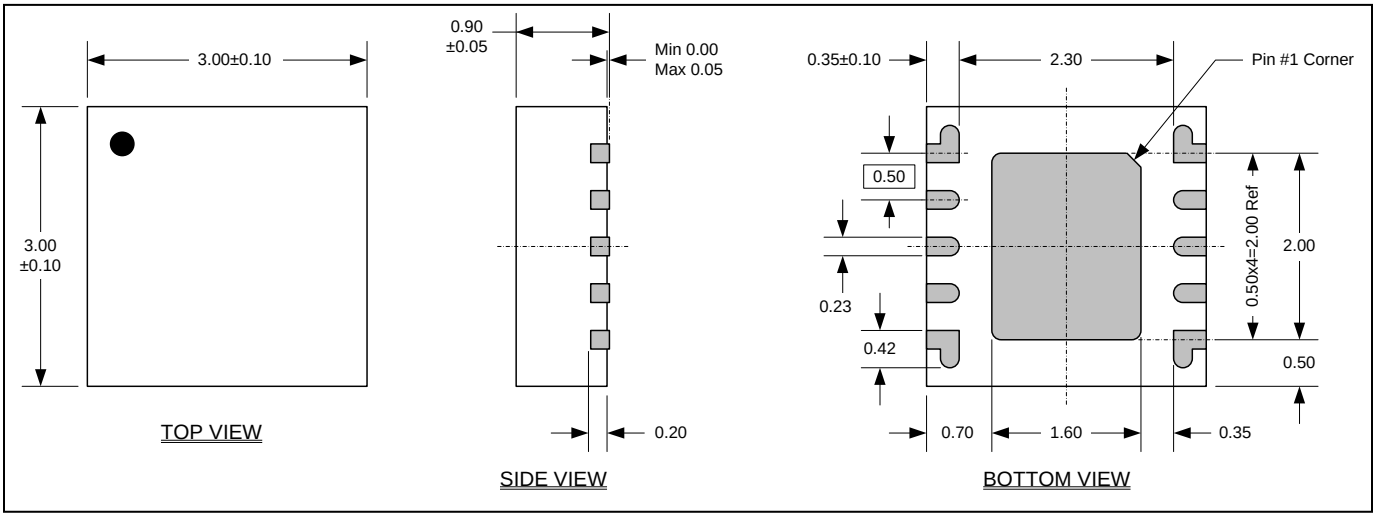
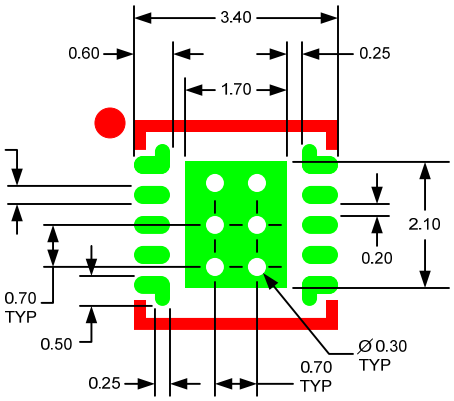
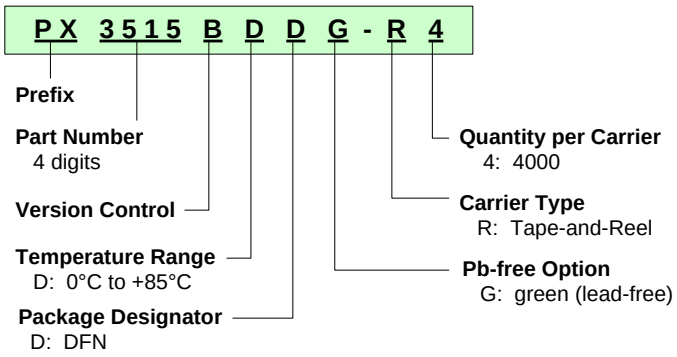


Figure 3. Physical dimensions.

Suggested land pattern



Ordering Information



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