Synchronous Rectified Buck MOSFET driver IC

PX3519

Datasheet

Revision 2.3, 2015-10-21

Power Management and Multimarket

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.0	2013-07-17 first issue
Revision 2.1	2014-08-21 changes:
	Table 5 page 8: PHASE voltage, pulsed Minimum to -12V
Revision 2.2	2014-09-19 changes:
	R_{PHASE} added in the Simplified Block Diagram
	SOA diagram for R_{PHASE} introduced
Revision 2.3	2015-10-21 changes:
	➔ Power up and power down sequence introduced
	➔ Junction operating temperature from -25°C to -40°C table 1 and table 7

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Last Trademarks Update 2010-06-09

1 Applications

- Desktop and Server VR12.X Vcore and non-Vcore buck-converters
- Network and Telecom uncontrolled processor VR
- Single Phase and Multiphase POL
- CPU/GPU Regulation in Notebook, Graphics Cards and Gaming
- Voltage Modules requiring high power density
- Memory (DDR2/3)

2 Features

- High frequency operation: up to 1.2MHz
- Capability to drive MOSFET for 50A per phase
- Wide VCC input voltage range: 4.5V to 9V
- Wide input voltage range: up to 13.2V
- Low power dissipation
- Includes bootstrap diode
- Gate disable pin for fast low side switch off
- Adaptive shoot through protection
- Compatible to standard +3.3V controller.
- Tri-state PWM input functionality
- Small package: 3mmx3mm VDSON-8
- RoHS compliant

Table 1 Product Identification

Part Number	Temp Range	Package	Marking
PX3519	-40 to 125°C	3x3 8-leads VDSON-8	3519

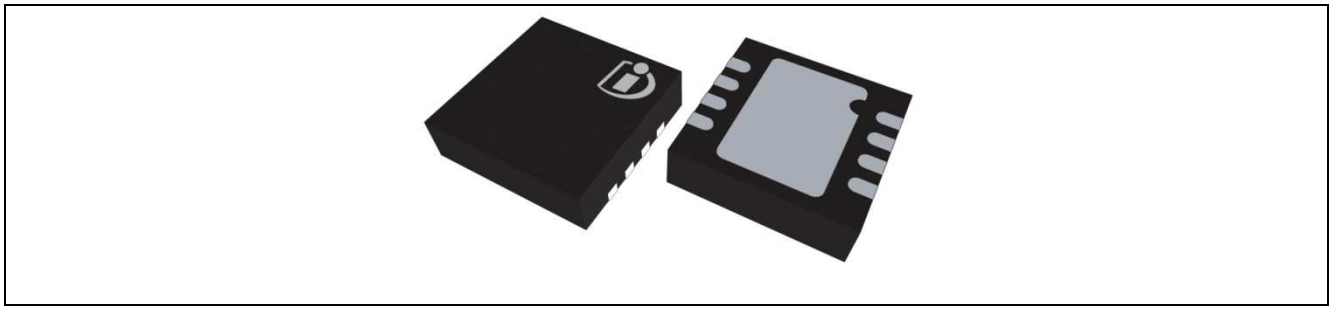


Figure 1 Picture of the product

3 Description

3.1 Pinout

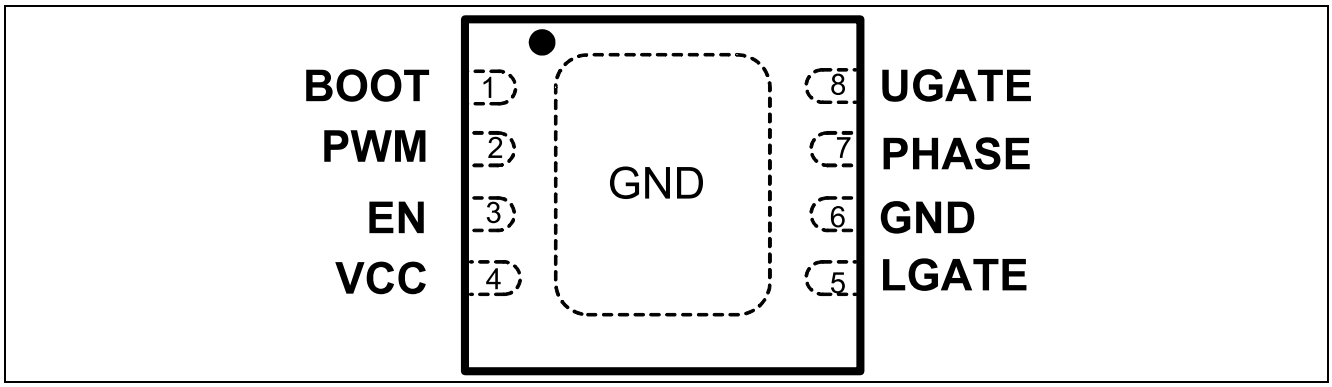


Figure 2 Pinout, numbering and name of pins (transparent top view)

Table 2 I/O Signals

Pin No.	Name	Pin Type	Buffer Type	Function
1	BOOT	O	Analog	**Floating bootstrap supply pin for the upper gate drive**. Connect the bootstrap capacitor [1)] between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section herein for guidance in choosing the capacitance value.
2	PWM	I	Logic	**PWM drive logic input** Connect this pin to the PWM output from the controller.
3	EN	I	Logic	**Enable signal** Used to activate the device. When connected to high level the status of the driver outputs (UGATE, LGATE), is determined by the PWM. When connected to low level the driver outputs are disabled regardless of signal levels on PWM input. EN input must be driven high or low and must not be left floating.
5	LGATE	O	Analog	**Low side gate signal** Connect to the gate of the low-side power N-channel MOSFET
7	PHASE	I	Analog	**Return path for the upper gate driver.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate drive.
8	UGATE	O	Analog	**Upper gate drive output.** Connect to the gate of high-side power N-channel MOSFET

[1)] See section 5.2 for guidance in choosing capaciatance value

Table 3 Power Supply

Pin No.	Name	Pin Type	Buffer Type	Function
4	VCC	POWER	-	**Supply for housekeeping/logic and driver sections power to the IC.** Connect to +4.5V – 8V. Place a high quality low ESR ceramic capacitor from this pin to GND.

Table 4 Ground Pins

Pin No.	Name	Pin Type	Buffer Type	Function
6	GND	GND	-	**GND connection.** Can be left open since main GND connection to circuit board is via die pad. Must not be used as single ground connection.
-	Die Pad	GND	-	**Bias and reference ground.** All signals are referenced to this node. It is also the power ground return of the driver. It is mandatory to connect the die paddle electrically and thermally to the circuit board.

3.2 General description

The PX3519 is a dual high speed driver designed to drive a wide range of high-side and low-side power N-channel MOSFETs in synchronous rectified buck converters. When combined with the Infineon PX38xx/PX88xx family of Digital Multi-phase Controllers or PX75xx Digital Point of Load (DiPOL™) Controllers and N-channel MOSFETs, the PX3519 forms a complete core-voltage regulator solution for advanced micro and graphics processors as well as point-of-load applications. The PX3519 provides the capability of driving the high-side gate and low-side gate with a variable gate driving voltage, ranging from 4.5V up to 8V, to tailor the efficiency of the system based on the customer conditions and needs.The input voltage for the power stage can range from 5V up to 13.2V. Adaptive shoot-through protection is integrated into the IC which prevents both upper and lower MOSFETs from conducting simultaneously while minimizing dead time. An enable pin is provided to switch off the outputs of the driving stage.

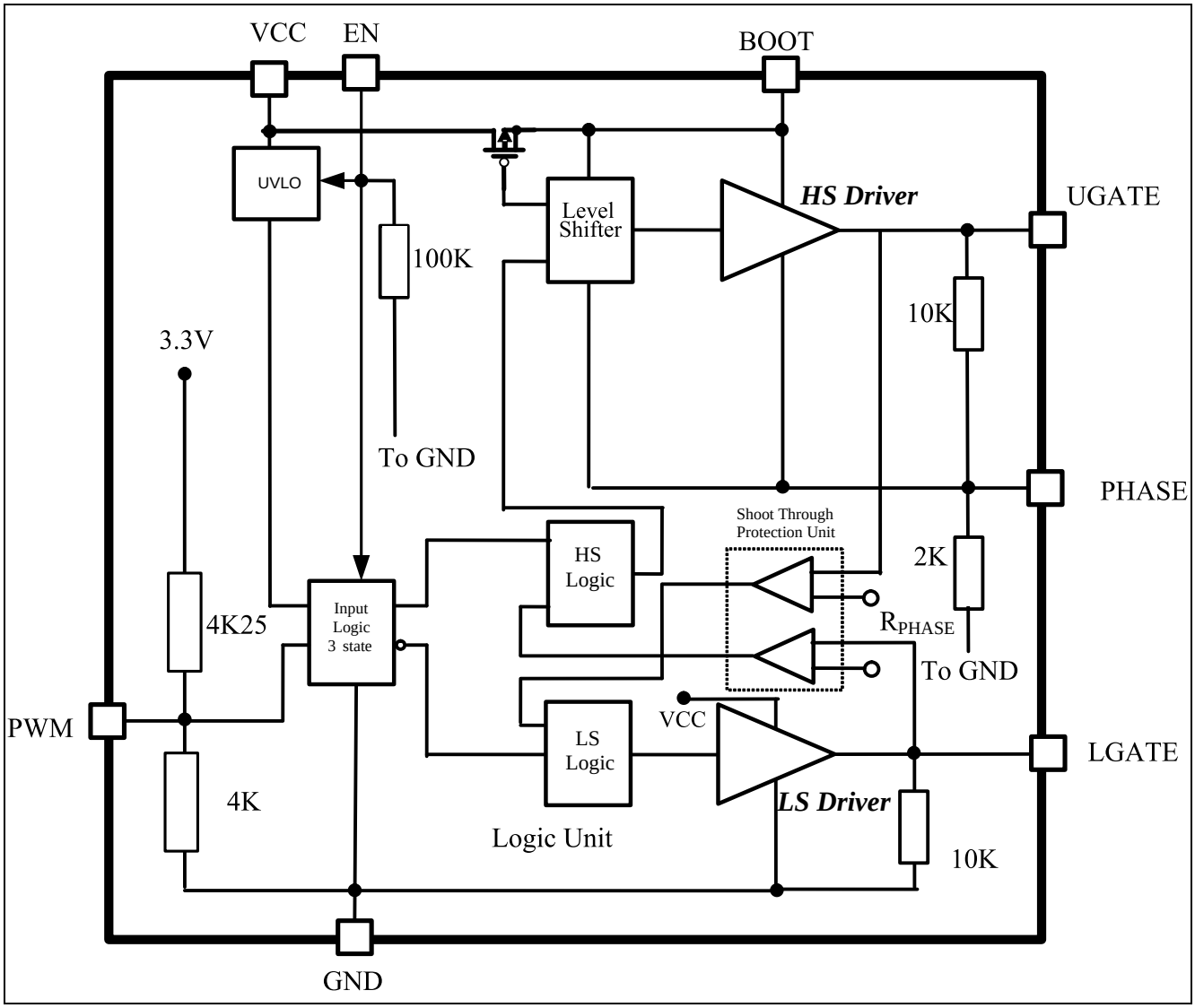


Figure 3 Simplified block diagram

4 Electrical specification

4.1 Absolute Maximum Ratings

Stresses above those listed in Table 5 “Absolute Maximum Ratings” may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational sections of this specification. Exposure to the absolute maximum ratings for extended periods may adversely affect the operation and reliability of the device.

Table 5 Absolute Maximum Ratings (Tambient =25°C)

Parameter	Symbol	Values			Unit	Note / Test Conditions
		Min.	Typ.	Max.		
VCC supply voltage (DC)	V_{VCC}	-0.3		9	V	
BOOT voltage, DC	V_{BOOT}	-0.3		25	V	
BOOT voltage, pulsed	V_{BOOT}	-0.3		30	V	
BOOT to PHASE voltage	V_{BOOT} - V_{PHASE}	-0.3		9	V	
PHASE voltage, DC	V_{PHASE}	-1		16	V	
PHASE voltage, pulsed	V_{PHASE}	-12		25	V	2)
LGATE voltage, DC	L_{GATE}	-0.3		9.3	V	
HGATE voltage to PHASE, DC	H_{GATE} - V_{PHASE}	-0.3		9.3	V	
V_{PWM}				3.6	V	
EN	V_{EN}			3.6	V	
Junction temperature	T_{Jmax}	-40	–	150	°C	–
Storage temperature	T_{STG}	-55	–	150	°C	–

2) The pulse duration is 2ns for the minimum and 10ns for the maximum.

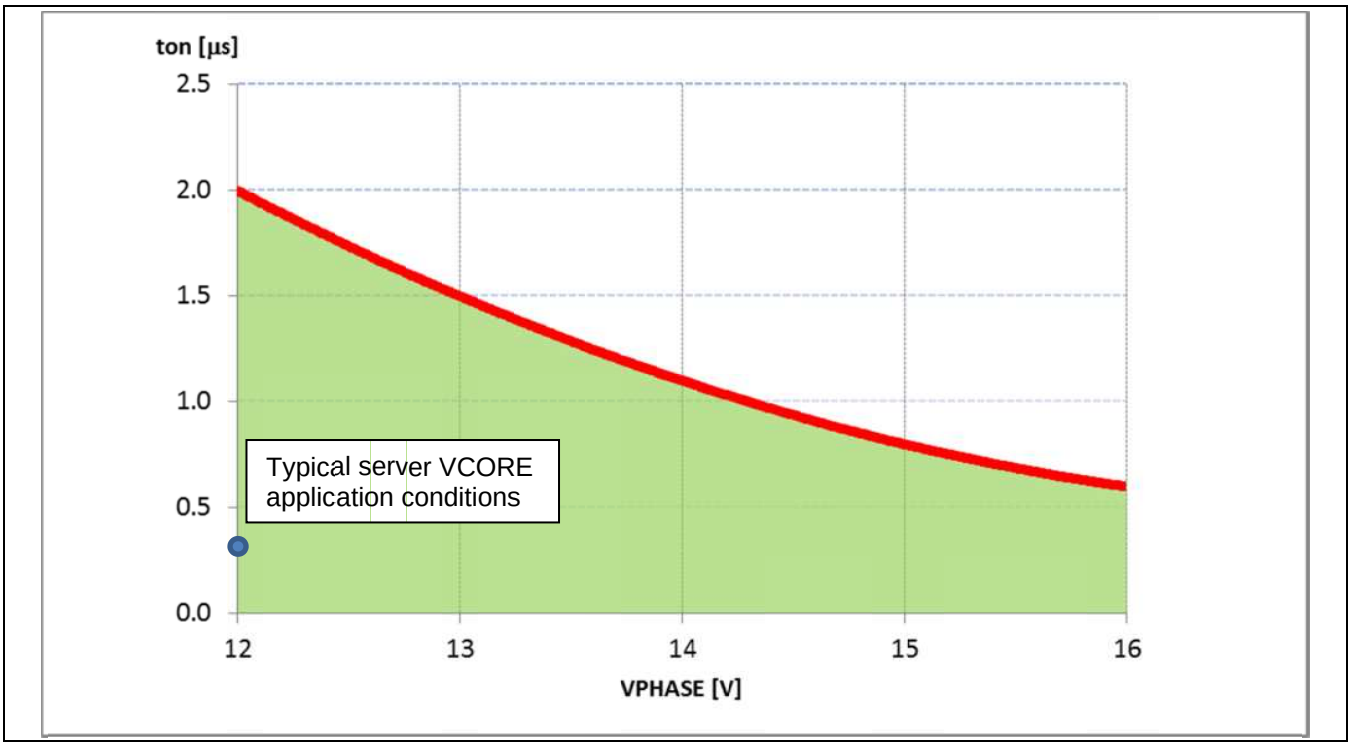


Figure 4 Safe Operating Area of R_{PHASE}

Note: t_{on} refers to the on-time of the HS-MOSFET. For input voltages below 12 V no limits on the duration of t_{on} need to be applied.The relative position of a typical Server VCORE application conditions V_{IN}=12V V_{OUT}=1.8V f_{SW}=450kHz is represented as reference.This Safe Operating Area is verified by design, not 100% tested in production.

Note: All rated voltages are relative to voltages on the GND pins unless otherwise specified.

4.2 Thermal characteristics

Table 6 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-soldering point[3]	θ_{JS}	-	7	-	K/W	-
Thermal resistance, junction-top of package	θ_{Jtop}	-	20	-		-

4.3 Recommended Operating Conditions and Electrical characteristics

Note: VCC = 5V, Tambient = 25°C

Table 7 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Test conditions
		Min.	Typ.	Max.		
Supply voltage rising edge between 3.1V and 4.5V : dv_{CC}/dt>5V/100ms	V_{VCC}	4.5	-	8	V	–
Frequency of the PWM	f_{SW}	-	-	1.2	MHz	Note[4]
Enable pin voltage	V_{EN}	0	-	3.3	V	
Junction temperature	T_{jOP}	-40	-	+125	°C	–
Minimum on time			20		ns	Note[4]
Minimum off time			30		ns	Note[4]

Table 8 Voltage Supply And Biasing Current

Parameter	Symbol	Values			Unit	Test conditions
		Min.	Typ.	Max.		
UVLO rising rising edge between 3.1V and 4.5V : dv_{CC}/dt>5V/100ms	V_{UVLO_R}	-	3.6	4.3	V	VCC rising
UVLO falling	V_{UVLO_F}	-	3.2	-		VCC falling
IC current	I_{VCC_300kHz}	-	2	-	mA	f_{SW} = 300kHz
	I_{VCC_PWML}	-	1.67	-		PWM = 0V
	$I_{VCC\_ENL\_PWML}$	-	1100	-	µA	EN = 0V PWM=0V
	I_{VCC_O}	-	780	-		PWM = Open

[3] The junction-soldering point is referred to the GND bottom exposed pad.

Table 9 Logic Inputs And Threshold

Parameter		Symbol	Values			Unit	Test conditions
			Min.	Typ.	Max.		
EN	Input low	V_{EN_L}			0.8	V	
	Input high	V_{EN_H}	2.0				
PWM	Input low	V_{PWM_L}	–	–	0.8	V	V_{PWM} falling
	Input high	V_{PWM_H}	2.5	–	–		V_{PWM} rising
	Input resistance	R_{IN-PWM}	-	2.06	-	kΩ	V_{PWM} = 1 V
	Open voltage	V_{PWM_O}	–	1.6	–	V	V_{PWM_O}
	Tristate shutdown window	V_{PWM_S}	1.2	–	2.0		–

Table 10 Timing Characteristics

Parameter	Symbol	Values			Unit	Test conditions
		Min.	Typ.	Max.		
Upper Gate (UGATE) Output						
Shutdown hold off time	t_{SSHD_U}		50		ns	Note, no load
UGATE rise time	t_{r_U}		10			Note[4], 3nF load
UGATE fall time	t_{f_U}		10			Note[4], 3nF load
tri-state to high propagation delay	t_{PDTS_U}		15			Note, no load
UGATE turn-on propagation delay	t_{PDH_U}		15			Note, no load
UGATE turn-off propagation delay	t_{PDL_U}		20			Note, no load
Lower Gate (LGATE) Output						
Shutdown hold-off time	t_{SSHD_L}		50		ns	Note, no load
LGATE rise time	t_{r_L}		10			Note[4], 3nF load
LGATE fall time	t_{f_L}		5			Note[4], 3nF load
tri-state to low propagation delay time	t_{PDTS_L}		15			Note, no load
LGATE turn-on propagation delay time	t_{PDH_L}		15			Note, no load
LGATE turn-off propagation delay time	t_{PDL_L}		7			Note, no load
Enable (EN)						
Propagation delay Time rising falling	t_{PDEN}		15		ns	

[4] Parameter verified by design, not 100% tested in production

Table 11 Output Characteristics

Parameter	Symbol	Values			Unit	Test conditions
		Min.	Typ.	Max.		
Output Characteristics						
Upper drive source current	I_{SRC_UG}		2		A	Note[2] current pulse < 20ns
Upper drive source impedance	R_{SRC_UG}		0.8		Ω	I_{SRC_UG} = 200mA
Upper drive sink current	I_{SNK_UG}		2		A	Note[2], current pulse < 20ns
Upper drive sink impedance	R_{SNK_UG}		0.6		Ω	I_{SINK_UG} = 200mA
Lower drive source current	I_{SRC_LG}		2		A	Note[2], current pulse < 40ns
Lower drive source impedance	R_{SRC_LG}		0.8		Ω	I_{SRC_UG} = 200mA
Lower drive sink current	I_{SNK_LG}		4		A	Note[2], current pulse < 40ns
Lower drive sink impedance	R_{SNK_LG}		0.35		Ω	I_{SINK_UG} = 200mA

5 Theory of operation

The PX3519 functionality is enabled by the EN pin. When the EN pin voltage overcomes the rising voltage threshold of the UVLO the driver begins to operate depending on the PWM status and the VCC pin status (VCC has to be higher then the rising threshold voltage). For VCC is recommended to have a slope for the rising edge higher than 5V/100ms around the rising UVLO threshold.

The VCC can range between 4.5V and 8V and it is the supply pin for both driver and logic sections.

The PX3519 functionality is driven by the PWM signal transitions. When the PWM signal performs a transition between low state to high state (PWM voltage higher than 2.5V) the Low Side MOSFET is turned off, after the turn off delay propagation time. Then the High Side MOSFET is turned on, after the turn on propagation delay time. Once the on time is expired the PWM signal provides a transition between the high state to the low state (PWM voltage lower than 0.8V). This will drive the High Side MOSFET from the ON state to the OFF state, after the turn off propagation delay time. The PX3519 is also capable to drive the two external MOSFETs both in off state. When the PWM signal enters in the shut down window or tri-state (typically between 1.2V and 2.0V) after the shut down hold off time both MOSFETs are switched off. This feature is useful when the IC controller wants to reduce the number of active phases in order to reduce the power consumption. In principle the tri-state status can be used also to improve the transition between high loads to low load.

The PX3519 implements an embedded resistor network, which forces the PWM pin of the device in the middle of the shut down window if the PWM input from the controller is floating.

In order to avoid cross conduction between the High Side MOSFET and the Low Side MOSFET an anti-shoot-through control is implemented with the adaptive scheme. The adaptive scheme is implemented in order to use a variety of different power MOSFETs for different kind of conversion. Nevertheless the dead time is kept as short as possible in order to increase the efficiency of the overall solution.

The driver includes gate drive functionality to protect against shoot through. In order to protect the power stage from overlap, both High Side and Low Side MOSFETs being on at the same time, the adaptive control circuitry monitors the voltage at the “PHASE” pin. When the PWM signal goes low, the High Side MOSFET will begin to turn off. Once the “PHASE” pin falls below 1V, the Low Side MOSFET is gated on. Additionally, the gate to source voltage of the High Side MOSFET is also monitored. When VGS (High Side) is discharged below 1V, a threshold known to turn the High Side MOSFET off, a secondary delay is initiated, which results in the Low Side being gated “ON” regardless of the state of the “PHASE” pin. This way it will be ensured that the converter can sink current efficiently and the bootstrap capacitor will be refreshed appropriately during each switching cycle.

During the start up depending on several factors it can be that the power input for the conversion (input rail) rises before the VCC input. In this case it could happen that the high side has an induced turn on. In order to avoid this undesirable effect the PX3519 embeds a resistance of 10 kOhm between UGATE pin and PHASE pin.

In order to reduce the sensitivity to issues generated during the power on sequence (like the induced turn on of the high side MOSFET) and to reduce further the power consumption an EN pin is implemented; in this case the designer has the possibility to create a short delay time between the VCC and the EN pin voltage to ensure the proper functionality. Moreover the EN pin can be used to disable the driver stage in case a very low consumption is required.

5.1 Driver characteristics

The gate driver of the PX3519 has one supply voltage to simplify the layout of the system.The VCC pin is used to power the section related to the logic for detecting the status of PWM pin and EN pin. The VCC pin is used also to supply the power section related to the driver of the power mosfet.

The MOSFETs selected for this application are optimized for 5V gate drive, thus giving the end user optimized high load as well as light load efficiency. Nevertheless the driving voltage can be increased up to 8V in order to have a customized efficiency curve depending on the application conditions. The reference for the power circuitry including the driver output stage and the reference for the gate driver control circuit is GND.

Proper response of the driver to the PWM signal is only guaranteed when UVLO have been cleared by the respective supply voltages (ref to table 8). Therefore, it is strongly recommended to only issue pulses to PWM when no UVLO conditions are present. The power down sequence should set PWM to HiZ with respect the internal threshold, before ramping down VIN (see figure 6 for VIN connection), PVCC and VCC respectively.

5.2 Current capability and internal Bootstrap

The PX3519 implements high current capability and low ohmic pull down resistances for the driving stages. The high current capability ensures fast switching transition for the MOSFETs in order to reduce the switching losses (2A of driving source/sink current for the upper MOSFET) even with high gate charge high side. The low ohmic pull down resistance (Low driver sink impedance 0.35 Ohm) is mainly important to avoid the induced turn on phenomenon on the low side during the fast turn on of the high side MOSFET.

The high side is powered through the bootstrap circuitry. The PX3519 provides an embedded bootstrap diode. To complete the power network only a capacitance between PHASE and BOOT is needed. In many cases the PX3519 is optimized for the best switching behavior. An external resistance is not needed. The bootstrap capacitance is chosen depending on the high side gate charge. The following formula is giving a good estimation of the voltage drop across the bootstrap capacitance due to the charging of the high side:

$$C_{BOOT} > {Q_{GS\_HS}}/{\Delta V_{BOOT}}$$

Where the ΔVBOOT is the desired variation of the bootstrap voltage.

The low side driver is powered through the VCC pin. The same considerations and formula done for the bootstrap capacitance can be done for the capacitance used to filter the VCC pin.

The flexibility to adjust the driving voltage from 4.5V to 8V gives designers the possibility to shape the efficiency curve in anyway that is desired.

5.3 Power dissipation

The power dissipation of the driver is given by the gate charge of the external power MOSFETs. The following formulas held:

$$P_{DISS} = VCC * f_{SW} * (Q_{GS\_HS} + Q_{GS\_LS})$$

Where FSW is the switching frequency and QGHS and QGLS are respectively the gate charge of the high side and the gate charge of the low side at the VCC driving voltage. The very low thermal resistance package used for the PX3519 allows the device to avoid any usage of external resistances to decrease the power dissipation inside the driver even with high driving voltage. Since the thermal resistance is strongly influenced by the numbers of layers used in the board, it is recommended to check roughly the expected junction temperature via the power calculation.

5.4 Inputs to the internal control circuits

The **PWM** is the control input to the IC from an external PWM controller and is compatible with 3.3V.

The PWM input has tri-state functionality. When the voltage remains in the specified PWM-shutdown-window for at least the PWM-shutdown-holdoff time T_tsshd, the operation will be suspended by keeping both MOSFET gate outputs low. Once left open, the pin is internally fixed to V_{PWM_O} = 1.6 V level.

Table 12 PWM Pin Functionality

PWM logic level	Driver output
Low	LGATE= High, UGATE = Low
High	LGATE = Low, UGATE = High
Open (left floating, or High impedance)	LGATE = Low, UGATE = Low

During power-up sequence, the initial state of the PWM signal is ignored, until the first rising edge.

Since all the thresholds are derived from an internal linear regulator they will not depend on the VCC input.

5.5 Enable pin

The EN pin has the main function to control the driver stage itself and enables operation. Once the voltage across the EN pin is higher than the rising edge threshold of the EN pin and the voltage across the VCC pin is above the rising edge threshold of the UVLO, the driver stage turns on and off the MOSFET based on the PWM status. The EN pin can not be left floating.

The enable can be used for three different purposes:

1. Power sequence: It can be delayed in order to turn on the power stage once VCC is at the expected level. This will reduce the probability of improper turn on sequences or oscillation created by unstable conditions.
2. Power saving: there are two ways of disabling the driver stage: the first one is through the PWM signal; once the PWM signal is in the tri-state window the gate activity is stopped. The second one is the EN pin; once the enable pin is pulled below the falling edge threshold the driver stage is completely switched off. The difference between the two methods is basically that the PWM still leaves alive all the comparators and the auxiliary voltages, so that the consumption of the power stage is not at the minimum level.
3. Zero Cross: if the controller is capable to detect the crossing of the inductor current, the EN pin could be used to switch off the low side MOSFET faster than the PWM (due to the hold off time)´in order to avoid the current reverse.

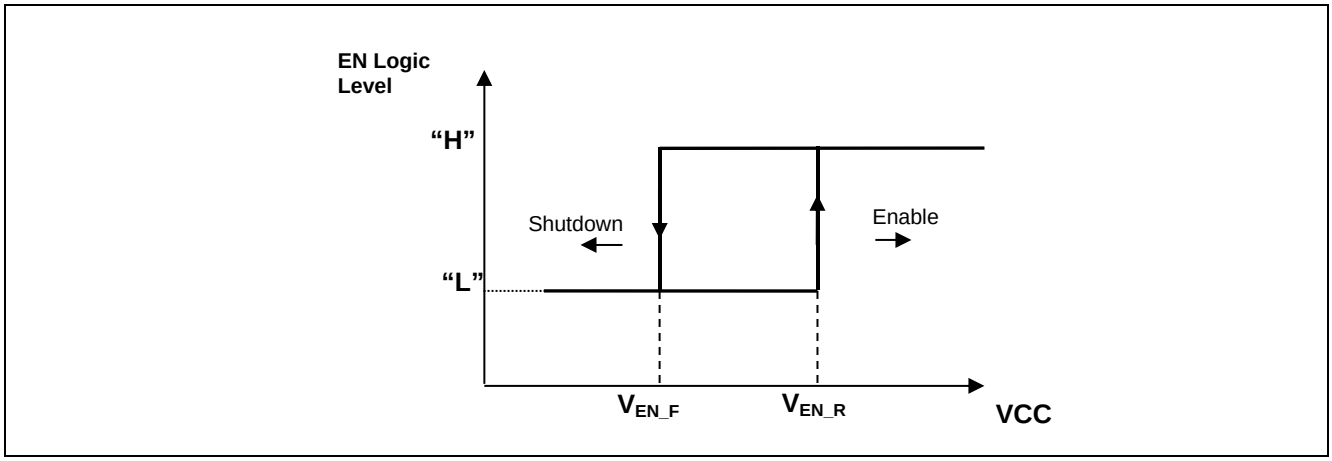


Figure 5 Enable pin

5.6 Layout consideration

The PX3519 has a good protection system against unwanted overshoot and undershoot; the PHASE pin can range between dynamically -12V to 25V.

The parasitic inductances of the PCB and of the power devices’ packaging (both upper and lower MOSFETs) can cause serious ringing, exceeding absolute maximum rating of the devices. Careful layout can help minimize such unwanted stress. The following advice is meant to lead to an optimized layout:

Keep decoupling loops (VCC-GND and BOOT-PHASE) as short as possible and use high quality ceramic capacitance with low ESR (10mOhm) and low ESL (lower than 1nH).

Minimize trace inductance, especially on low-impedance lines. All power traces (UGATE, PHASE, LGATE, GND, VCC) should be short and wide, as much as possible.

Minimize the area of the PHASE node. Ideally, the source of the upper and the drain of the lower MOSFET should be as close as close as possible.Minimize the current loop of the output and input power trains. Short the source connection of the lower MOSFET to ground as close to the transistor pin as feasible. Input capacitors (especially ceramic decoupling) should be placed as close to the drain of upper and source of lower MOSFETs as possible.

To optimize heat spreading, copper should be placed directly underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried copper plane(s) with thermal vias. This combination of vias for vertical heat escape, extended copper plane, and buried planes for heat spreading allows the IC to achieve its full thermal potential.

6 Application

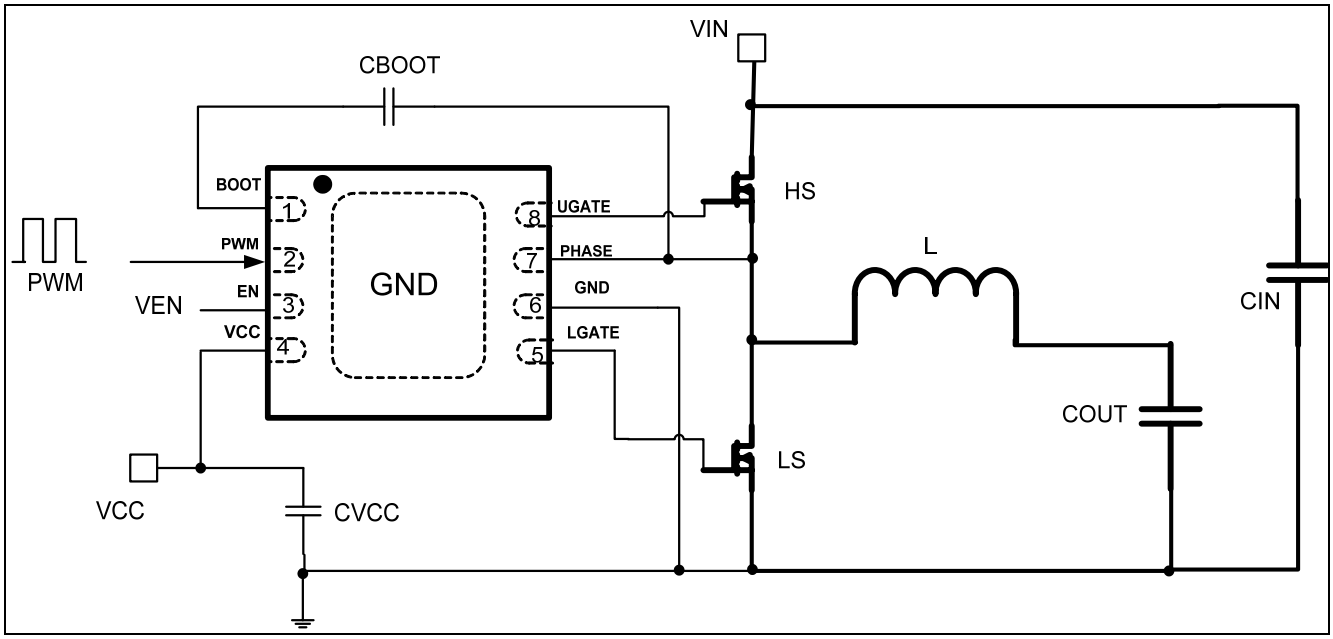


Figure 6 Pin interconnection outline (transparent top view)

7 Gate driver timing diagram

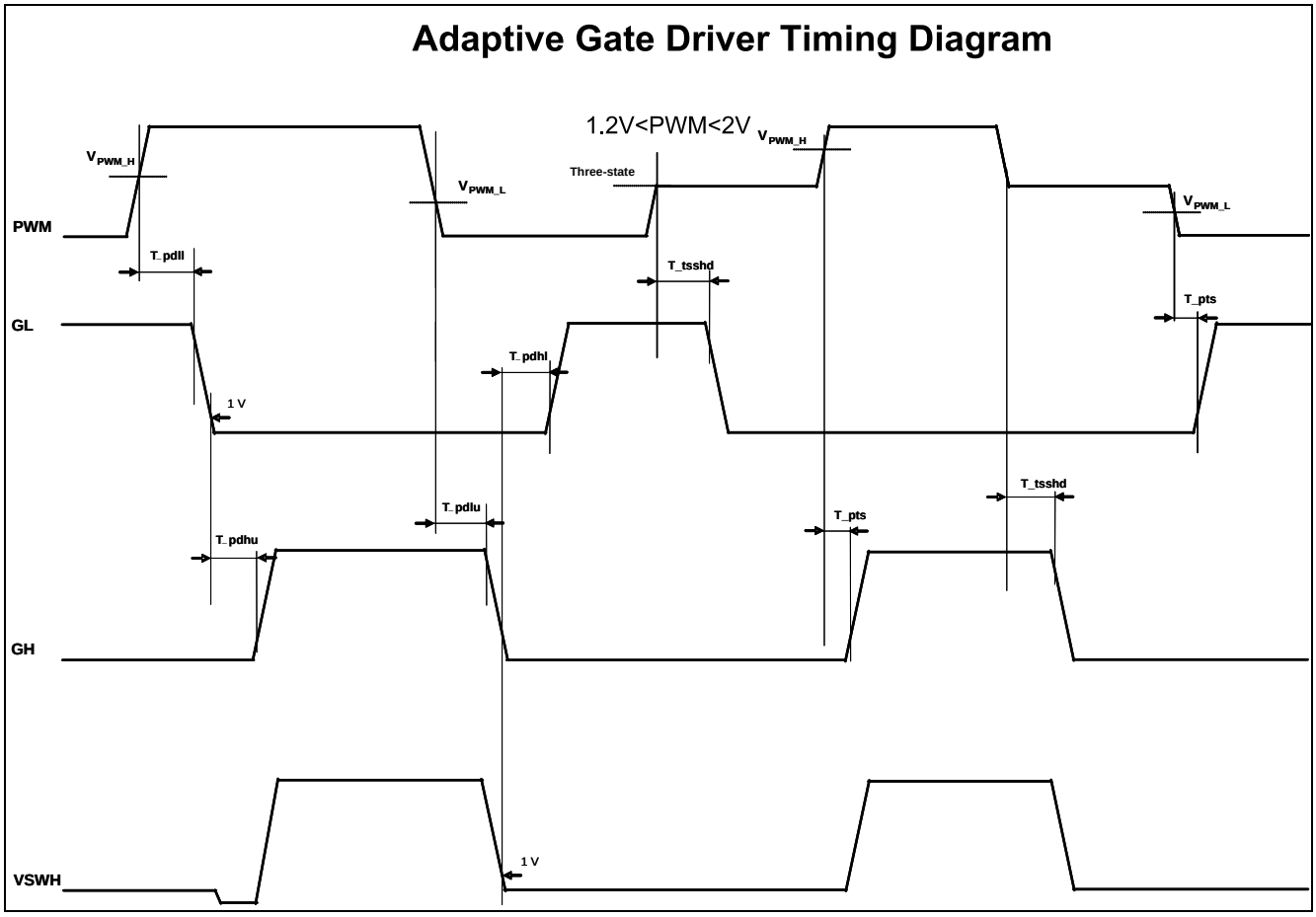


Figure 7 Adaptive gate driver timing diagram

8 Enable timing diagram

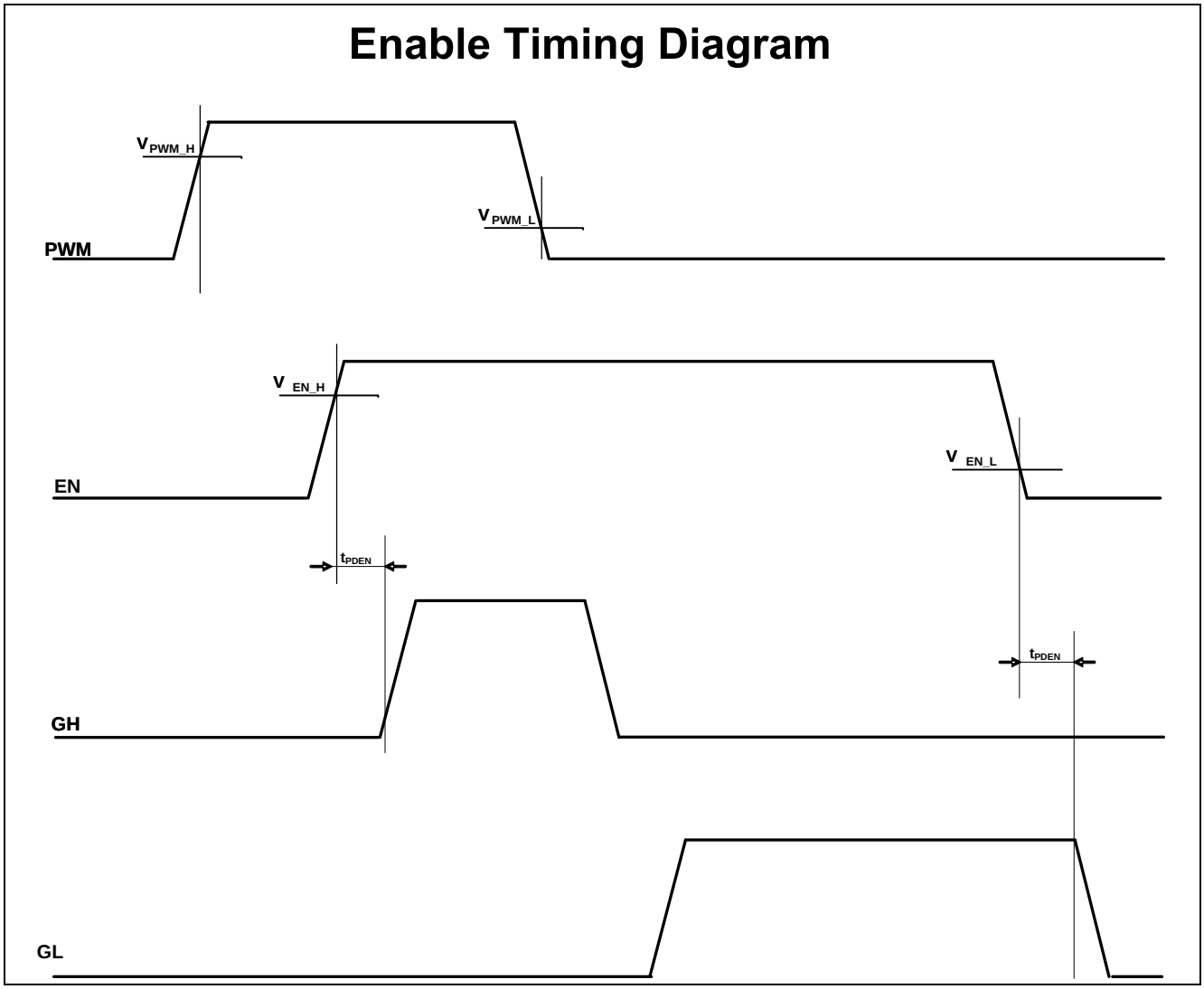
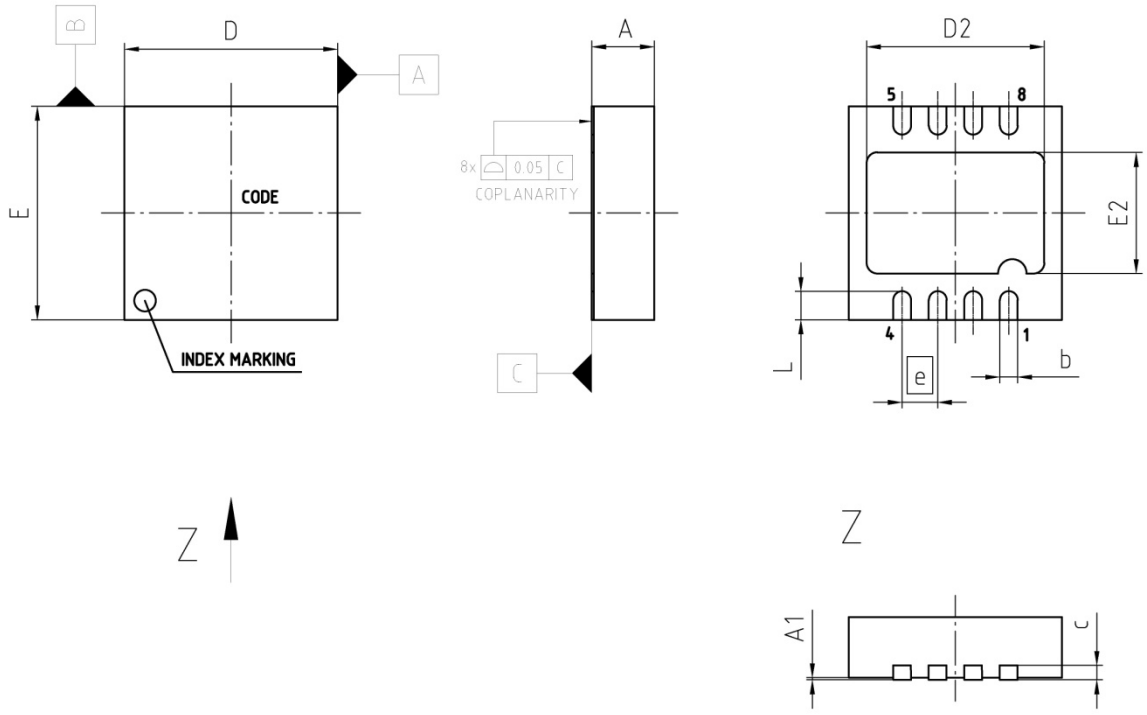


Figure 8 Enable Vs PWM timing diagram

9 Mechanical drawing



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	0.90	0.031	0.035
A1	0.00	0.05	0.000	0.002
b	0.20	0.30	0.008	0.012
c	0.20		0.008	
D	2.90	3.10	0.114	0.122
D2	2.40	2.60	0.094	0.102
E	2.90	3.10	0.114	0.122
E2	1.60	1.80	0.063	0.071
e	0.50 (BSC)		0.020 (BSC)	
N	8		8	
L	0.35	0.45	0.014	0.018

DOCUMENT NO.
Z8B000169261

SCALE
0
1
0 1
2mm

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Figure 9 Mechanical dimensions

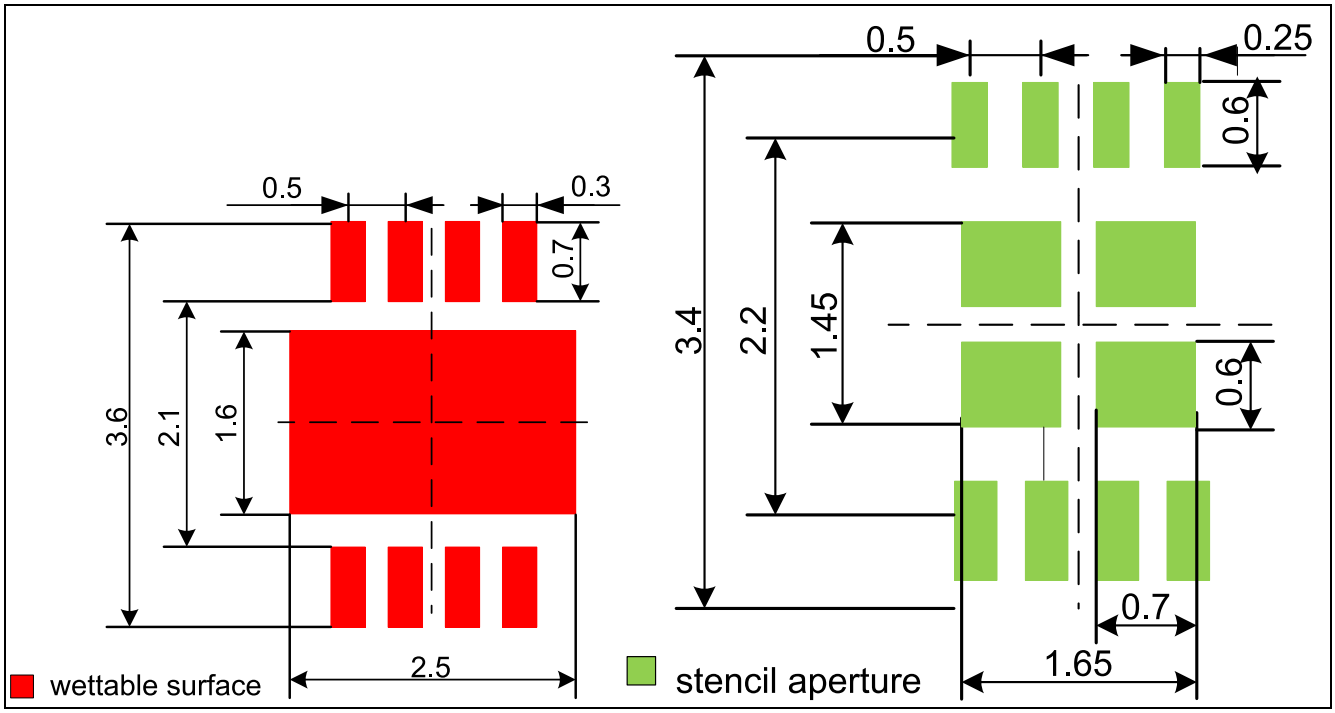

Figure 10 Footprint and solder stencil recommendations

w w w . i n f i n e o n . c o m

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