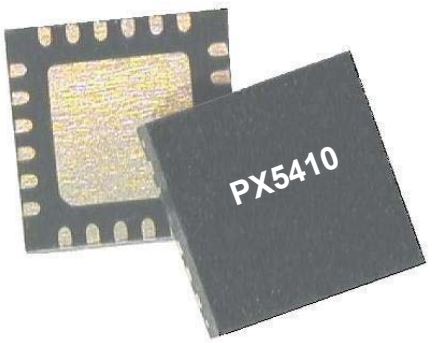
PX5410
Multi-Rate VCSEL Driver
Product Brief

January 2004



Features

- Up to 4.25 Gb/s serial VCSEL driver
- Single +3.3 V supply
- Average power control (APC) provides constant output optical power
- Digital diagnostics provided with bias, photodiode, and temperature monitors
- Independent temperature compensation for VCSEL bias and modulation current
- VCSEL fault protection limits output optical power for laser safety
- Differential CML compatible inputs with on-chip termination
- 4 mm x 4 mm QFN package

Applications

- SFP, SFF form factors
- 4GFC, 2GFC, 1GFC, OC-48, Gigabit Ethernet
- Proprietary intra-system optics

Description

The growing use of the Internet and the increasing demand for storage area network (SAN) solutions has created the need for next generation physical layer ICs. In addition the introduction of 4 G Fiber Channel (4GFC) has introduced the need for next generation ICs to be backwards compatible with 1 G and 2 G Fiber Channel. The Zarlink PX5410 provides a multi-rate VCSEL driver solution for 1, 2, and 4GFC.

The Zarlink PX5410 Multi-Rate VCSEL Driver is designed for various applications up to 4.25 Gb/s. It consists of a DC-coupled amplifier with adjustable modulation and bias currents optimized for driving commercially available VCSEL-based transmit optical sub assemblies (TOSAs) from a single +3.3 V supply.

VCSEL modulation and bias currents can be programmed by a variety of means including external resistors, programmable potentiometers, SFF-8472 controllers, or microcontroller DAC outputs. Selectable temperature compensation and closed-loop average power control deliver optimized optical output power and extinction ratio over temperature.

Figure 1: Filtered 4.25 Gb/s optical output with a PRBS7 data pattern

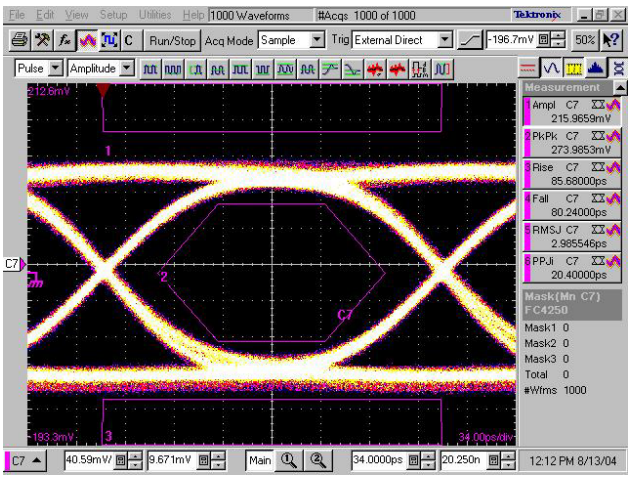


Figure 2: Typical APC closed-loop configuration using TOSA monitor photo diode to provide constant VCSEL output power. Modulation current temperature compensation also enabled to improve extinction ratio across operating temperatures.

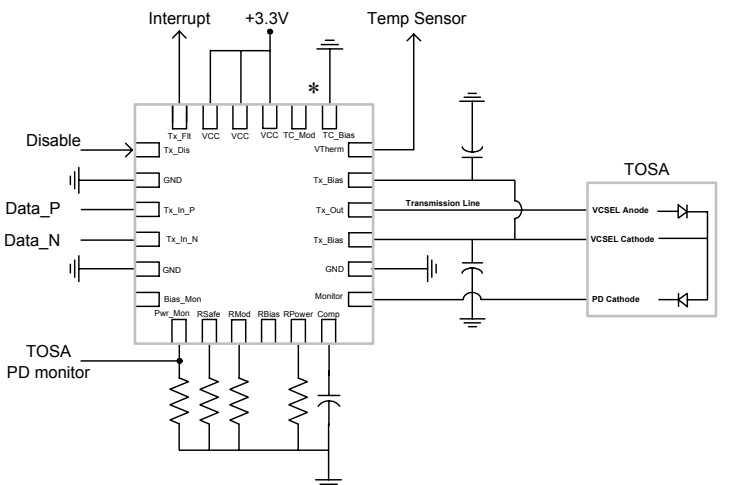
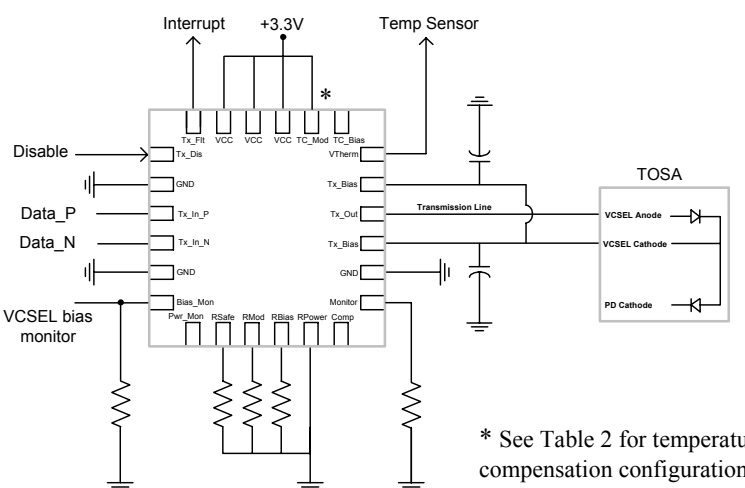


Figure 3: Typical open-loop configuration with internal temperature compensation enabled for bias and modulation currents.



* See Table 2 for temperature compensation configurations

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE