PX6419

12x10 Gb/s VCSEL Driver

Product Brief

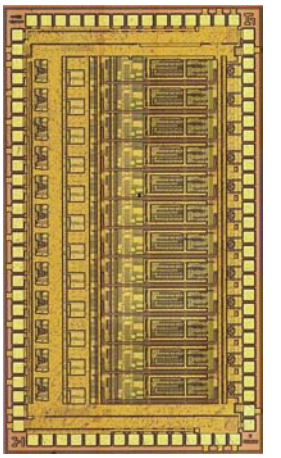
January 2005

Features

- 12x10 Gb/s VCSEL Driver
- Single +3.3V supply dissipating 142 mW per channel
- Serial digital interface for global and individual channel control
- Individual channel control for enable, modulation and bias current
- On-chip adjustable VCSEL temperature compensation
- Adjustable output current waveform for VCSEL jitter reduction
- Analog control input for closed-loop optical power optimization
- VCSEL open/short detection with autonomous fault handling
- 250-micron channel pitch matches optical ribbon fiber and array VCSELs
- Differential CML inputs with on-chip termination

Applications

- Proprietary 120 Gb/s intra-system parallel optics
- Proprietary 12-lane optical modules and CWDM
- 10GbE, 10GFC, OC-192 VSR parallel optics



Description

The growing use of the Internet has created increasingly higher demand for multi-Gb/s I/O performance. The demand for 1 Tb/s+ WAN bandwidth fuels the growth of short-reach 120 Gb/s infrastructures within high-end telco and datacom routers, switches, servers and other proprietary chassis-to-chassis links.

The Zarlink PX6419 12X10 Gb/s VCSEL Driver* is a 12-channel VCSEL driver designed for various 12x10 Gb/s, 120 Gb/s parallel optics and CWDM PMD applications. It consists of a DC-coupled amplifier with selectable modulation and bias currents optimized for driving commercially available, common cathode VCSELs from a single +3.3 V supply.

Individual channel settings are used to control the modulation and bias current and their temperature coefficients, allowing the optical output power and extinction ratio to be optimized. Data controlling the Zarlink PX6419 VCSEL Driver settings is loaded by a simple four-wire CMOS serial interface that features read/write and daisy chain capabilities.

Figure 1: Zarlink PX6419 IC driving a commercially-available VCSEL at 10 Gb/s with a PRBS 2^{31}-1 pattern

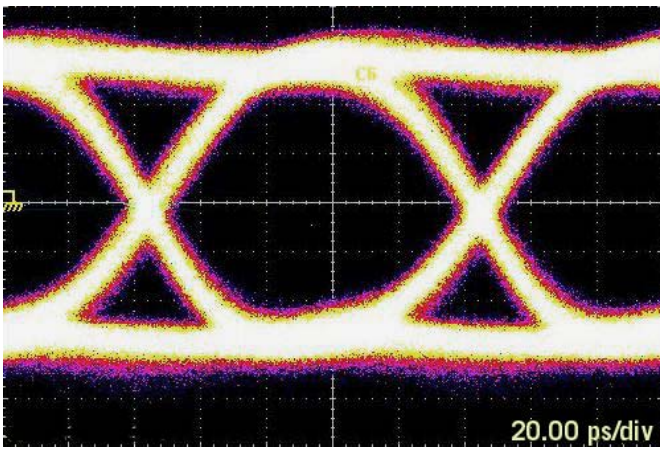
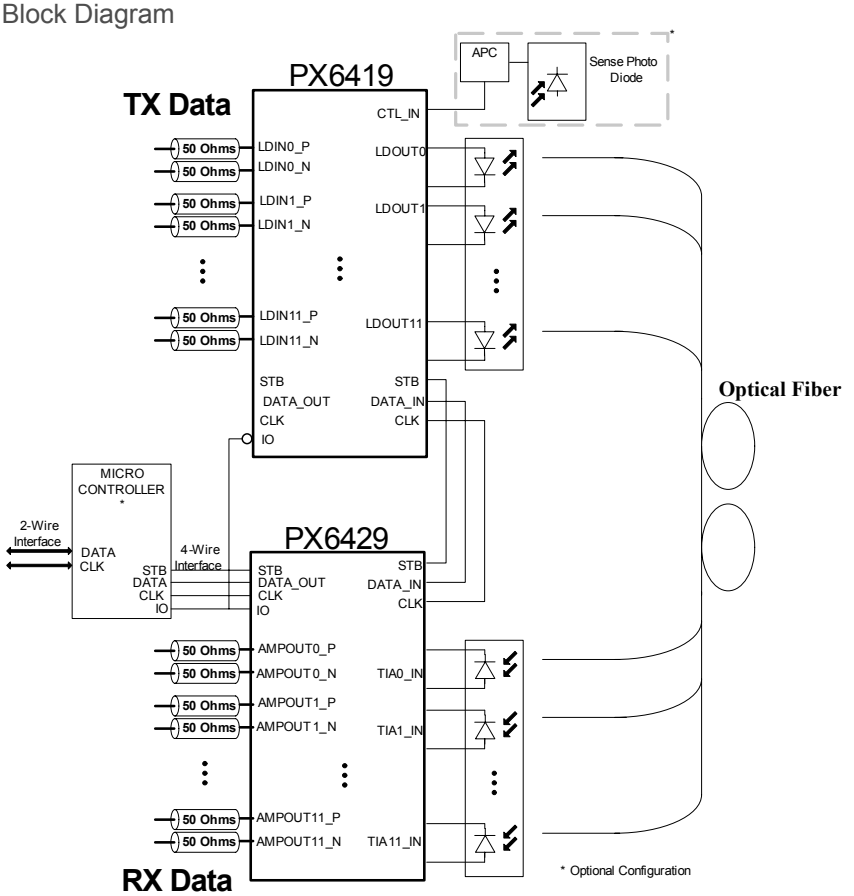


Figure 2: Application Block Diagram



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