PX6429

12 x 10 Gb/s TIA/LA Optical Receiver

Product Brief

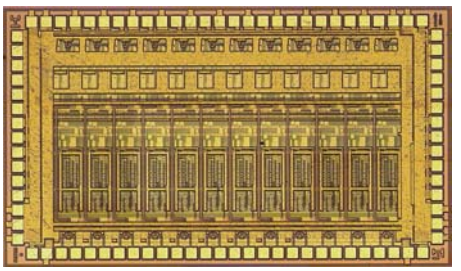
April 2005

Features

- 12x10 Gb/s Integrated Transimpedance and Limiting Amplifier for parallel channel optical receiver applications
- Channels support data rates up to 10.7 Gb/s enabling various 120 Gb/s parallel PMD applications
- Global signal detect senses quiescent photocurrent with adjustable threshold and hysteresis
- Individual channel signal detect senses input signal strength (0MA) with adjustable sensitivity and hysteresis
- 20 uA_{pp} receiver sensitivity for 10^{-12} BER
- 180 mW per channel power dissipation for >500 mV differential output swing
- Serial digital interface for controlling channel power down, signal detect sensitivity, output amplitude and global signal detect
- Differential back-terminated outputs
- Flip-chip or direct wire-bond attach to photodiode
- 250-micron channel pitch matches optical ribbon fiber and array photodiodes

Applications

- Proprietary 120Gb/s intra-system parallel optics
- Multi-channel 10GbE, 10GFC, OC-192 VSR optical links



Description

The growing use of the Internet has created increasingly higher demand for multi-Gb/s I/O performance. The demand for 100+ Gb/s WAN bandwidth fuels the growth of short-reach 120 Gb/s infrastructures within high-end telco and datacom routers, switches, servers and other proprietary chassis-to-chassis links. The Zarlink PX6429 120 GB/s TIA/LA Receiver is a 12-channel TIA/LA optical receiver designed for various 12x10 Gb/s, 10 Gb/s parallel optics and CWDM PMD applications. It consists of a DC coupled transimpedance amplifier and an AC coupled differential limiting amplifier.

The transimpedance amplifier achieves a nominal 8 GHz bandwidth over a wide range of photodiode input capacitance. Excellent channel-to-channel isolation ensures data integrity at the receiver sensitivity limits. A global signal detect circuit provides the photodiode reverse bias voltage supply and senses average photocurrent supplied to the photodiode array.

The transimpedance amplifier is AC-coupled internally to a high-gain, high-bandwidth differential limiting amplifier. The limiting amplifier provides a differential back-terminated CML output that can be used to drive 10 Gb/s per channel transceivers or other CML compatible clock and data recovery circuits. The limiting amplifier features an adjustable signal detect circuit that senses optical modulation amplitude (OMA) to provide a received signal indication for each channel.

Figure 1: Typical optical to electrical differential data eye from the Zarlink PX6429 IC using a commercially available photodiode at 10 Gb/s with a PRBS31 data pattern.

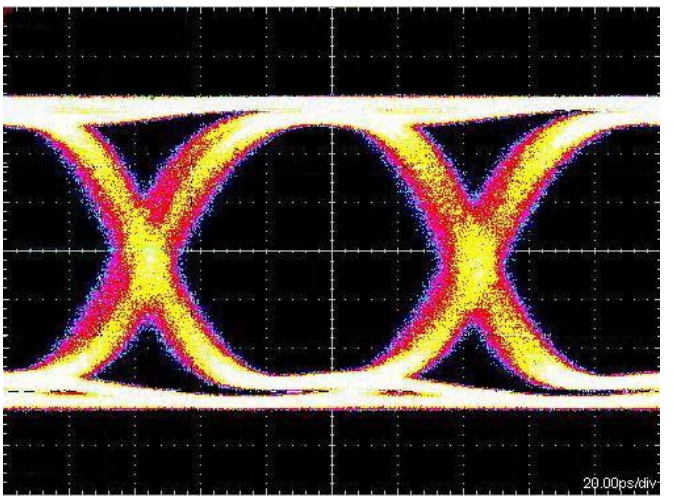
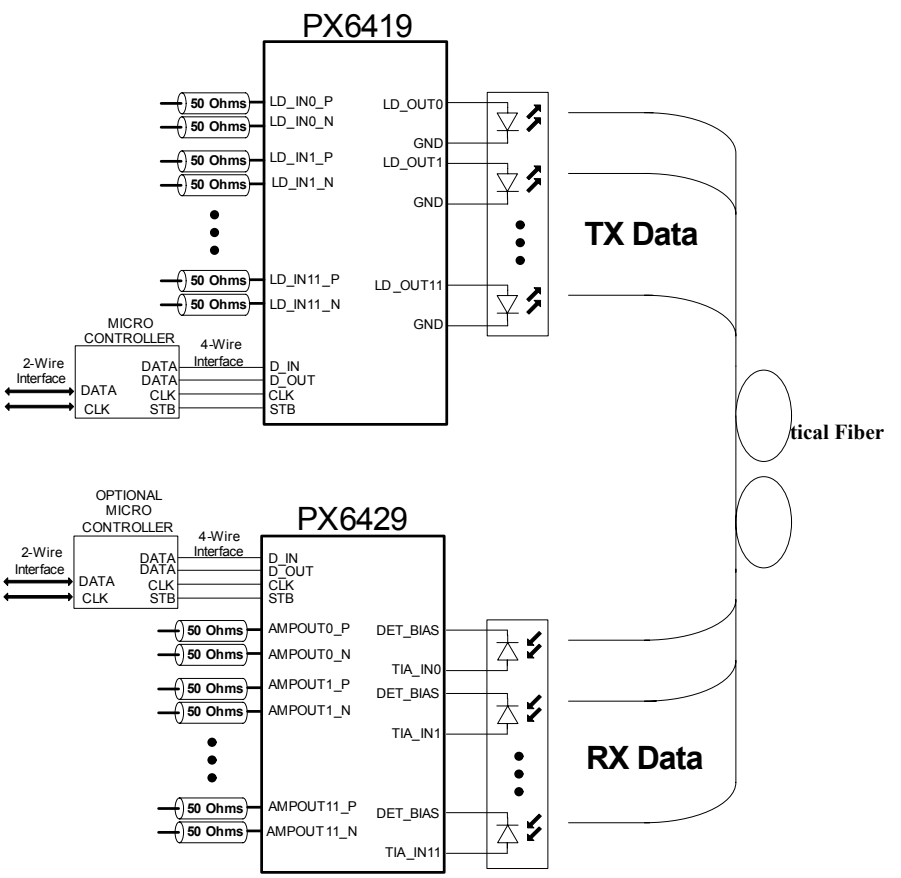


Figure 2: Application Block Diagram



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