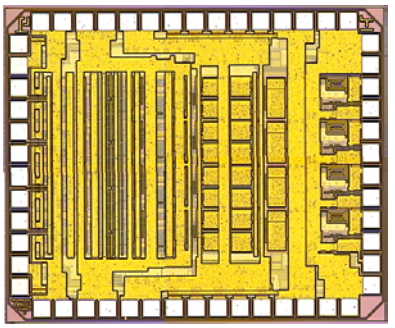
PX6524

4 x 10 Gb/s TIA/LA Receiver

Product Brief

April 2006



Features

- 4-channel integrated transimpedance and liming amplifier operates up to 10.7 Gb/s
- 20 uA_{PP} receiver sensitivity for 10^{-12} BER
- Single +3.3V supply dissipating 160 mW per channel
- Individual channel signal detect compares input signal strength (OMA) with adjustable threshold
- Global signal detect compares quiescent photocurrent with adjustable threshold
- Squelch automatically disables output when input signal strength falls below programmable threshold
- Serial digital interface for controlling channel enable and signal detect features
- Reconfigurable I/O provides access to serial digital interface and dedicated channel signal detect outputs
- 250-micron channel pitch matches optical ribbon fiber and photodiode arrays

Applications

- 4-lane 10GbE, 10GFC, 8GFC, and OC-192 VSR parallel optical modules
- Proprietary OC-768 parallel optics and CWDM
- Proprietary 4-lane intra-system parallel optics

Description

The growing use of the Internet has created increasingly higher demand for multi-Gb/s I/O performance. The demand for 100+ Gb/s WAN bandwidth fuels the growth of short-reach 40 Gb/s infrastructures within high-end telco and datacom routers, switches, servers and other proprietary chassis-to-chassis links. The Zarlink PX6524 10 Gb/s TIA/LA Receiver is a four-channel TIA/LA optical receiver designed for various 4x10 Gb/s parallel optics and CWDM PMD applications. It consists of a DC-coupled transimpedance amplifier and an AC-coupled differential limiting amplifier.

The transimpedance amplifier achieves a nominal 8 GHz bandwidth over a wide range of photodiode input capacitance. Excellent channel-to-channel isolation ensures data integrity at the receiver sensitivity limits. A global signal detect circuit provides the photodiode reverse bias voltage supply and senses average photocurrent supplied to the photodiode array.

The transimpedance amplifier is AC-coupled internally to a high-gain, high-bandwidth differential limiting amplifier. The limiting amplifier provides a differential back-terminated CML output that can be used to drive 10 Gb/s per channel transceivers or other CML compatible clock and data recovery circuits. The limiting amplifier features an adjustable signal detect circuit that senses optical modulation amplitude (OMA) to provide a received signal indication for each channel.

Figure 1: Typical 10 Gb/s PRBS31 output data pattern with optical input

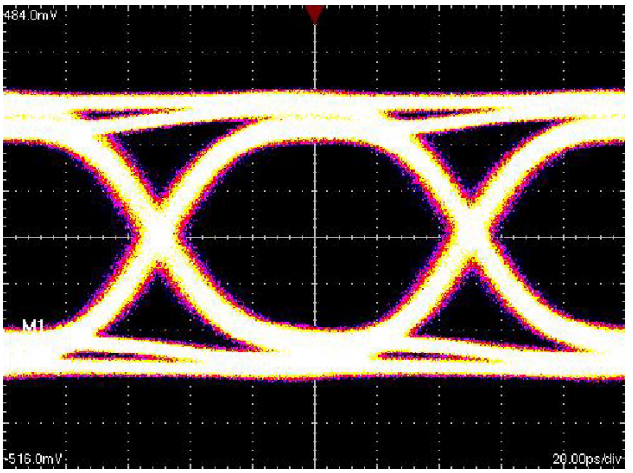
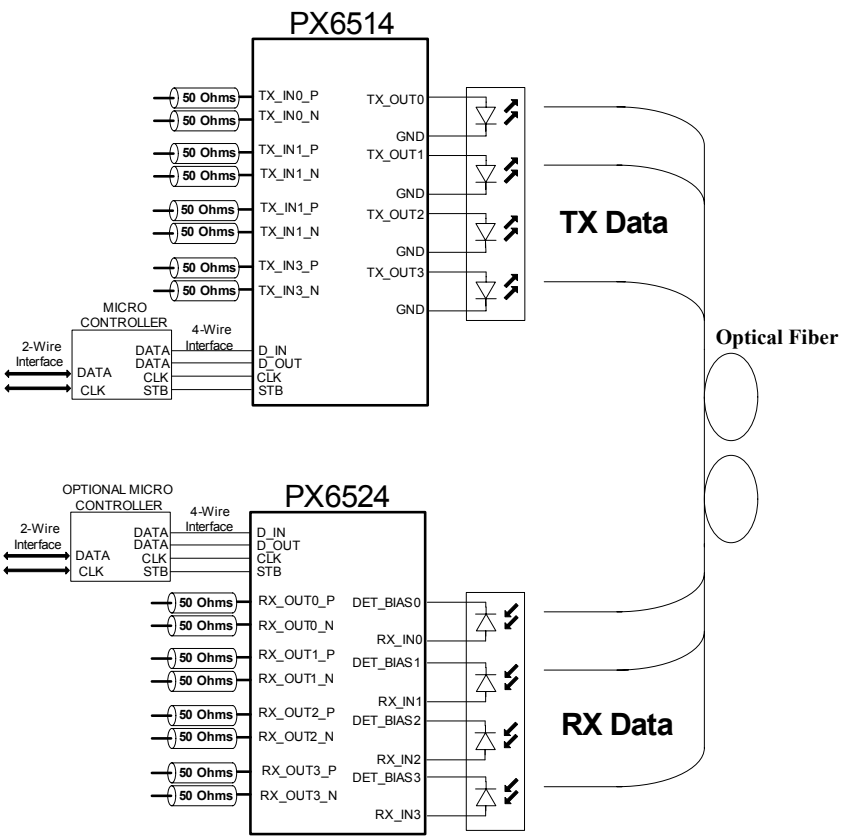


Figure 2: Application block diagram utilizing the PX6514 VCSEL driver and the PX6524 optical receiver



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