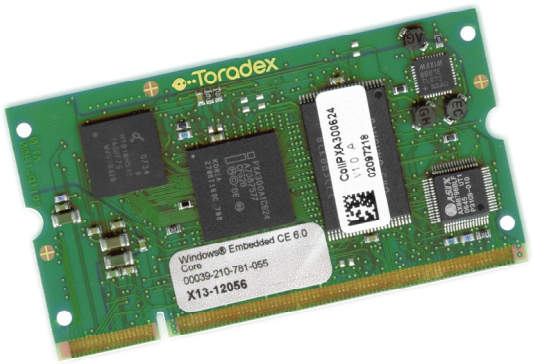
Colibri XScale® PXA300

Datasheet



Revision history

Date	Doc. Rev.	Colibri PXA300 Version	Changes
22-Oct-07	Rev. 1.0	V1.1	Initial Release
24-Dec-07	Rev. 1.1	V1.1	Changed some pin names (MD to DATA, MA to ADDRESS)

Contents

1. Introduction

1.1 Hardware

Colibri XScale® PXA300 is a SODIMM sized computer module based on the new Marvell XScale® PXA300 processor. It runs at up to 208 MHz and consumes as little as *tbd* mW (*about 600mW*). The module delivers state of the art technology, targeting low power systems that still require high CPU performance.

It also offers all the interfaces needed in a modern embedded device: beside the internal Flash memory, SDCard is also available. The module provides glueless connectivity to passive and active LCDs with resolutions of up to 1024x768. Colibri PXA300 can directly connect to a CMOS/CCD camera sensor.
In addition Colibri PXA300 offers a 100 MBit Ethernet as well as USB host and USB device functionality.

The 16 bit wide demultiplexed system bus (DFI) is available for custom extensions, such as special interfaces for high bandwidth applications.

1.2 Software

The module is shipped with a preinstalled WinCE image with WinCE Core license.
Other OS like Embedded Linux and QNX are available from third-party.

1.2.1 Windows CE

Colibri PXA300 modules are shipped with a valid Windows CE 6.0 core license.
Toradex provides a WinCE5.0 image and a WinCE6.0 (from end of 2007).
All WinCE images contain drivers for the most common interfaces and are easily customizable by registry settings to adapt to specific hardware.

1.3 Features

CPU:
Marvell PXA300 208 MHz

Memory:
64 MByte of DDR SDRAM (16 Bit)
128 MByte of NAND FLASH (8 Bit)

Interfaces:
16 Bit demultiplexed DFI bus
LCD (up to 1024x768)
CMOS/CCD image sensor interface
I2C
SPI
2x SDCard (SDIO, MMC)
Up to 120 GPIOs
USB host / device
USB 2.0 device (requires external UTMI chip)
100 MBit Ethernet
One-Wire
Keypad
Consumer Infrared
USIM

Supported operating systems:
WinCE 5.0
WinCE 6.0 (begin of 2008)

1.4 Reference Documents

For detailed technical information about the Colibri PXA300 components, please refer to the documents listed below.

1.4.1 Marvell PXA300 Processor Based on Intel XScale Technology

The datasheets and other technical documents about the PXA300 processor are available on the Marvell web page (NDA required).
http://www.marvell.com

1.4.2 AX88796B Ethernet Controller

http://www.asix.com.tw

2. Architecture Overview

2.1 Block Diagram

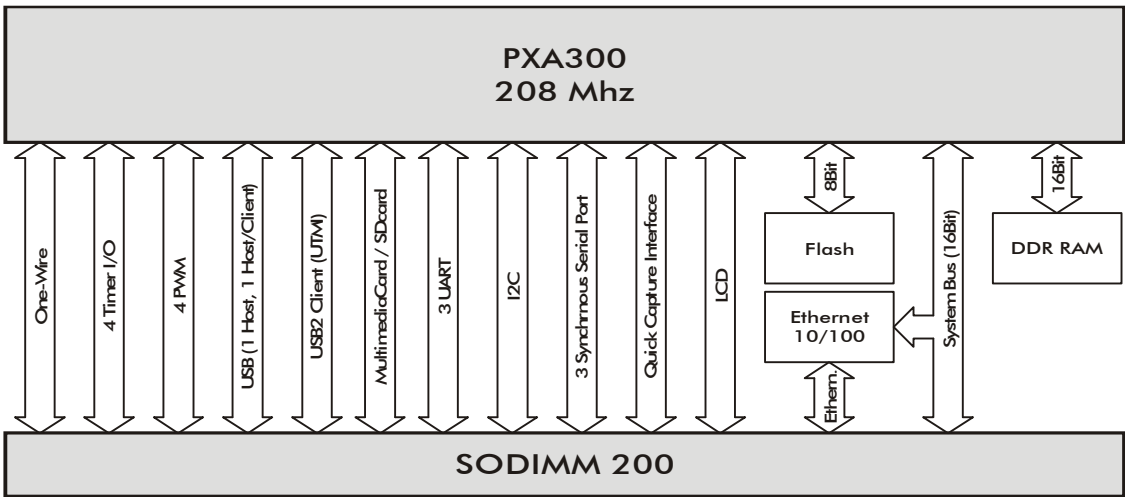


Figure 1: Colibri PXA300 block diagram

Figure 1 shows the Colibri PXA300 interfaces. However, some PXA300 pins are mapped to multiple interfaces. Therefore not all functions can be used simultaneously.

Colibri PXA300 features an 8 bit interface to on board NAND FLASH and a 16 bit interface to the Ethernet controller.

Wireless Intel (Marvell) Speedstep® Technology, which adjusts the CPU core voltage dynamically according to the CPU load, and four low-power modes both enable excellent MIPS/mW performance for the Colibri PXA300 module.

3. Colibri PXA300 Connectors

3.1 Physical Locations

Along with the main 200 Pin SODIMM connector the Colibri PXA300 is equipped with two additional FCC connectors. The position of the connectors is shown in the figure below.

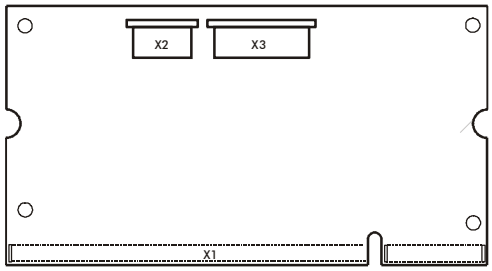


Figure 2: Location of Colibri PXA300's Connectors

3.2 Assignment

Some of the following pins are multiplexed, that means there is more than one PXA300 pin connected to one SODIMM or FFC pin. For example GPIO101 and GPIO115 are both assigned to SODIMM pin 25. Take care to tristate (set to input) the unused GPIO of the two multiplexed GPIO's when you are writing your software.

3.2.1 SODIMM 200 (X1)

Pin#	Top side (Toradex logo)	Note
1	SYS_EN	1
3	Not connected	
5	Not connected	
7	Not connected	
9	Not connected	
11	Not connected	
13	Not connected	
15	Not connected	
17	Not connected	
19	GPIO110	1
21	GPIO8	1
23	GPIO103	1
25	GPIO101 / GPIO115	1,5
27	GPIO90 / GPIO106	1,5
29	GPIO105	1
31	GPIO102	1
33	GPIO99	1
35	GPIO100	1
37	GPIO104 / GPIO119	1,5
39	GND	

Pin#	Bottom side	Note
2	GPIO23	1
4	GPIO24	1
6	GPIO25	1
8	Not connected	
10	Not connected	
12	Not connected	
14	GPIO27	1
16	GPIO28	1
18	GPIO29	1
20	GPIO107	1
22	nGPIO_RESET	1
24	BATT_SENSE	4
26	nRESET_IN	1
28	GPIO19	1,5
30	GPIO17	1,5
32	GPIO111	1
34	GPIO114	1
36	GPIO112	1
38	GPIO113	1
40	+3V3 (VCC_BATT)	

Pin#	Top side (Toradex logo)	Note
41	GND	
43	GPIO13 / EXT_WAKEUP0	1,8
45	GPIO127	1
47	GPIO7	1
49	GPIO4	1
51	GPIO5	1
53	GPIO6	1
55	GPIO80	1
57	GPIO70	1
59	GPIO20 / CIF_DD7 (GPIO46)	1,5,9
61	GPIO71	1
63	GPIO31	1
65	GPIO48 / GPIO124	1,5
67	GPIO45	1
69	GPIO77	1
71	GPIO39	1
73	GPIO78	1
75	CIF_MCLK (GPIO49) / GPIO79	1,5,9
77	GPIO81	1
79	GPIO43	1
81	GPIO52 / GPIO83	1,5
83	GND	
85	GPIO47 / GPIO125	1,5
87	nRESET_OUT	1
89	DF_ALE_nWE	1
91	DF_CLE_nOE	1
93	GPIO12 (RDnWR see CPLD descr)	1,6
95	GPIO0	1
97	GPIO44	1
99	nWE (GPIO95)	1,7
101	GPIO41	1
103	GPIO42	1
105	GPIO16 / EXT_nCS0	1,2
107	GPIO15 / EXT_nCS1	1,2
109	GND	
111	ADDRESS[00]	1,10
113	ADDRESS[01]	1,10
115	ADDRESS[02]	1,10
117	ADDRESS[03]	1,10
119	ADDRESS[04]	1,10
121	ADDRESS[05]	1,10
123	ADDRESS[06]	1,10

Pin#	Bottom side	Note
42	+3V3	
44	GPIO75	1,5
46	GPIO61	1,5
48	GPIO63	1
50	GPIO65	1
52	GPIO66	1
54	GPIO67	1
56	GPIO74	1,5
58	GPIO57	1,5
60	GPIO56	1,5
62	GPIO62	1
64	GPIO69	1
66	GPIO68	1
68	GPIO73	1,5
70	GPIO55	1,5
72	GPIO59	1,5
74	GPIO64	1
76	GPIO54	1,5
78	GPIO58	1,5
80	GPIO60	1,5
82	GPIO72	1,5
84	+3V3	
86	GPIO86	1
88	GPIO85	1
90	GPIO87	1
92	GPIO88	1
94	CIF_HSYNC (GPIO51)	1,9
96	CIF_PCLK (GPIO50)	1,9
98	GPIO40	1
100	GPIO122	1
102	GPIO12	1,5
104	GPIO11	1,5
106	GPIO89 / EXT_nCS2	1,2
108	+3V3	
110	ADDRESS[08]	1,10
112	ADDRESS[09]	1,10
114	ADDRESS[10]	1,10
116	ADDRESS[11]	1,10
118	GPIO116	1
120	GPIO117	1
122	GPIO118	1
124	GPIO120	1

Pin#	Top side (Toradex logo)	Note
125	ADDRESS[07]	1,10
127	GPIO11	1
129	GPIO0_2	1,5
131	GPIO1_2	1,5
133	GPIO96	1
135	GPIO97	1
137	GPIO98	1
139	USBH1_P	1
141	USBH1_N	1
143	USBOTG_P	1
145	USBOTG_N	1
147	GND	
149	DATA[00]	1
151	DATA[01]	1
153	DATA[02]	1
155	DATA[03]	1
157	DATA[04]	1
159	DATA[05]	1
161	DATA[06]	1
163	DATA[07]	1
165	DATA[08]	1
167	DATA[09]	1
169	DATA[10]	1
171	DATA[11]	1
173	DATA[12]	1
175	DATA[13]	1
177	DATA[14]	1
179	DATA[15]	1
181	GND	
183	ETH_LINK_ACT	3
185	nETH_SPEED100	3
187	ETH_TXO-	3
189	ETH_TXO+	3
191	GND	
193	ETH_RXI-	3
195	ETH_RXI+	3
197	GND	
199	GND	

Pin#	Bottom side	Note
126	nBE0	1
128	nBE1	1
130	nDF_RE_OE	1
132	nDF_WE	1
134	GPIO38	1,5
136	GPIO2_2	1,5
138	GPIO3_2	1,5
140	GPIO121	1
142	GPIO123	1
144	GPIO4_2	1,5
146	GPIO5_2	1,5
148	+3V3	
150	GPIO82	1
152	GPIO18 / GPIO126	1,5
154	GPIO53 / GPIO91	1,5
156	GPIO92	1
158	GPIO93	1
160	GPIO94	1
162	GPIO32	1
164	GPIO33	1
166	GPIO34	1
168	GPIO35	1
170	GPIO36	1
172	GPIO37	1
174	GPIO10	1
176	GPIO9	1
178	GPIO6_2	1,5
180	GPIO30	1
182	+3V3	
184	GPIO2	1
186	nLUA	1
188	nLLA	1
190	GPIO14	1
192	GPIO3	1
194	GPIO22	1
196	GPIO21	1
198	+3V3	
200	+3V3	

3.2.2 JTAG (X2)

Connector: FCC 8 pins, 0.5mm pitch, bottom contact

Pin Nr.	Signal name	IO Type
1	+3V3	PWR
2	GND	PWR
3	TMS	I
4	nTRST	I
5	TCK	I
6	TDO	O
7	TDI	I
8	nReset_OUT	O

3.2.3 Additional GPIOs (X3)

Connector: FCC 18 pins, 0.5mm pitch, bottom contact

Pin Nr.	Signal name	IO Type
1	GPIO86[1]	IO
2	GPIO3_2[1,5]	IO
3	GPIO110[1]	IO
4	GPIO6_2[1,5]	IO
5	GPIO109[1]	IO
6	GPIO2_2[1,5]	IO
7	GPIO31[1]	IO
8	GPIO108[1]	IO
9	GPIO15_2[1,5]	IO
10	GPIO118[1]	IO
11	GPIO120[1]	IO
12	GPIO116[1]	IO
13	GPIO117[1]	IO
14	GPIO121[1]	IO
15	GPIO123[1]	IO
16	GPIO4_2[1,5]	IO
17	GPIO101 / GPIO115[1,5]	IO
18	GPIO16[1]	IO

Notes: (see next page)

Notes:

1. For the electrical specification please refer to PXA300 Processor Electrical, Mechanical and Thermal Specification Datasheet
2. See chapter 4.2 External Chip Selects for more details.
3. For the electrical specification please refer to Ethernet Controller AX88796B datasheet
4. See chapter 4.1 Batt_Sense for more details.
5. See chapter 4.5 GPIO for more details.
6. SODIMM pin 93 is GPIO12 or can be RDnWR when enabling this signal in CPLD.
   Set GPIO12 to input when using RDnWR. (see 4.3 MEM_CTRL signals for details)
7. SODIMM pin 99 is nWE by default. Ask Toradex if you would like to use this pin as GPIO95.
8. See chapter 4.4 EXT_WAKEUP0 for more details.
9. This pins don't have GPIO as alternate function 0. See 4.5 GPIO for more details.
10. The pins Address[3:0] are the dedicated DF_ADDR[3:0] from the DFI bus of the PXA320.
    The pins Address[11:4] are the demultiplexed addresses from the DFI bus of the PXA320.

4. Signal description

The following signals are Colibri PXA300 specific signals. For descriptions about the other signals see the PXA300, or AX88796B datasheets.

4.1 Batt_Sense

The Batt_Sense signal can be used control the nBatt_Fault signal of the PXA300. It is pulled up on the Colibri with a 1MOhm resistor to VCC.
The nBatt_Fault signal is asserted if the voltage applied to the Batt_Sense input pin drops below 1.2V. It's deasserted if the voltage exceeds 1.25V.

4.2 External Chip Selects

The PXA300 provides only two CS for external use. One of them is used by the Ethernet controller on the module. The other is splitted into three CS. Those are available on the SODIMM pins 105, 106 and 107. You have to enable them by writing the CPLD CS_CTRL register.
All the EXT_nCSx have the same behavior (timings, VLIO, SRAM, etc.). You can change them by modifying the PXA300 nCS3 registers (e.g. CSADRCFG3, MSC1, etc.)
Set all the GPIOs that are multiplexed with these signals to input before enabling the cs.
All CS are disabled after Reset.

4.2.1 EXT_nCSx memory map

0x1780_0000	CPLD Register block (8MB)
0x1700_0000	EXT_nCS2 (8MB)
0x1600_0000	EXT_nCS1 (16MB)
0x1400_0000	EXT_nCS0 (32MB)

4.2.2 CPLD CS_CTRL register (0x1780_0000, write only (read prohibited), 16Bit)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	res	res	res	res	res	EXT_nCS2_DIS	EXT_nCS1_DIS	EXT_nCS0_DIS	res	res	res	res	res	EXT_nCS2_EN	EXT_nCS1_EN	EXT_nCS0_EN

Bit	Name	Description
15:11	res	Reserved
10	EXT_nCS2_DIS	Disable the EXT_nCS2 (on SODIMM PIN 106)
9	EXT_nCS1_DIS	Disable the EXT_nCS1 (on SODIMM PIN 107)
8	EXT_nCS0_DIS	Disable the EXT_nCS0 (on SODIMM PIN 105)
7:3	res	Reserved
2	EXT_nCS2_EN	Enable the EXT_nCS2 (on SODIMM PIN 106)
1	EXT_nCS1_EN	Enable the EXT_nCS1 (on SODIMM PIN 107)
0	EXT_nCS0_EN	Enable the EXT_nCS0 (on SODIMM PIN 105)

4.3 MEM_CTRL Signals

The signal RDnWE is provided through a CPLD on the Colibri PXA300 module. To enable it you have to write the CPLD MEM_CTRL register.
Set the GPIO12 to input before enabling the signal.
RDnWR is disabled by default (reset).

4.3.1 CPLD MEM_CTRL register (0x1780_0004, write only (read prohibited), 16Bit)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	res	res	res	res	res	res	RDnWR_DIS	res	res	res	res	res	res	res	RDnWR_EN	res

Bit	Name	Description
15:10	res	Reserved
9	RDnWR_DIS	Write this bit to 0x1 to disable the RDnWR signal from PXA.
8:2	res	Reserved
1	RDnWR_EN	Write this bit to 0x1 to enable the RDnWR signal from PXA.
0	res	Reserved

4.4 EXT_WAKEUP0

The EXT_WAKEUP0 signal on SODIMM pin 43 is the main wakeup source of the PXA300. For more information about this pin see the PXA300 developer's manual.

4.5 GPIO

Some of the SODIMM pins have more than one GPIO assigned. If you would like to use one of them, then tristate the other one (set to GPIO input). For example if you would like to use an alternate function of the GPIO101 you have to set the GPIO115 to GPIO input.

The GPIO46 and GPIO49-52 don't have GPIO as alternate function 0.
The alternate function GPIO is as mentioned below:
GPIO46 (AltFn 1)
GPIO49 (AltFn 3)
GPIO50 (AltFn 2)
GPIO51 (AltFn 3)
GPIO52 (AltFn 3)

The GPIO0 to GPIO6 have a second instance on the PXA300. (GPIO0_2 to GPIO6_2). They are assigned to different balls on the PXA300. You can use one of them as GPIO and the other one should have a different alternate function than GPIO. The GPIO registers are the same for both (e.g. GPIO0 and GPI0_2 share the same bit in the GPIO level register GPLR0[0]). Be careful when using both as GPIO. When choosing GPIO input, then the value in the GPIO level register is GPIOx OR GPIOx_2. When choosing output, both GPIO pins will provide the level from the level register.

5. Compatibility to Colibri PXAxxx and Trizeps III/IV

Colibri PXA300 modules can be used as a replacement for the Colibri PXA270/Colibri PXA320 (Colibri PXAxxx) or Keith & Koep's Trizeps III / IV family of modules. This chapter points out the differences for a smooth transition.
There is a Migration Guide available on www.toradex.com which shows the compatible signals of all Colibri modules.

5.1 Alternate Function Mapping

Colibri PXA300 and PXAxxx/Trizeps share a compatible pin mapping regarding all pins as GPIOs. However, the mapping GPIOxx to SODIMM pin yy is not identical.
This fact leads to the following consequences:

- As long as Colibri PXA300 pins are used only as general purpose IOs (GPIOs), Colibri PXAxxx and Trizeps III/IV are hardware compatible. Slight Software adaptions are necessary in most projects to transition between Colibri PXAxxx and Trizeps III / IV to remap the GPIO pins.
- Many of the PXA300 pins are multiplexed so they can be configured for use as a general purpose I/O signal (GPIOxx) or as one of several alternate functions (for example as SDIO interface signals). Not all of these alternate functions are available on the same Colibri PXAxxx and Trizeps III / IV pins.

5.2 USB Channels

The Colibri PXA300 module provides one USB host and one USB On-The-Go (selectable host/client) channel as differential pair.
The Colibri PXA300 module can be configured to map the USB OTG channel to SODIMM pins 28 and 30. Contact Toradex for further information.

6. Technical Specifications

6.1 Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
VCC	Power supply voltage	3.1	3.3	3.4	V
IDD_208	Operating current at 208 MHz		tbd	tbd	mA
VIH	Digital input high voltage	VCC*0.8		VCC+0.3	V
VIL	Digital input low voltage	-0.3		VCC*0.2	V

6.2 Mechanical Characteristics

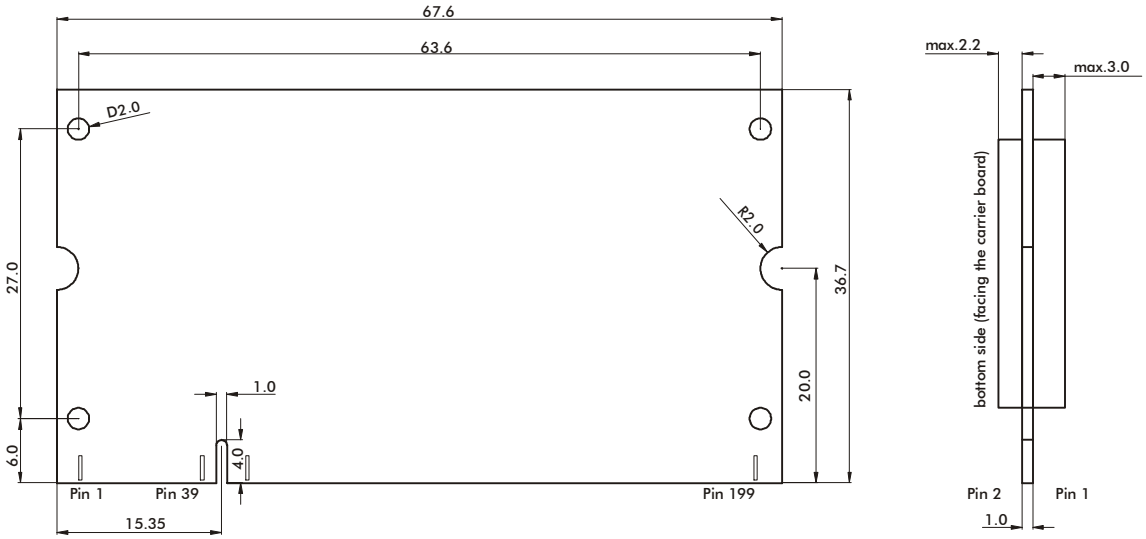


Figure 3: Mechanical dimensions of the Colibri PXA300 module

6.2.1 Sockets for the Colibri PXA300 Module

The Colibri PXA300 module fits into a regular 2.5V (DDR1) SODIMM200 memory socket. A choice of SODIMM200 socket manufacturers is given below:

FCI: http://www.fciconnect.com
Foxconn: http://www.foxconn.com
JAE: http://www.jae.com
Tyco Electronics (AMP): http://www.tycoelectronics.com

6.3 Temperature Range

Module	Description	Min	Typ	Max	Unit
Colibri PXA 300	Operating temperature range	-10		70	°C

6.4 RoHS Compliance

Colibri PXA300 modules comply with the European Union's Directive 2002/95/EC: "Restrictions of Hazardous Substances".

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