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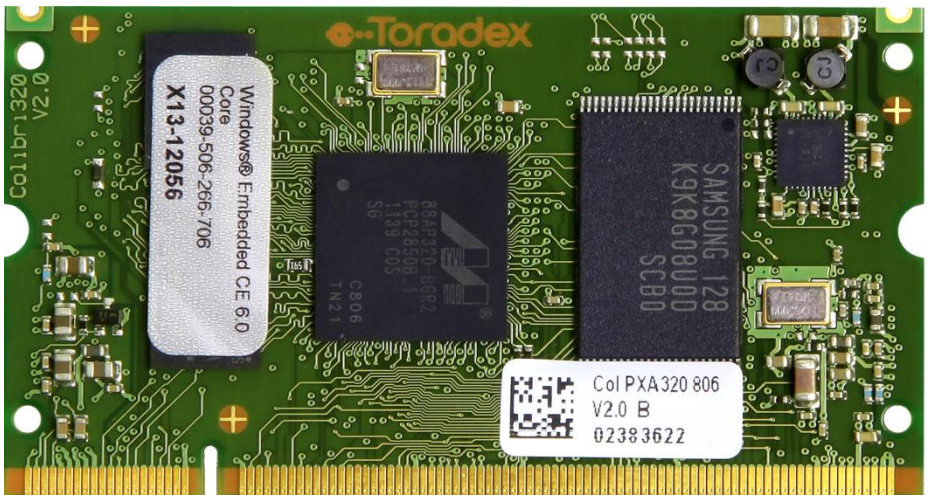
# Colibri XScale® PXA320

## Datasheet



# Revision history

| Date | Doc. Rev. | Colibri PXA320 (IT) Version | Changes |
|---|---|---|---|
| 26-Apr-06 | Rev. 0.1 | V1.0 | Initial Release |
| 18-Sept-06 | Rev. 0.2 | V1.0 | Some tbd values evaluated |
| 10-Nov-06 | Rev. 0.3 | V1.0 | Changed from PXA290 to PXA320 |
| 07-Dec-06 | Rev. 0.4 | V1.0 | Colibri mechanical drawing updated<br>nBATT_FAULT description added |
| 15-Mar-07 | Rev. 1.0 | V1.1 | New HW Revision SODIMM Pin 106, 107, 152, 178 changed assignement; Ext_nCSx available |
| 23-Aug-07 | Rev. 1.2 | V1.2 | CPLD register change (RDnWR can be controlled separately; nOE signal for SODIMM Pin 97 tri-state with CPLD) |
| 24-Dec-07 | Rev. 1.3 | V1.2 | Changed some pin names (MA to address, MD to data) |
| 16-May-08 | Rev. 1.4 | V1.2 | PXA320: changed pin names from -> to (these pins have no GPIO functionality)<br>GPIO56 -> CIF_DD<7><br>GPIO59 -> CIF_MCLK<br>GPIO60 -> CIF_PCLK<br>GPIO61 -> CIF_HSYNC<br>GPIO62 -> CIF_VSYNC<br><br>IT module operating temperature from -40°C to 85°C<br><br>Operation currents updated |
| 25-Nov-08 | Rev. 1.5 | V1.2 | Added note 14 for SODIMM pins 88, 90, 92<br><br>Moved CPLD description to separate document (Colibri PXA CPLD Description) |
| 03-Jun-09 | Rev. 1.6 | V1.2 | Added Tolerance value for PCB outline<br>Added chapter for known issues.<br>Added slew rate and some current consumption values<br>Added new Marvell datasheet link (without NDA) |
| 07-Jul-09 | Rev. 1.7 | V1.2 | Adjusted temperature range (0-70°C) |
| 24-Sep-09 | Rev. 1.8 | V1.2 | Added temperature range description.<br>Deleted compatibility list and referred to Colibri Migration Guide<br>Added note 14 and 15 to SODIMM pin assignment list (SODIMM Pin 88,90,92) |
| 25-May-10 | Rev. 2.0 | V1.2/V2.0 | Added HW V2.0 description (new PMIC, new codec)<br>Added description for VDDA_AUDIO, VSSA_AUDIO and VCC_BAT |
| 04-Jun-10 | Rev. 2.1 | V1.2/V2.0 | Added analog input voltage range description (chap. 4.9) |
| 10-Jun-10 | Rev. 2.2 | V1.2/V2.0 | Added clarification to chap. 4.9 |
| 23-Nov-11 | Rev. 2.3 | V1.2/V2.0 | Changed Disclaimer<br>Clarified nBATT_FAULT description |
| 14-Jan-13 | Rev 2.4 | V1.2/V2.0 | Clarified 4/5-wire Touchscreen and 2D graphic s accelerator capability |
| 04-Dec-14 | Rev. 2.5 | V1.2/V2.0 | Section 7.4 renamed and updated |
| 05-Feb-15 | Rev. 2.6 | V1.2/V2.0 | Section 3.2.1: deleted “SYS_EN” from Pin# 1 details.<br>Section 3.2, note 10 have been updated.<br>Section 3.2, note 7: “Toradex wiki” have been updated to the “Toradex Developer Website”. Web-link has been updated. |

# Contents

# 1. Introduction

## 1.1 Hardware

Colibri XScale® PXA320 is a SODIMM sized computer module based on the new Marvell Xscale® PXA320 processor. It runs at up to 806 MHz at very low power consumption. The module delivers state of the art technology, targeting low power systems that still require high CPU performance.

It also offers all the interfaces needed in a modern embedded device: beside the internal Flash memory, there are plenty of interfaces available for data storage: CompactFlash/ PCMCIA and SDCard. The module provides glueless connectivity to passive and active LCDs with resolutions of up to 1024x768, as well as 4/5-wire resistive touch screens. An integrated 16 bit stereo codec allows Colibri PXA320 to play and record sound. Colibri PXA320 can directly connect to a CMOS/CCD camera sensor.

In addition Colibri PXA320 offers a 100 Mbit Ethernet as well as USB host and USB device functionality.

The 16 bit wide demultiplexed system bus (DFI) is available for custom extensions, such as special interfaces for high bandwidth applications.

For enhanced video processing, a 2D graphics accelerator and 768KB frame buffer are provided.

## 1.2 Software

The module is shipped with a preinstalled WinCE image with a WinCE Core license.
Embedded Linux is available from our developer website.

### 1.2.1 Windows CE

Colibri PXA320 modules are shipped with a valid Windows CE 6.0 core license.
Toradex provides a WinCE5.0 image and a WinCE6.0 (from end of 2007).
All WinCE images contain drivers for the most common interfaces and are easily customizable by registry settings to adapt to specific hardware.

## 1.3 Features

CPU:
- ✓ Marvell PXA320 806 MHz

Memory:
- ✓ 128 Mbyte of DDR SDRAM (32 Bit)
- ✓ 1Gbyte of NAND FLASH (8 Bit)

Interfaces:
- ✓ 16 Bit demultiplexed DFI bus
- ✓ CompactFlash / PCMCIA
- ✓ LCD (up to 1024x768)
- ✓ Touch screen (<V2.0 = 4-wire, V2.0 and higher = 4/5-wire)
- ✓ Audio I/O (16 Bit stereo)
- ✓ CMOS/CCD image sensor interface
- ✓ I2C
- ✓ SPI
- ✓ 2x SDCard (SDIO, MMC )
- ✓ Up to 127 GPIOs
- ✓ USB host / device
- ✓ USB 2.0 device (requires external UTMI chip)
- ✓ 100 Mbit Ethernet
- ✓ One-Wire
- ✓ Keypad
- ✓ Consumer Infrared
- ✓ USIM

Supported operating systems:
- ✓ WinCE 5.0
- ✓ WinCE 6.0

## 1.4 Reference Documents

For detailed technical information about the Colibri PXA320 components, please refer to the documents listed below.

### 1.4.1 Marvell PXA320 Processor Based on Intel Xscale Technology

The datasheets and other technical documents about the PXA3xx processor are available on the Marvell web page.
http://www.marvell.com

### 1.4.2 Ethernet Controller

Up to module HW V1.2: Asix AX88796B:
Module HW V2.0 and higher: Asix AX88796C:
http://www.asix.com.tw

### 1.4.3 Audio Codec and Touch Screen Controller

Up to module HW V1.2: NXP UCB1400:
http://www.nxp.com

Module HW V2.0 and higher: Wolfson WM9715L:
http://www.wolfsonmicro.com

### 1.4.4 Power Management IC

Up to module HW V1.2: Maxim MAX8661:
http://www.maxim-ic.com

Module HW V2.0 and higher: National LP3972SQ:
http://www.national.com

### 1.4.5 CPLD

Xilinx XC2C64A:
http://www.xilinx.com

# 2. Architecture Overview

## 2.1 Block Diagram

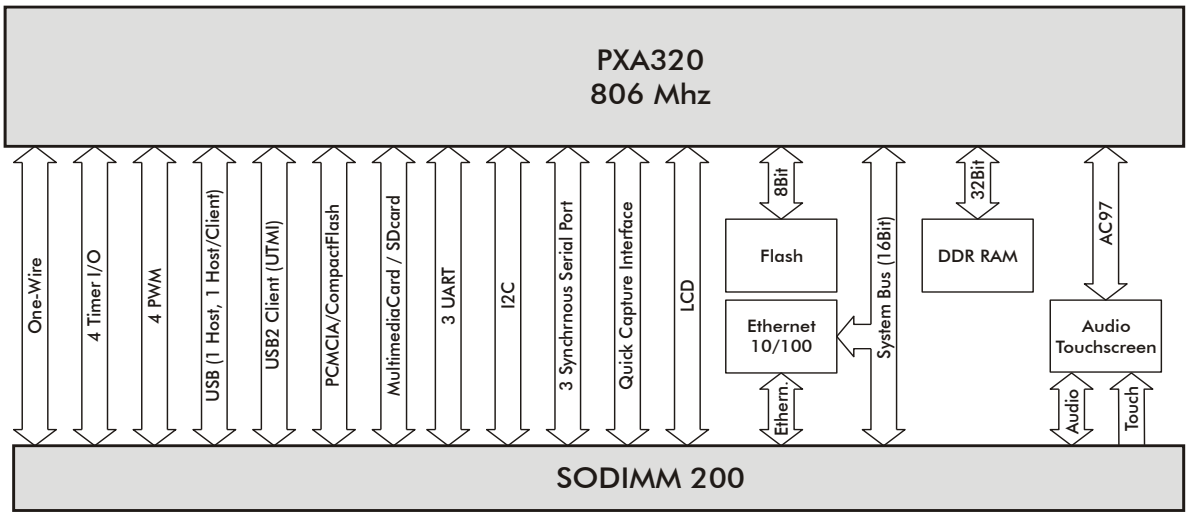



Figure 1: Colibri PXA320 block diagram

Figure 1 shows the Colibri PXA320 interfaces. However, some PXA320 pins are mapped to multiple interfaces. Therefore not all functions can be used simultaneously (for example it is not possible to use the Camera Interface and the CF Card at the same time).

Colibri PXA320 features full 8 bit interfaces to on board NAND FLASH and a 16 bit interface to the Ethernet controller.

Wireless Intel (Marvell) Speedstep® Technology, which adjusts the CPU core voltage dynamically according to the CPU load, and four low-power modes both enable excellent MIPS/mW performance for the Colibri PXA320 module.

# 3. Colibri PXA320 Connectors

## 3.1 Physical Locations

Along with the main 200 Pin SODIMM connector the Colibri PXA320 is equipped with two additional FCC connectors. The position of the connectors is shown in the figure below.

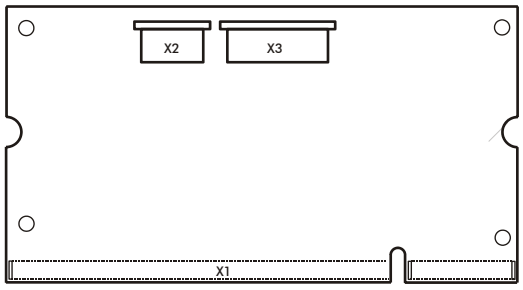



Figure 2: Location of Colibri PXA320's Connectors

## 3.2 Assignment

Some of the following pins are multiplexed, that means there is more than one PXA320 pin connected to one SODIMM or FFC pin. For example GPIO99 and GPIO113 are both assigned to SODIMM pin 25. Take care to tristate (set to input) the unused GPIO of the two multiplexed GPIO's when you are writing your software.

### 3.2.1 SODIMM 200 (X1)

| Pin# | Top side (Toradex logo) | Note |
|---|---|---|
| 1 | MIC_IN | 2,10 |
| 3 | MIC_GND | 2 |
| 5 | LINEIN_L | 2 |
| 7 | LINEIN_R | 2 |
| 9 | VSSA_AUDIO | |
| 11 | VSSA_AUDIO | |
| 13 | HEADPHONE_GND | 2 |
| 15 | HEADPHONE_L | 2 |
| 17 | HEAPHONE_R | 2 |
| 19 | GPIO30 | 1 |
| 21 | GPIO31 | 1 |
| 23 | GPIO101 | 1 |
| 25 | GPIO99 / GPIO113 | 1,5 |
| 27 | GPIO88 / GPIO104 | 1,5 |
| 29 | GPIO103 | 1 |
| 31 | GPIO100 | 1 |
| 33 | GPIO97 | 1 |
| 35 | GPIO98 | 1 |
| 37 | GPIO102 / GPIO117 | 1,5 |
| 39 | GND | |
| 41 | GND | |
| 43 | GPIO28 / EXT_WAKEUP0 | 1,12 |

| Pin# | Bottom side | Note |
|---|---|---|
| 2 | AD3 | 2 |
| 4 | AD2 | 2 |
| 6 | AD1 | 2 |
| 8 | AD0 | 2 |
| 10 | VDDA_AUDIO | |
| 12 | VDDA_AUDIO | |
| 14 | TSPX | 2 |
| 16 | TSMX | 2 |
| 18 | TSPY | 2 |
| 20 | TSMY | 2 |
| 22 | nGPIO_RESET | 1 |
| 24 | nBATT_FAULT (BATT_SENSE) | 1,16 |
| 26 | nRESET_IN | 17 |
| 28 | GPIO13 | 1 |
| 30 | GPIO11 | 1 |
| 32 | GPIO109 | 1 |
| 34 | GPIO112 | 1 |
| 36 | GPIO110 | 1 |
| 38 | GPIO111 | 1 |
| 40 | +3V3 (VCC_BATT) | |
| 42 | +3V3 | |
| 44 | GPIO17_2 | 1,5 |

| Pin# | Top side (Toradex logo) | Note |
|---|---|---|
| 45 | GPIO29 / EXT_WAKEUP1 | 1,12 |
| 47 | GPIO22 | 1 |
| 49 | GPIO19 | 1 |
| 51 | GPIO20 | 1 |
| 53 | GPIO21 | 1 |
| 55 | GPIO78 | 1 |
| 57 | GPIO71 | 1 |
| 59 | GPIO14 / CIF_DD[7] | 1,5 |
| 61 | GPIO72 | 1 |
| 63 | GPIO42 / GPIO105 | 1,5 |
| 65 | GPIO58 / GPIO124 | 1,5 |
| 67 | GPIO55 | 1 |
| 69 | GPIO75 | 1 |
| 71 | GPIO49 | 1 |
| 73 | GPIO76 | 1 |
| 75 | CIF_MCLK / GPIO77 | 1,5 |
| 77 | GPIO79 | 1 |
| 79 | GPIO53 | 1 |
| 81 | CIF_VSYNC / GPIO81 | 1,5 |
| 83 | GND | |
| 85 | GPIO57 / GPIO125 | 1,5 |
| 87 | nRESET_OUT | 1 |
| 89 | DF_ALE_nWE | 1 |
| 91 | DF_CLE_nOE | 1 |
| 93 | GPIO27 (RDnWR) | 1,6 |
| 95 | GPIO2 | 1 |
| 97 | GPIO54 (DF_CLE_nOE) | 1,6 |
| 99 | GPIO93 (DF_ALE_nWE) | 1,7 |
| 101 | GPIO6 / GPIO51 | 1,5 |
| 103 | GPIO5 / GPIO52 | 1,5 |
| 105 | GPIO73 / EXT_nCS0 | 1,11 |
| 107 | GPIO9 / EXT_nCS1 | 1,11 |
| 109 | GND | |
| 111 | ADDRESS[00] | 1,13 |
| 113 | ADDRESS[01] | 1,13 |
| 115 | ADDRESS[02] | 1,13 |
| 117 | ADDRESS[03] | 1,13 |
| 119 | ADDRESS[04] | 1,13 |
| 121 | ADDRESS[05] | 1,13 |
| 123 | ADDRESS[06] | 1,13 |
| 125 | ADDRESS[07] | 1,13 |
| 127 | GPIO26 | 1 |
| 129 | GPIO2_2 | 1,5 |

| Pin# | Bottom side | Note |
|---|---|---|
| 46 | GPIO13_2 | 1,5 |
| 48 | GPIO64 | 1 |
| 50 | GPIO66 | 1 |
| 52 | GPIO67 | 1 |
| 54 | GPIO68 | 1 |
| 56 | GPIO16_2 | 1,5 |
| 58 | GPIO9_2 | 1,5 |
| 60 | GPIO8_2 | 1,5 |
| 62 | GPIO63 | 1 |
| 64 | GPIO70 | 1 |
| 66 | GPIO69 | 1 |
| 68 | GPIO15_2 | 1,5 |
| 70 | GPIO7_2 | 1,5 |
| 72 | GPIO11_2 | 1,5 |
| 74 | GPIO65 | 1 |
| 76 | GPIO6_2 | 1,5 |
| 78 | GPIO10_2 | 1,5 |
| 80 | GPIO12_2 | 1,5 |
| 82 | GPIO14_2 | 1,5 |
| 84 | +3V3 | |
| 86 | GPIO84 | 1 |
| 88 | GPIO83 | 1,14,15 |
| 90 | GPIO85 | 1,14 |
| 92 | GPIO86 | 1,14,15 |
| 94 | CIF_HSYNC / nPCE1 | 1,8 |
| 96 | CIF_PCLK / nPCE2 | 1,8 |
| 98 | GPIO50 / nPREG | 1,8 |
| 100 | GPIO122 / nPXCVREN | 1,4,8 |
| 102 | GPIO8 | 1 |
| 104 | GPIO7 | 1 |
| 106 | GPIO87/ DREQ / EXT_nCS2 | 1,9,11 |
| 108 | +3V3 | |
| 110 | ADDRESS[08] | 1,13 |
| 112 | ADDRESS[09] | 1,13 |
| 114 | ADDRESS[10] | 1,13 |
| 116 | ADDRESS[11] | 1,13 |
| 118 | GPIO114 | 1 |
| 120 | GPIO115 | 1 |
| 122 | GPIO116 | 1 |
| 124 | GPIO118 | 1 |
| 126 | nBE0 | 1 |
| 128 | nBE1 | 1 |
| 130 | nDF_RE_OE | 1 |

| Pin# | Top side (Toradex logo) | Note |
|---|---|---|
| 131 | GPIO3_2 | 1,5 |
| 133 | GPIO94 | 1 |
| 135 | GPIO95 | 1 |
| 137 | GPIO96 | 1 |
| 139 | USBH1_P | 1 |
| 141 | USBH1_N | 1 |
| 143 | USBOTG_P | 1 |
| 145 | USBOTG_N | 1 |
| 147 | GND | |
| 149 | DATA[00] | 1 |
| 151 | DATA[01] | 1 |
| 153 | DATA[02] | 1 |
| 155 | DATA[03] | 1 |
| 157 | DATA[04] | 1 |
| 159 | DATA[05] | 1 |
| 161 | DATA[06] | 1 |
| 163 | DATA[07] | 1 |
| 165 | DATA[08] | 1 |
| 167 | DATA[09] | 1 |
| 169 | DATA[10] | 1 |
| 171 | DATA[11] | 1 |
| 173 | DATA[12] | 1 |
| 175 | DATA[13] | 1 |
| 177 | DATA[14] | 1 |
| 179 | DATA[15] | 1 |
| 181 | GND | |
| 183 | ETH_LINK_ACT | 3 |
| 185 | nETH_SPEED100 | 3 |
| 187 | ETH_TXO- | 3 |
| 189 | ETH_TXO+ | 3 |
| 191 | GND | |
| 193 | ETH_RXI- | 3 |
| 195 | ETH_RXI+ | 3 |
| 197 | GND | |
| 199 | GND | |

| Pin# | Bottom side | Note |
|---|---|---|
| 132 | nDF_WE | 1 |
| 134 | GPIO10 | 1 |
| 136 | GPIO119 | 1 |
| 138 | GPIO120 | 1 |
| 140 | GPIO121 | 1 |
| 142 | GPIO123 | 1 |
| 144 | GPIO126 | 1 |
| 146 | GPIO127 | 1 |
| 148 | +3V3 | |
| 150 | GPIO80 | 1 |
| 152 | GPIO0_2 / GPIO12 | 1,5 |
| 154 | GPIO89 | 1 |
| 156 | GPIO90 | 1 |
| 158 | GPIO91 | 1 |
| 160 | GPIO92 | 1 |
| 162 | GPIO43 | 1 |
| 164 | GPIO44 | 1 |
| 166 | GPIO45 | 1 |
| 168 | GPIO46 | 1 |
| 170 | GPIO47 / GPIO82 | 1,5 |
| 172 | GPIO48 | 1 |
| 174 | GPIO25 | 1 |
| 176 | GPIO24 | 1 |
| 178 | GPIO5_2 | 1,5 |
| 180 | GPIO41 | 1 |
| 182 | +3V3 | |
| 184 | nXCVREN | 1 |
| 186 | nLUA | 1 |
| 188 | nLLA | 1 |
| 190 | GPIO23 | 1 |
| 192 | GPIO18 | 1 |
| 194 | GPIO33 | 1 |
| 196 | GPIO32 | 1 |
| 198 | +3V3 | |
| 200 | +3V3 | |

### 3.2.2 JTAG (X2)

Connector: FCC 8 pins, 0.5mm pitch, bottom contact

| Pin Nr. | Signal name | IO Type |
|---|---|---|
| 1 | +3V3 | PWR |
| 2 | GND | PWR |
| 3 | TMS | I |

| Pin Nr. | Signal name | IO Type |
|---|---|---|
| 4 | nTRST | I |
| 5 | TCK | I |
| 6 | TDO | O |
| 7 | TDI | I |
| 8 | nReset_OUT | O |

### 3.2.3 Additional GPIOs (X3)

Connector: FCC 18 pins, 0.5mm pitch, bottom contact

| Pin Nr. | Signal name | IO Type |
|---|---|---|
| 1 | GPIO16 | IO |
| 2 | GPIO120 | IO |
| 3 | GPIO108 | IO |
| 4 | GPIO5_2[5] | IO |
| 5 | GPIO107 | IO |
| 6 | GPIO119 | IO |
| 7 | GPIO42 / GPIO105[5] | IO |
| 8 | GPIO106 | IO |
| 9 | GPIO127 | IO |
| 10 | GPIO116 | IO |
| 11 | GPIO118 | IO |
| 12 | GPIO114 | IO |
| 13 | GPIO115 | IO |
| 14 | GPIO121 | IO |
| 15 | GPIO123 | IO |
| 16 | GPIO126 | IO |
| 17 | GPIO17 | IO |
| 18 | GPIO15 | IO |

Notes: (see next page)

Notes:

1. For the electrical specification please refer to PXA320 Processor Electrical, Mechanical and Thermal Specification Datasheet
2. For the electrical specification please refer to Audio and Touch Screen Controller datasheet.
   The input voltage ranges of the analog input pins (AD[3:0]) are different depending on the Colibri module version.
   See chapter 1.4.3 and 4.9
3. For the electrical specification please refer to Ethernet Controller AX88796B datasheet
4. nPXCVREN could be used to control a PCMCIA transceiver.
5. See chapter 4.6 GPIO for more details.
6. SODIMM pin 97 is GPIO54 or can be DF_CLE_nOE when enabling this signal in CPLD register.
   SODIMM pin 93 is GPIO27 or can be RDnWR when enabling this signal in CPLD.
   Set the corresponding GPIO to input when using nOE or RDnWR. (see 4.3 MEM Ctrl Signals for details)
7. Up to HW V1.2: SODIMM pin 99 is DF_ALE_nWE by default. GPIO93 cannot be used.
   HW V2.0 and higher: SODIMM pin 99 is GPIO93 by default. It is possible to enable the DF_ALE_nWE signal on this pin by software. Visit the Toradex developer website for more details (http://developer.toradex.com/)
8. See chapter 4.3 MEM Ctrl Signals for details.
9. See chapter 4.5 DREQ for more information.
10. On Colibri PXA320, the SYS_EN signal is not available on the SODIMM pin 1.
11. See chapter 4.2 External Chip Selects for more details.
12. See chapter 4.4 EXT_WAKEUPx for more details.
13. The pins Address[3:0] are the dedicated DF_ADDR[3:0] from the DFI bus of the PXA320.
    The pins Address[11:4] are the demultiplexed addresses from the DFI bus of the PXA320.
14. These pins are used when updating the CPLD on the PXA (SODIMM pin 88, 90, 92). Do not drive these pins until the CPLD update is done. The CPLD update has to be started manually (Toradex Bootloader V3.3 and higher). You can use these pins when not performing a CPLD update.
15. These pins have an internal pull-up of about 10kOhm.
16. See nBATT_FAULT signal description in chapter 4.1 of this document.
17. Up to HW V1.2: nRESET_IN is connected to the MR# pin of the Maxim 8661 IC, to a 100kOhm pull-up resistor and to a 100nF capacitor to GND.
    HW V2.0 and higher: nRESET_IN is connected to the nRSTI pin of the National LP3972SQ IC, to a 100kOhm pull-up resistor and to a 100nF capacitor to GND.

# 4. Signal description

The following signals are Colibri PXA320 specific signals. For descriptions about the other signals see the corresponding datasheets mentioned in chapter 1.4 *Reference Documents*.

## 4.1 nBATT_FAULT (formerly BATT_SENSE)

The nBATT_FAULT signal can be used control the nBATT_FAULT signal of the PXA3xx.

### 4.1.1 For Colibri PXA320 up to V 1.2

nBATT_FAULT is connected to the LBF and LBR input of the Maxim 866x PMIC and to a 1MOhm pull-up resistor to VCC on the Colibri module.
The nBatt_Fault signal of the PXA3xx gets asserted if the voltage applied to the nBATT_FAULT input pin drops below 1.2V. It's deasserted if the voltage exceeds 1.25V.

### 4.1.2 For Colibri PXA320 V2.0 and higher

The nBATT_FAULT signal is connected to the PXA3xx's nBATT_FAULT pin through a diode. You can always pull down this signal externally to assert the nBATT_FAULT signal of the PXA.
This signal is also connected to the power management IC LP3972 on the Colibri and is asserted when VCC_BATT is present and the +3.3V supply is below 2.8V. It de-asserts when the +3.3V supply is above 3.0V (Default PMIC values).

## 4.2 External Chip Selects

See Colibri PXA CPLD Description document for more details.

## 4.3 MEM Ctrl Signals

See Colibri PXA CPLD Description document for more details.

## 4.4 EXT_WAKEUPx

The EXT_WAKEUPx signals on SODIMM pin 43 and 45 are the main wakeup sources of the PXA320. Tristate (set to input) the corresponding GPIO's when using these pins as EXT_WAKEUP.
For more information about these pins see the PXA320 developer's manual.

## 4.5 DREQ

DREQ is an alternate function of the PXA320 GPIO[0]. If you would like to use this function then enable this alternate function for GPIO[0], set GPIO[87] to input and disable the EXT_nCS2. Now you can use the SODIMM pin 106 as DREQ input.

## 4.6 GPIO

Some of the SODIMM pins have more than one GPIO assigned. If you would like to use one of them, then tristate the other one (set to GPIO input). For example you can use an alternate function of the GPIO99. Then you have to set the GPIO113 to GPIO input.

CIF_DD<7>, CIF_MCLK, CIF_PCLK, CIF_HSYNC and CIF_VSYNC (former GPIO 56 and 59-62) on PXA320 don't have an alternate function GPIO (neither altFn0 nor another altFn is GPIO).
Recommendation for PXA320 and compatible designs:
Don't use SODIMM pin 94 (CIF_HSYNC) and SODIMM pin 96 (CIF_PCLK) as GPIO. You can use SODIMM pins 59, 75 and 81(CIF_DD<7>, CIF_MCLK and CIF_VSYNC) as GPIO because there is another GPIO multiplexed to this SODIMM pins. Set the alternate function of CIF_DD<7>, CIF_MCLK and CIF_VSYNC to 0x7 (tristate) if you would like to use the multiplexed GPIO's.

The GPIO0 to GPIO17 have a second instance on the PXA320. (GPIO0_2 to GPIO17_2). They are assigned to different balls on the PXA320. You can use one of them as GPIO and the other one should have a different alternate function than GPIO. The GPIO registers are the same for both (e.g.

GPIO0 and GPI0_2 share the same bit in the GPIO level register GPLR0[0]). Be careful when using both as GPIO. When choosing GPIO input, then the value in the GPIO level register is GPIOx OR GPIOx_2. When choosing output, both GPIO pins will provide the level from the level register.

## 4.7 VCC_BATT

This power domain can be used to power the VCC_BATT power domain of the PXA processor. For general designs it is recommended to connect this pin to normal +3.3V power supply. This pin must be powered in order to boot the Colibri successfully.

## 4.8 VDDA_AUDIO, VSSA_AUDIO

These pins must be connected to 3.3V and GND even if audio and touch-screen functionality aren't used. You can connect this to normal 3.3V and GND or to filtered 3.3V and GND for better audio quality.

## 4.9 Analog Inputs AD[3:0]

Input Voltage Range is different depending on module version:
Colibri PXA320 up to V1.2
- AD[3:0]: 0V to 7.5V
Colibri PXA320 V2.0 and higher:
- AD[3, 1, 0]: 0V to 3.3V
- AD[2]: 0V to 5V

We recommend using 3.3V as maximum voltage on all AD inputs to ensure the compatibility to future Colibri modules.

# 5. Compatibility to Colibri PXAxxx and Trizeps III/IV

Colibri PXA320 modules can be used as a replacement for the Colibri PXA270 or Keith & Koep's Trizeps III / IV family of modules. This chapter points out the differences for a smooth transition.

## 5.1 Alternate Function Mapping

Colibri PXA3xx and PXA270/Trizeps share a compatible pin mapping regarding all pins as GPIOs. However, the mapping GPIOxx to SODIMM pin yy is not identical.
This fact leads to the following consequences:

- As long as Colibri PXA320 pins are used only as general purpose Ios (GPIOs), Colibri PXA320, Colibri PXA270 and Trizeps III/IV are hardware compatible. Slight Software adaptions are necessary in most projects to transition between Colibri PXA320, Colibri PXA270 and Trizeps III / IV to remap the GPIO pins.
- Many of the PXA320 pins are multiplexed so they can be configured for use as a general purpose I/O signal (GPIOxx) or as one of several alternate functions (for example as SDIO interface signals). Not all of these alternate functions are available on the same Colibri PXA270 and Trizeps III / IV pins.

## 5.2 Compatibility Lists

See the Colibri PXAxxx Migration Guide for details about compatibility of the whole Colibri family.

## 5.3 USB Channels

The Colibri PXA320 module provides one USB host and one USB On-The-Go (selectable host/client) channel as differential pair.
The Colibri PXA320 module can be configured to map the USB OTG channel to SODIMM pins 28 and 30. Contact Toradex for further information.

# 6. Known Issues

## 6.1 Start-up behavior

On the Colibri PXA320 HW Rev. up to V1.2 there is a problem regarding pin states of the GPIOs during power-on of the module. The pin states are not defined in the first 2s to 2.5s after supplying the main voltage. They can be tied to GND or VCC, weak pulled-up or down or even floating.
To prevent inaccurate behavior of the HW connected to the GPIOs a convenient circuit should be attached for the affected signals. E.g. a buffer circuit could be used. Pull-up or down the signal after the buffer, as you wish to make sure your HW gets the right signal level all the time during start-up. Use the nRESET_OUT signal as buffer enable. The nRESET_OUT signal is asserted (low) during start-up and gets high when the core is ready to proceed. From this time on the GPIOs are pulled-up or down as mentioned it the PXA3xx datasheets (EMTS). After a short time all the GPIOs are set to floating input therefore put a pull-up/down resistor on both, the input and the output of the buffer.
On the Colibri HW Rev. 2.0 and higher the GPIOs behave as described in the PXA320 datasheets. But take care because short glitches could occur during ramp-up of the supply voltages.

# 7. Technical Specifications

## 7.1 Electrical Characteristics

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VCC | Power supply operating voltage | 3.0 | 3.3 | 3.6 | V |
| IDD_806A | Operating at 806 MHz, Ethernet off, Display off, Idle | | 220 | | mA |
| IDD_806B | Operating at 806 MHz, Ethernet off, Display on, Idle | | 244 | | mA |
| IDD_806C | Operating at 806 MHz, Ethernet off, Display on, 100% CPU | | 428 | 678 | mA |
| IDD_ETHL | Ethernet on with link | | +106 | | mA |
| IDD_ETHNL | Ethernet on, no link (probing with default timings) | | +81 | | mA |
| IDD_SUSP | In Suspend-Mode | | 2.1 | | mA |
| VIH | Digital input high voltage | VCC*0.8 | | VCC+0.3 | V |
| VIL | Digital input low voltage | -0.3 | | VCC*0.2 | V |
| VCC_SR | VCC Slew Rate | 2 | | 12 | kV/s |

## 7.2 Mechanical Characteristics

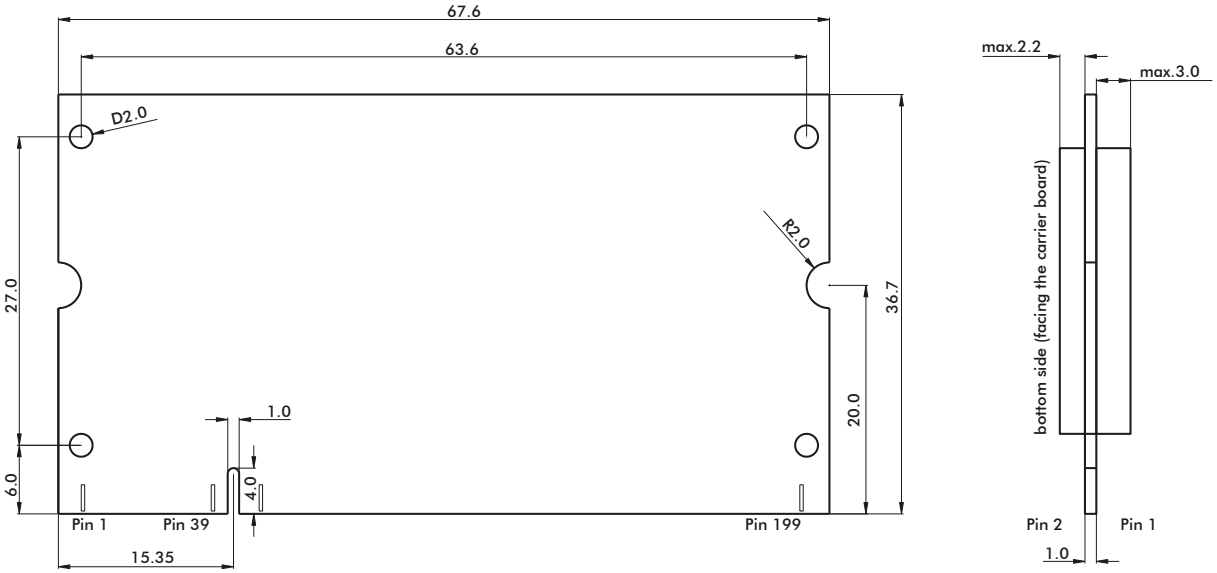



Figure 3: Mechanical dimensions of the Colibri PXA320 module
Tolerance for all measures: +/- 0.1mm

### 7.2.1 Sockets for the Colibri PXA320 Module

The Colibri PXA320 module fits into a regular 2.5V (DDR1) SODIMM200 memory socket.
A choice of SODIMM200 socket manufacturers is given below:

| | |
|---|---|
| FCI: | http://www.fciconnect.com |
| Foxconn: | http://www.foxconn.com |
| JAE: | http://www.jae.com |
| Tyco Electronics (AMP): | http://www.tycoelectronics.com |

## 7.3 Temperature Range

| Module | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Colibri PXA 320 | Operating temperature range | 0 | | 70[1] | °C |
| Colibri PXA320 IT | Operating temperature range | -40 | | 85[1] | °C |

Notes:

1. The maximum temperature is limited by the case temperature of the PXA processor which must not exceed 85°C. For passive thermal solutions this may result in an ambient temperature lower than the stated value. For further details please refer to Marvell's EMTS datasheet.

## 7.4 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH etc. can be found on our website at: http://www.toradex.com/support/product-compliance