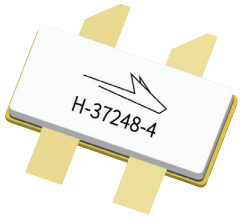
PXAC200902FC

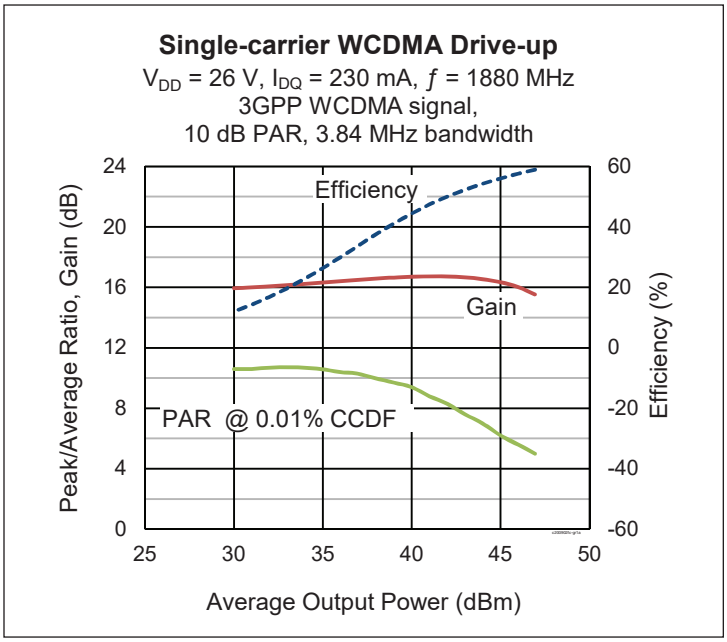
Thermally-Enhanced High Power RF LDMOS FET
90 W, 28 V, 1805 – 2170 MHz

Description

The PXAC200902FC is a 90-watt LDMOS FET with an asymmetric deisgn intended for use in multi-standard cellular power amplifier applications in the 1805 to 2170 MHz frequency band. Features include dual path design, input and output matching, high gain and a thermally-enhanced push-pull package with earless flange. Manufactured with Wolfspeed's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



PXAC200902FC
Package H-37248-4



Features

- Broadband internal input and output matching
- • Asymmetric Doherty design
  - Main: P1dB = 35 W Typ
  - Peak: P1dB = 55 W Typ
- Typical CW performance, 1920 MHz, 26 V,
  - Output power at P_{1dB} = 50 W
  - Efficiency = 58%
  - Gain = 16.6 dB
- Capable of handling 10:1 VSWR @28 V, 90 W (CW) output power
- Integrated ESD protection
- ESD Rating: Human Body Model, Class 1C (per ANSI/ESDA/JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in Wolfspeed Doherty test fixture)
V_{DD} = 26 V, I_{DQ} = 230 mA, $V_{GS(peak)}$ = 1.3 V, P_{OUT} = 15 W avg, f = 1920 MHz, 3GPP WCDMA signal, 3.84 MHz channel bandwidth, 10 dB peak/average @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	16.5	17.2	—	dB
Drain Efficiency	η_D	45.0	50.3	—	%
Adjancent Channel Power Ratio	ACPR	—	–27.0	–25.5	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics

Characteristic		Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage		V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	(main & peak)	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	0.1	µA
		V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
Gate Leakage Current	(main & peak)	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	0.1	µA
On-State Resistance	(main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.22	—	Ω
	(peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.16	—	Ω
Operating Gate Voltage	(main)	V_{DS} = 26 V, I_{DQ} = 230 mA	V_{GS}	2.15	2.65	3.15	V
	(peak)	V_{DS} = 26 V, I_{DQ} = 0 A	V_{GS}	0.80	1.30	1.80	V

Maximum Ratings

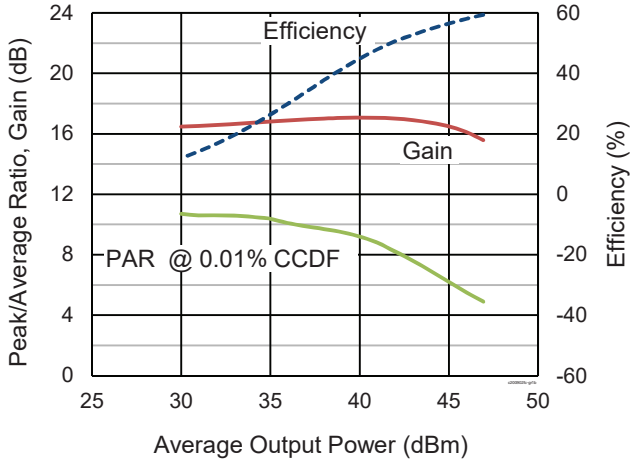
Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	65	V
Gate-Source Voltage		V_{GS}	–6 to +10	V
Operating Voltage		V_{DD}	0 to +32	V
Junction Temperature		T_J	225	°C
Storage Temperature Range		T_{STG}	–65 to +150	°C
Thermal Resistance	Main (T_{CASE} = 70°C, 26 V, I_{DQ} = 230 mA, 15 W CW)	$R_{\theta JC}$	1.75	°C/W
	Peak (T_{CASE} = 70°C, 26 V, V_{GS} = 1.3 V, 41 W CW)	$R_{\theta JC}$	0.76	°C/W

Ordering Information

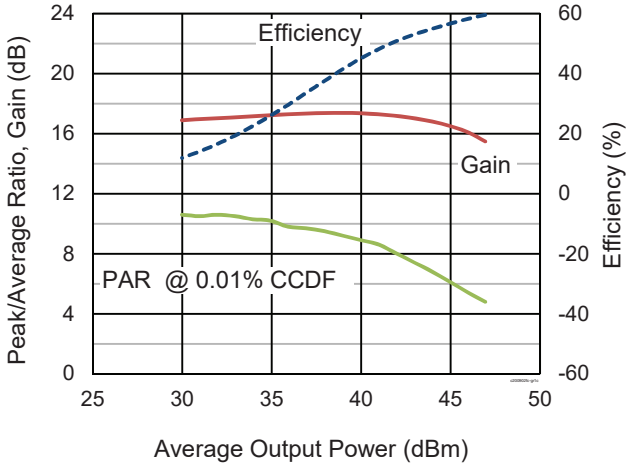
Type and Version	Order Code	Package and Description	Shipping
PXAC200902FC V1 R0	PXAC200902FC-V1-R0	H-37248-4, ceramic open cavity push-pull, earless flange	Tape & Reel, 50 pcs
PXAC200902FC V1 R2	PXAC200902FC-V1-R2	H-37248-4, ceramic open cavity push-pull, earless flange	Tape & Reel, 250 pcs

Typical Performance (data taken in a production Doherty test fixture)

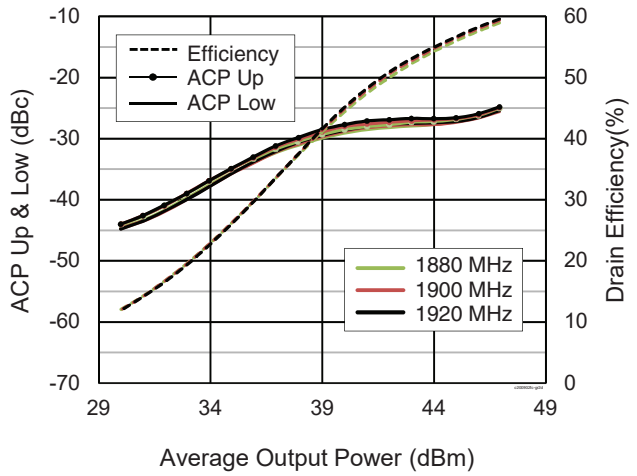
Single-carrier WCDMA Drive-up
V_{DD} = 26 V, I_{DQ} = 230 mA, f = 1900 MHz
3GPP WCDMA signal,
10 dB PAR, 3.84 MHz bandwidth



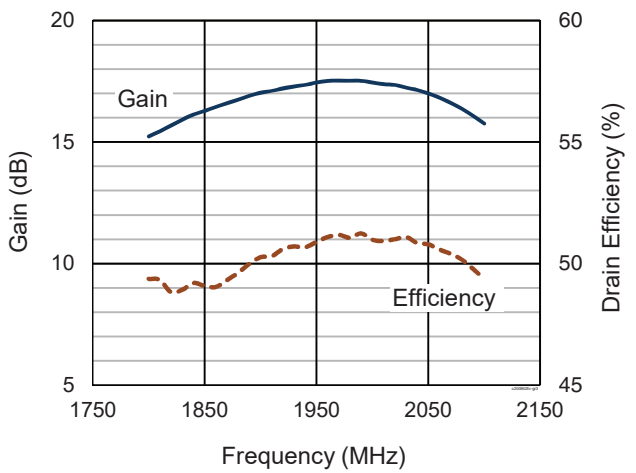
Single-carrier WCDMA Drive-up
V_{DD} = 26 V, I_{DQ} = 230 mA, f = 1920 MHz
3GPP WCDMA signal,
10 dB PAR, 3.84 MHz bandwidth



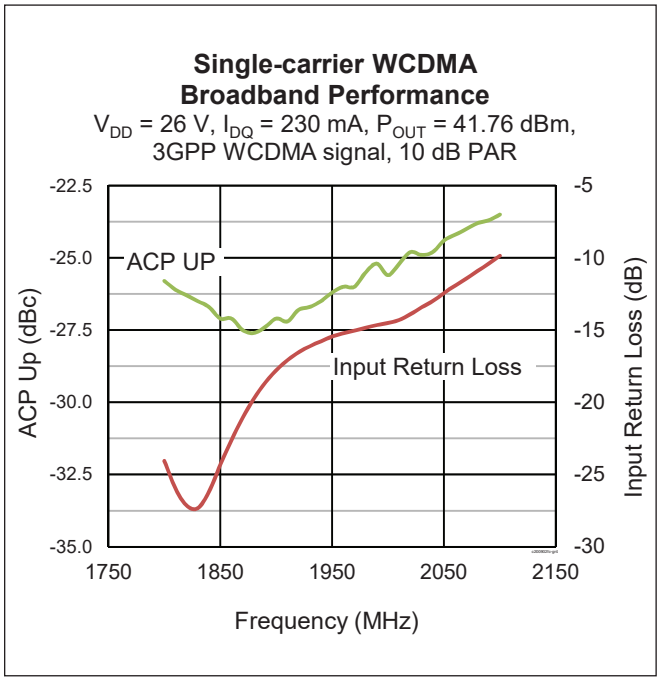
Single-carrier WCDMA 3GPP Drive-up
V_{DD} = 26 V, I_{DQ} = 230 mA, f = 1880-1920 MHz
3GPP WCDMA signal,
10 dB PAR, 3.84 MHz bandwidth

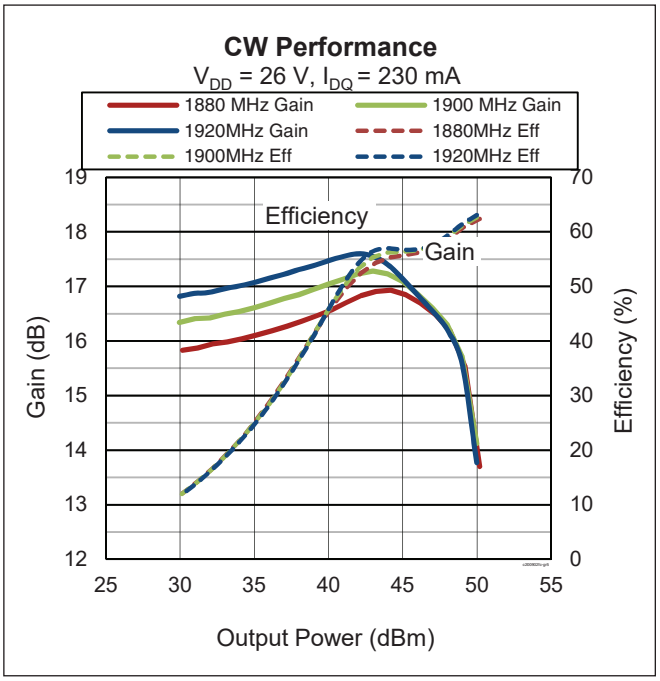


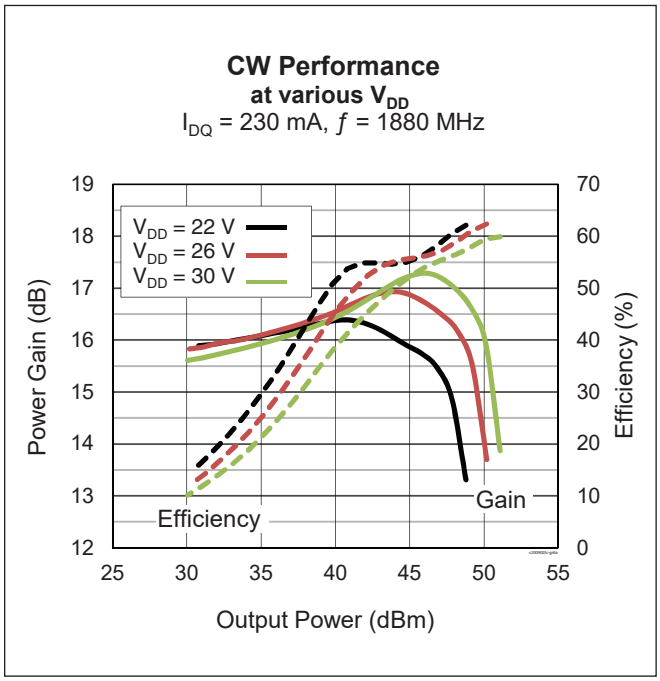
Single-carrier WCDMA Broadband Performance
V_{DD} = 26 V, I_{DQ} = 230 mA, P_{OUT} = 41.76 dBm
3GPP WCDMA signal, 10 dB PAR

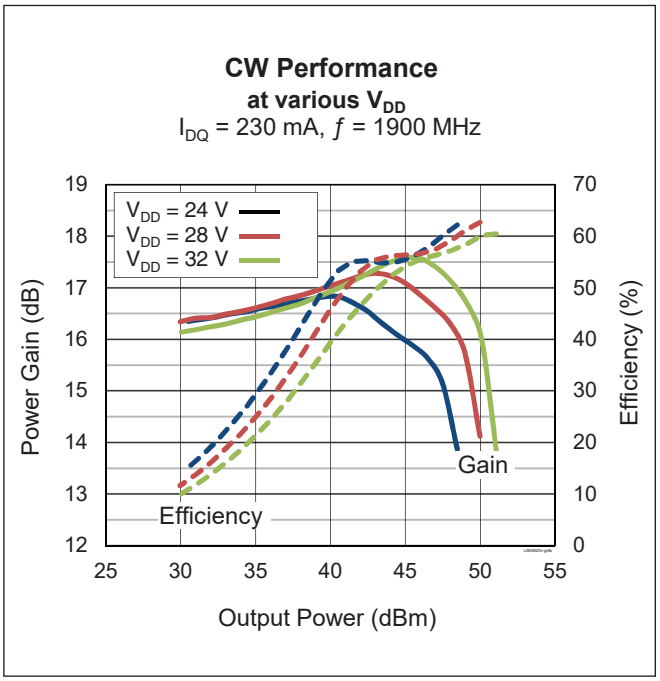


Typical Performance (cont.)

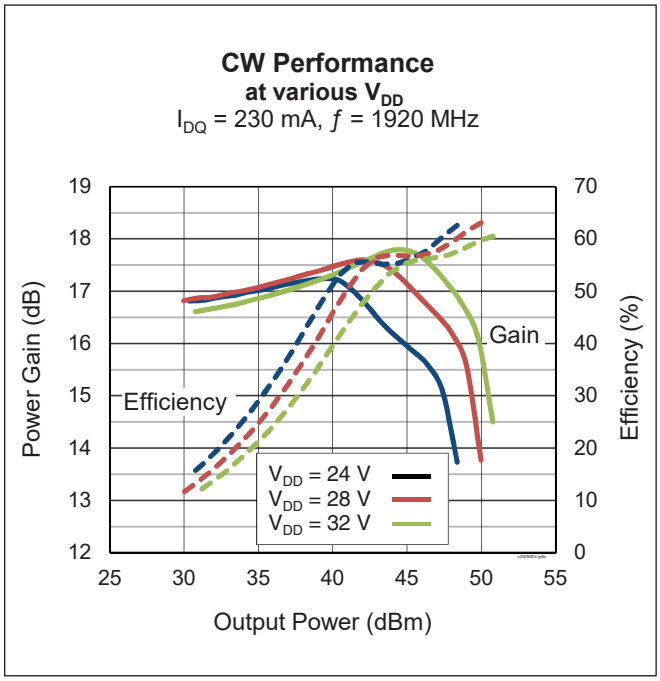


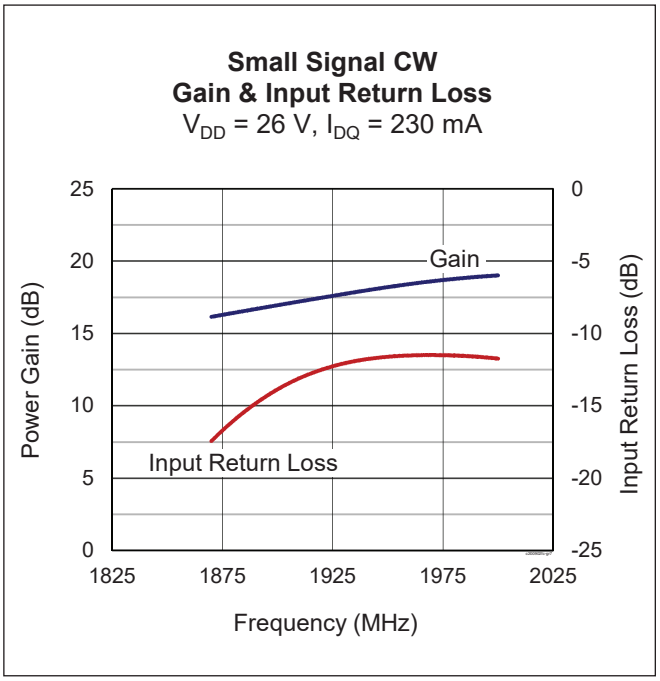






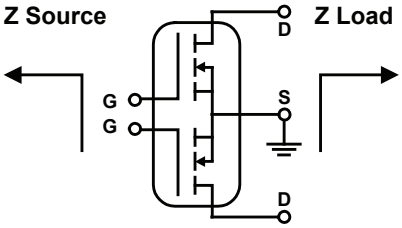
Typical Performance (cont.)





See next page for load pull information

Load Pull Performance



Main side load pull, pulsed CW signal: 160 µs, 10% duty cycle, V_{DD} = 28 V, I_{DQ} = 230 mA

		P_{1dB}									
Class AB		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
1880	8.89 – j15.56	6.31 – j9.65	19.5	46.76	47.4	57.3	12.29 – j4.78	21.8	44.96	31.3	68.5
1900	9.25 – j15.69	5.47 – j10.96	18.8	46.4	43.7	49.8	12.17 – j5.25	21.9	44.62	29	64.1
1920	12.83 – j18.84	6.42 – j10.7	19.5	46.6	45.7	55.7	11.76 – j4.27	22.0	44.6	28.8	66.5

Peak side load pull, pulsed CW signal: 160 µs, 10% duty cycle, V_{DD} = 28 V, I_{DQ} = 280 mA

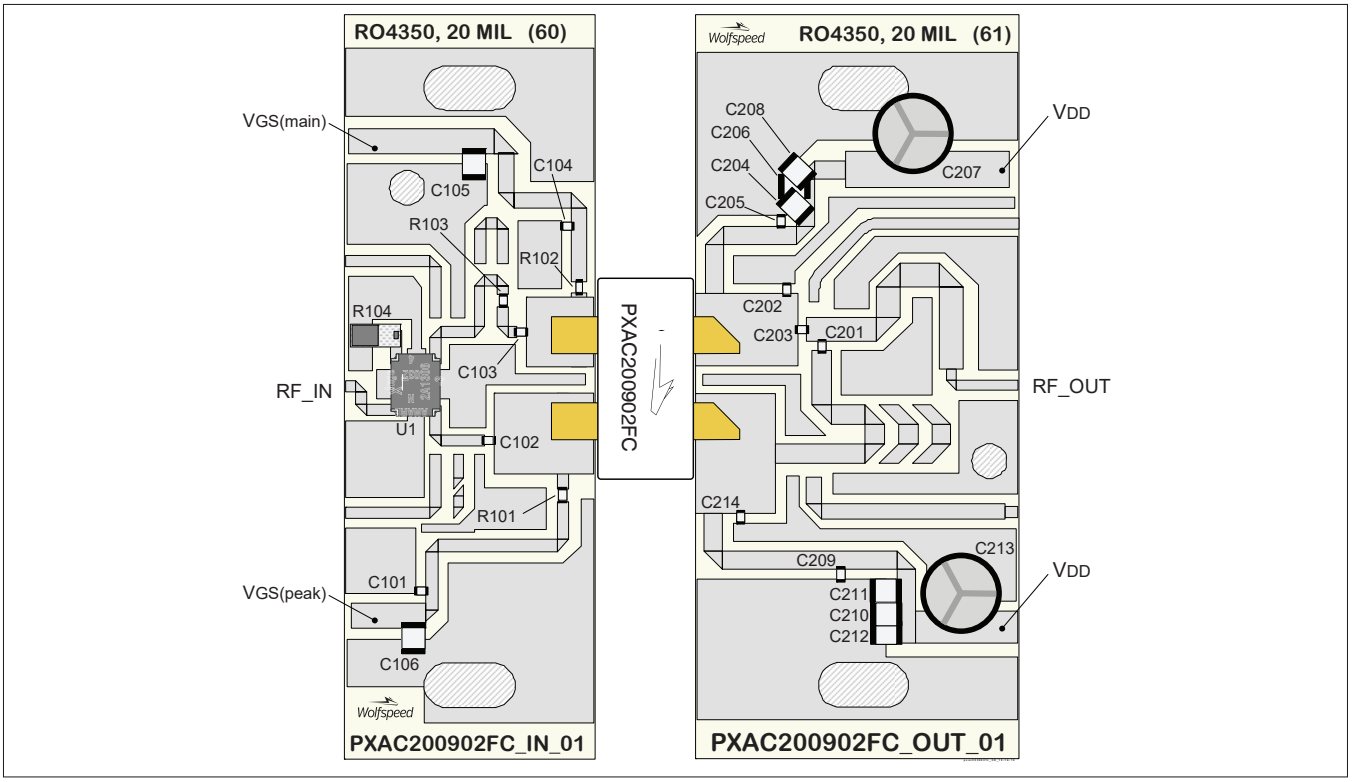
		P_{1dB}									
Class AB		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
1880	3.46 – j8.04	3.21 – j6.17	19.3	48.4	69.2	56.8	3.21 – j6.17	22.3	45.96	39.4	68.6
1900	3.5 – j8.19	3.21 – j6.44	19.3	48.1	64.6	53.8	6.2 – j3.08	22.1	45.9	38.9	64.3
1920	4.29 – j9.3	3.03 – j6.35	19.3	48.3	67.6	54.6	5.33 – j3.12	21.9	46.3	42.7	66.0

Reference Circuit Assembly, 1880 – 1920 MHz

DUT	PXAC200902FC V1
Reference Circuit No.	LTA/PXAC200902FC V1
Order Code	LTA/PXAC200902FC V1
PCB	Rogers 4350, 0.508 mm [0.020”] thick, 2 oz. copper, ε_r = 3.66

Find Gerber files for this test fixture on the Wolfspeed Web site at **http://www.wolfspeed.com/RF**

Reference Circuit (cont.)

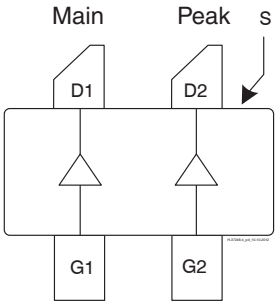


Reference circuit assembly diagram (not to scale)

Components Information

Component	Description	Manufacturer	P/N
In			
C101, C102, C104	Capacitor, 18 pF	ATC	ATC600F180JW250T
C103	Capacitor, 9.1 pF	ATC	ATC600F9R1JW250T
C105, C106	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T
R101, R102	Resistor, 10 Ω	Panasonic	ERJ-8GEYJ100V
R103	Resistor, 5.6 Ω	Panasonic	ERJ-8RQJ5R6V
R104	Resistor, 50 Ω	Anaren	C8A50Z4A
U1	Hybrid Coupler	Anaren	X3C19P1-03S
Out			
C201	Capacitor, 15 pF	ATC	ATC600F150JW250T
C202	Capacitor, 0.7 pF	ATC	ATC600F0R7CW250T
C203	Capacitor, 10 pF	ATC	ATC600F100JW250T
C204, C206, C208, C210, C211, C212	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T
C205, C209	Capacitor, 18 pF	ATC	ATC600F180JW250T
C207, C213	Capacitor, 220 µF	Cornell Dubilier Electronics	SK221M050ST
C214	Capacitor, 1.6 pF	ATC	ATC600F1R6JW250T

Pinout Diagram (top view)



Pin Description
D1 Drain device 1 (Main)
D2 Drain device 2 (Peak)
G1 Gate device 1 (Main)
G2 Gate device 2 (Peak)
S Source (flange)

See next page for package outline specifications

Package Outline Specifications

Package H-37248-4

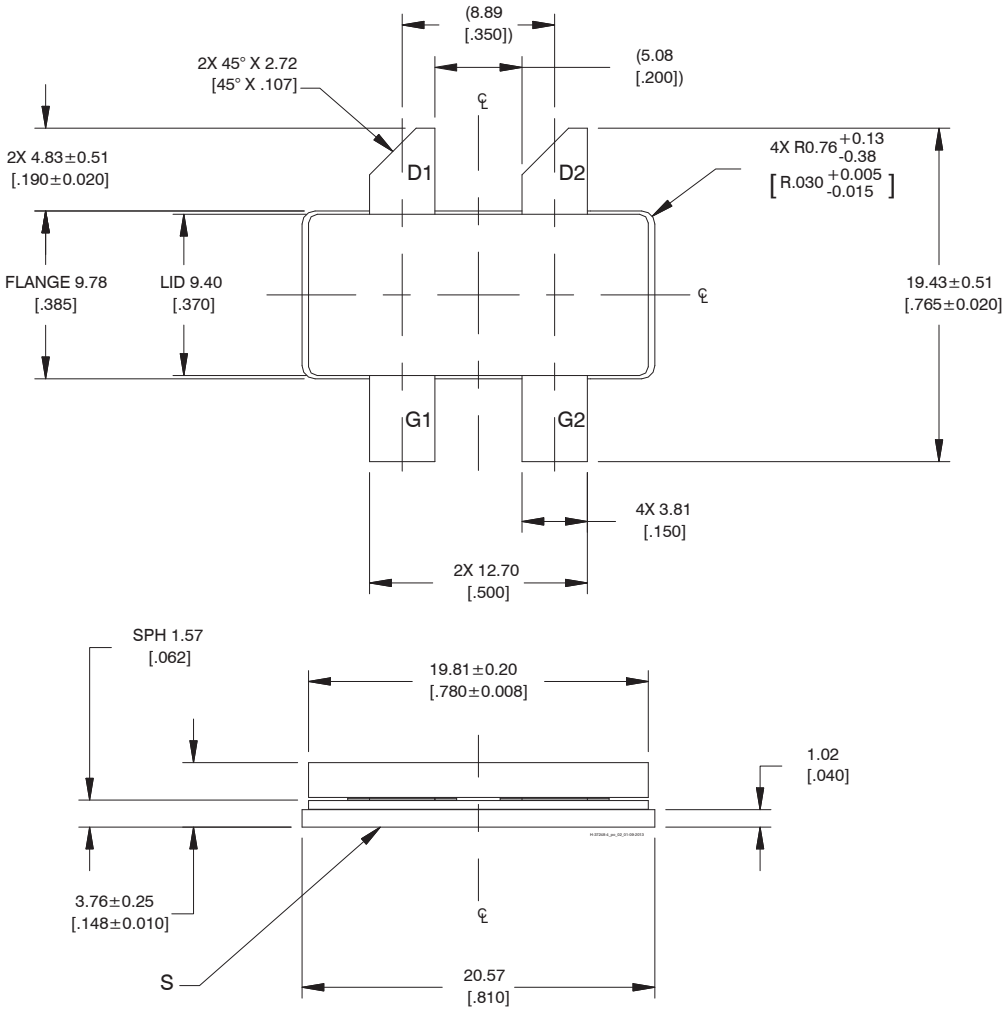


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994
2. Primary dimensions are mm, alternate dimensions are inches
3. All tolerances ± 0.127 [0.005]
4. Pins: D1, D2 – drain, G1, G2 – gate, S – source (flange)
5. Lead thickness: 0.10 +0.076/–0.025 mm [0.004 + 0.002/–0.001 inch]
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch]

Revision History

01	2015-06-08	Advance	All	First Data Sheet for this released product.
02	2015-10-27	Production	All	Updated and firm specifications for released product.
02.1	2016-02-11	Production	All	Updated Order Code and Reference Circuit MHz
03	2018-06-29	Production	All	Converted to Wolfspeed Data Sheet

For more information, please contact:

4600 Silicon Drive
Durham, North Carolina, USA 27703
www.wolfspeed.com/RF

Sales Contact
RFSales@wolfspeed.com

RF Product Marketing Contact
RFMarketing@wolfspeed.com
919.407.7816

Notes

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