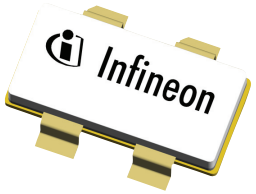
green Product

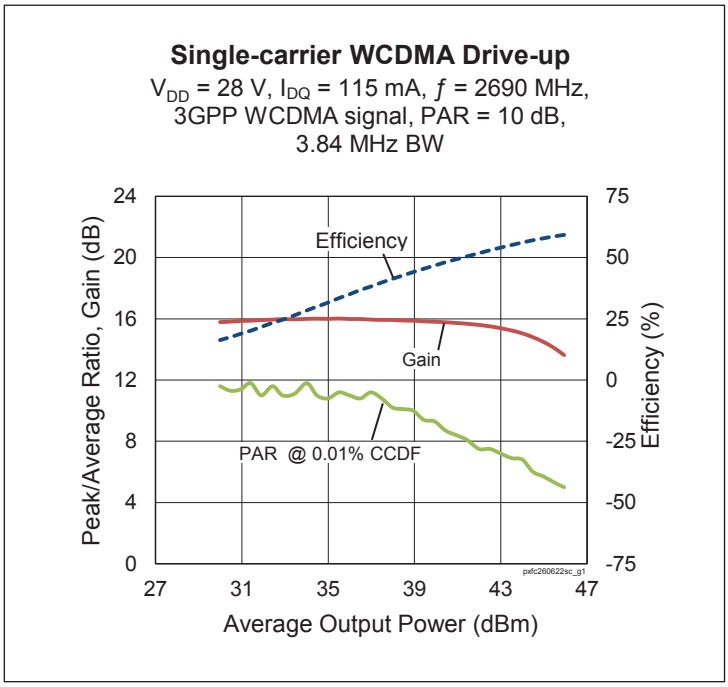
Thermally-Enhanced High Power RF LDMOS FET
75 W, 28 V, 2496 – 2690 MHz

Description

The PXAC260622SC is a 75-watt LDMOS FET with an asymetric design for use in multi-standard cellular power amplifier applications in the 2496 to 2690 MHz frequency band. It features dual-path design, input and output matching, and a thermally-enhanced, surface-mount package with earless flange. Manufactured with Infineon's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.

PXAC260622SC
Package H-37248H-4
with formed leads





Features

- Broadband internal input and output matching
- Asymmetrical Doherty design
  - Main: 25 W Typ (P_{1dB})
  - Peak: 50 W Typ (P_{1dB})
- Typical pulsed performance in a Doherty configuration, at 39.5 dB P_{OUT}, 2690 MHz, 28 V, with pulse 10 µs, 10% DC
  - Gain = 16dB
  - Efficiency = 45%
- Integrated ESD protection
- Pb-free and RoHS compliant
- Capable of handling 10:1 VSWR @28 V, 50 W (CW) output power

RF Characteristics

Single-carrier WCDMA Specifications (device tested in Infineon Doherty test fixture with straight leads)
V_{DD} = 28 V, I_{DQ} = 115 mA, P_{OUT} = 8.9 W avg, f_1 = 2690 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	14.5	15.8	—	dB
Drain Efficiency	η_D	40	42	—	%
Adjancent Channel Power Ratio	ACPR	—	–30	–27	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics

Characteristic		Conditions	Symbol	Min	Typ	Max	Unit
Drain-source Breakdown Voltage		V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current		V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1	µA
		V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10	µA
Gate Leakage Current		V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA
On-state Resistance	(main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.50	—	Ω
	(peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.25	—	Ω
Operating Gate Voltage	(main)	V_{DS} = 28 V, I_{DQ} = 115 mA	V_{GS}	2.0	2.6	3.0	V
	(peak)	V_{DS} = 28 V, I_{DQ} = 0 A	V_{GS}	—	1.4	—	V

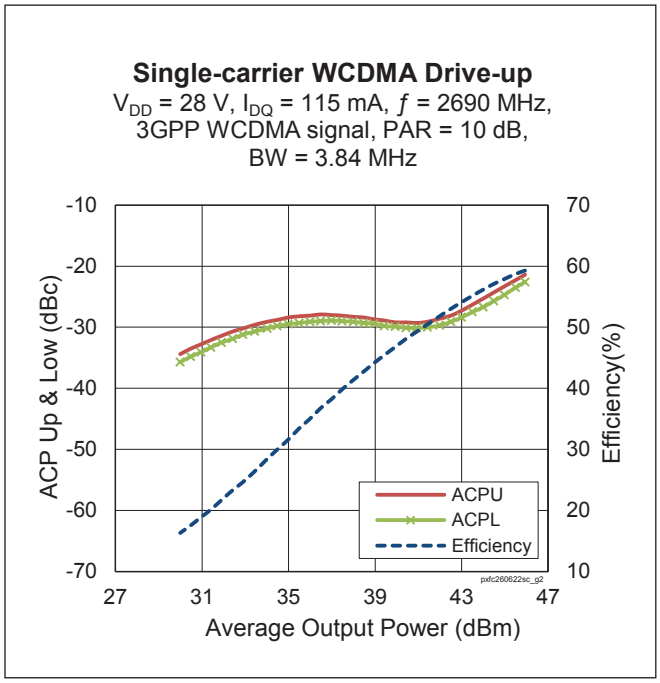
Maximum Ratings

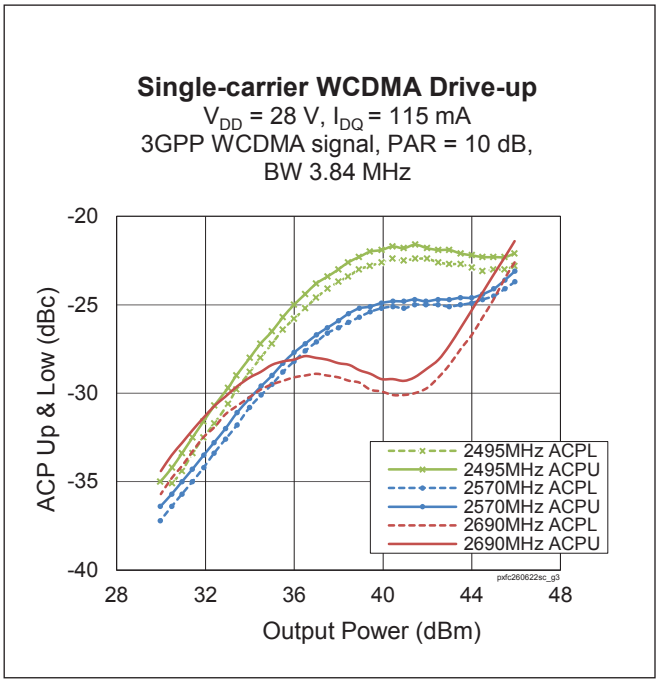
Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	65	V
Gate-source Voltage	V_{GS}	–6 to +10	V
Operating Voltage	V_{DD}	0 to +32	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C
Thermal Resistance (main, T_{CASE} = 70°C, 55 W CW)	$R_{\theta JC}$	0.962	°C/W
Thermal Resistance (peak, T_{CASE} = 70°C, 55 W CW)	$R_{\theta JC}$	0.499	°C/W

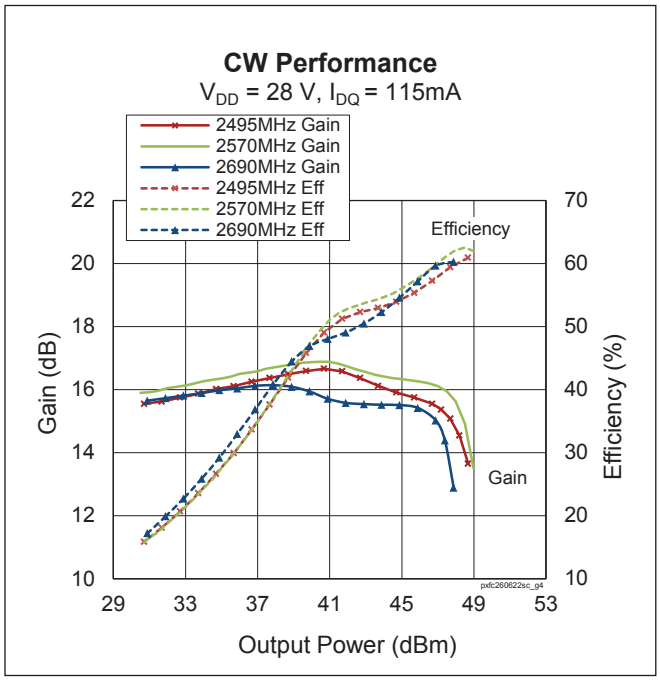
Ordering Information

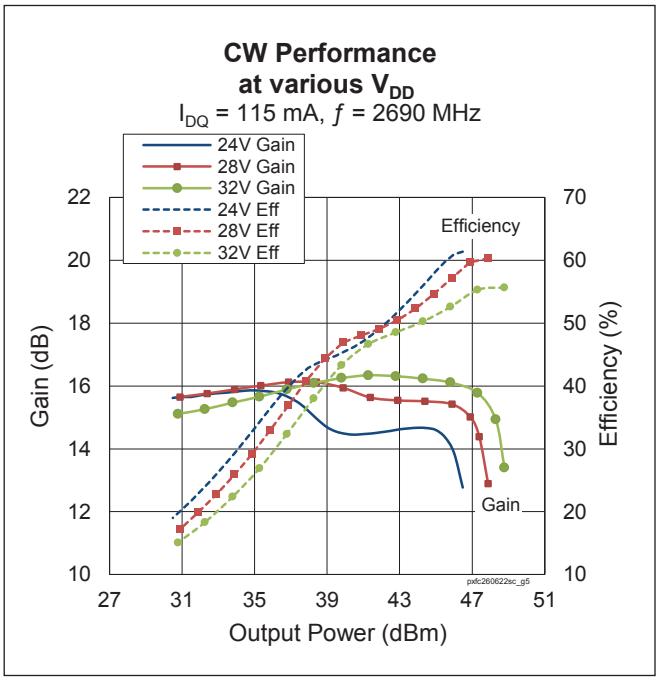
Type and Version	Order Code	Package Description	Shipping
PXAC260622SC V1 R250	PXAC260622SCV1R250XTMA1	H-37248H-4, earless flange	Tape & Reel, 250 pcs

Typical Performance (data taken in a production test fixture)

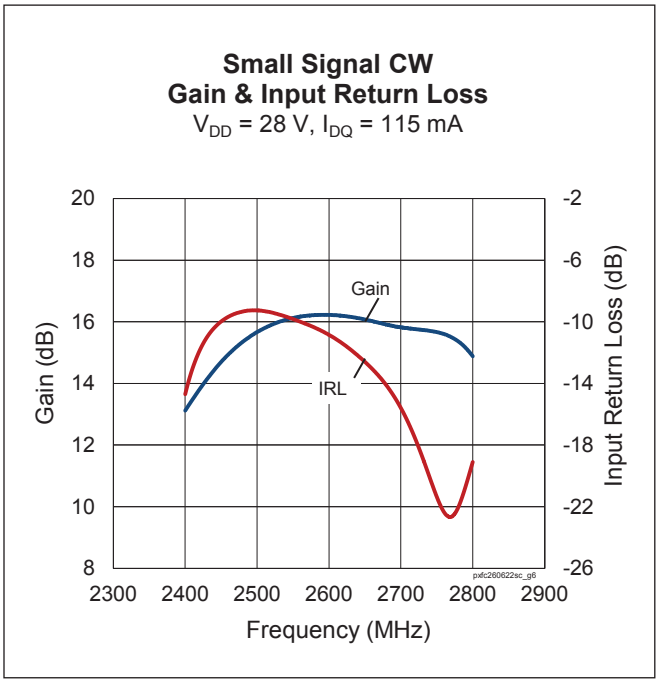








Typical Performance (cont.)



Load Pull Performance

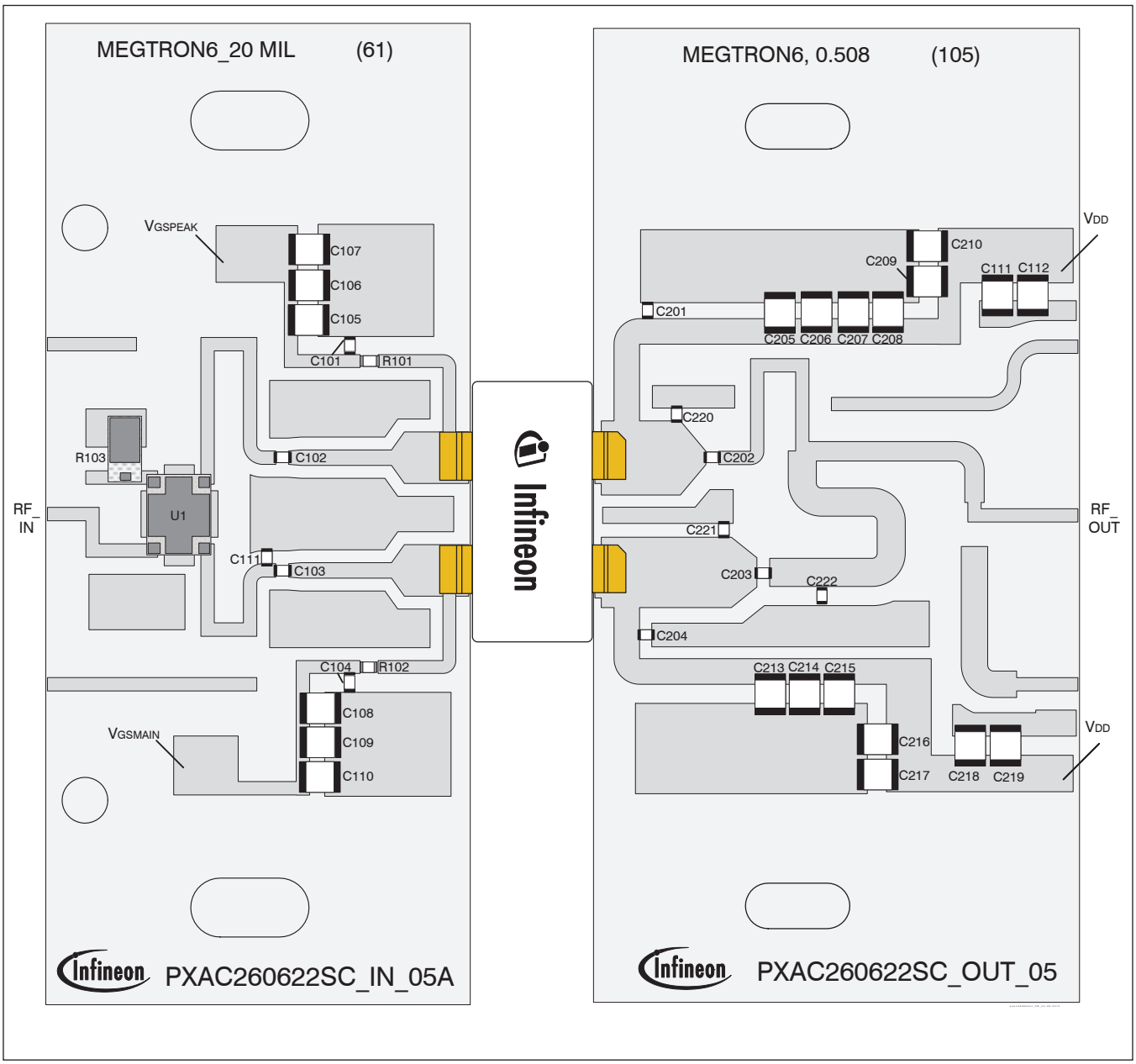
Main Side Load Pull Performance – Pulsed CW signal: 10 µs, 10% duty cycle, 28 V, I_{DQ} = 115 mA

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
2496	16.4 – j12.3	9.8 – j12.0	19.8	44.3	27.1	55.1	10.9 – j5.9	21.6	43.2	20.8	61.3
2570	18.0 – j11.1	8.9 – j11.8	19.4	44.3	26.7	54.1	9.5 – j6.0	21.4	43.0	20.0	60.4
2690	18.3 – j 0.1	10.1 – j13.5	19.2	44.4	27.8	56.0	8.0 – j8.4	20.9	43.3	21.4	61.5

Peak Side Load Pull Performance – Pulsed CW signal: 10 µs, 10% duty cycle, 28 V, V_{GSPEAK} = 1.4 V , I_{DQ} = 115 mA

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
2495	17.6 – j14.7	5.3 – j11.1	14.7	47.7	59	59.4	7.8 – j7.1	15.6	46.2	42	67.6
2570	19.7 – j11.1	6.2 – j13.2	15.5	47.4	55	56.8	7.0 – j7.4	15.6	45.7	37	65.5
2690	19.0 – j0.5	6.1 – j15.1	14.1	47.4	55	57.8	6.2 – j10.5	15.1	45.9	38	64.8

Reference Circuit , 2496 – 2690 MHz



Reference circuit assembly diagram (not to scale)

Reference Circuit (cont.)

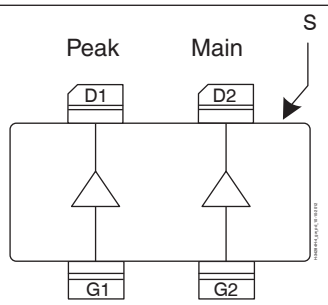
Reference Circuit Assembly

DUT	PXAC260622SC V1
Test Fixture Part No.	LTA/PXAC260062SC V1
PCB	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, ε_r = 3.66, f = 2496 – 2690 MHz
Find Gerber files for this test fixture on the Infineon Web site at http://www.infineon.com/rfpower	

Components Information

Component	Description	Manufacturer	P/N
Input			
C101, C102, C103, C104	Capacitor, 8.2 pF	ATC	ATC800A8R2JW150XB
C105, C106, C107, C108, C109, C110	Capacitor, 4.7 µF	Murata Electronics North America	GRM32ER71H475KA88L
C111	Capacitor, 0.5 pF	ATC	ATC800A0R5CW150XB
R101, R102	Resistor, 10 Ω	Panasonic Electronic Components	ERJ-3GEYJ100V
R103	Resistor, 50 Ω	Richardson	C16A50Z4
U1	Hybrid Coupler	Anaren	X3C25P1-04S
Output			
C201, C202, C203, C204	Capacitor, 8.2 pF	ATC	ATC800A8R2JW150XB
C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219	Capacitor, 4.7 µF	Murata Electronics North America	GRM32ER71H475KA88L
C220	Capacitor, 1.5 pF	ATC	ATC800A1R5CW150XB
C221	Capacitor, 1.0 pF	ATC	ATC800A1R0CW150XB
C222	Capacitor, 0.6 pF	ATC	ATC800A0R6CW150XB

Pinout Diagram (top view)



Pin Description
D1 Drain device 1 (Peak)
D2 Drain device 2 (Main)
G1 Gate device 1 (Peak)
G2 Gate device 2 (Main)
S Source (flange)

Lead connections for PXAC260622SC

Package Outline Specifications

Package H-37248H-4 with Formed Leads

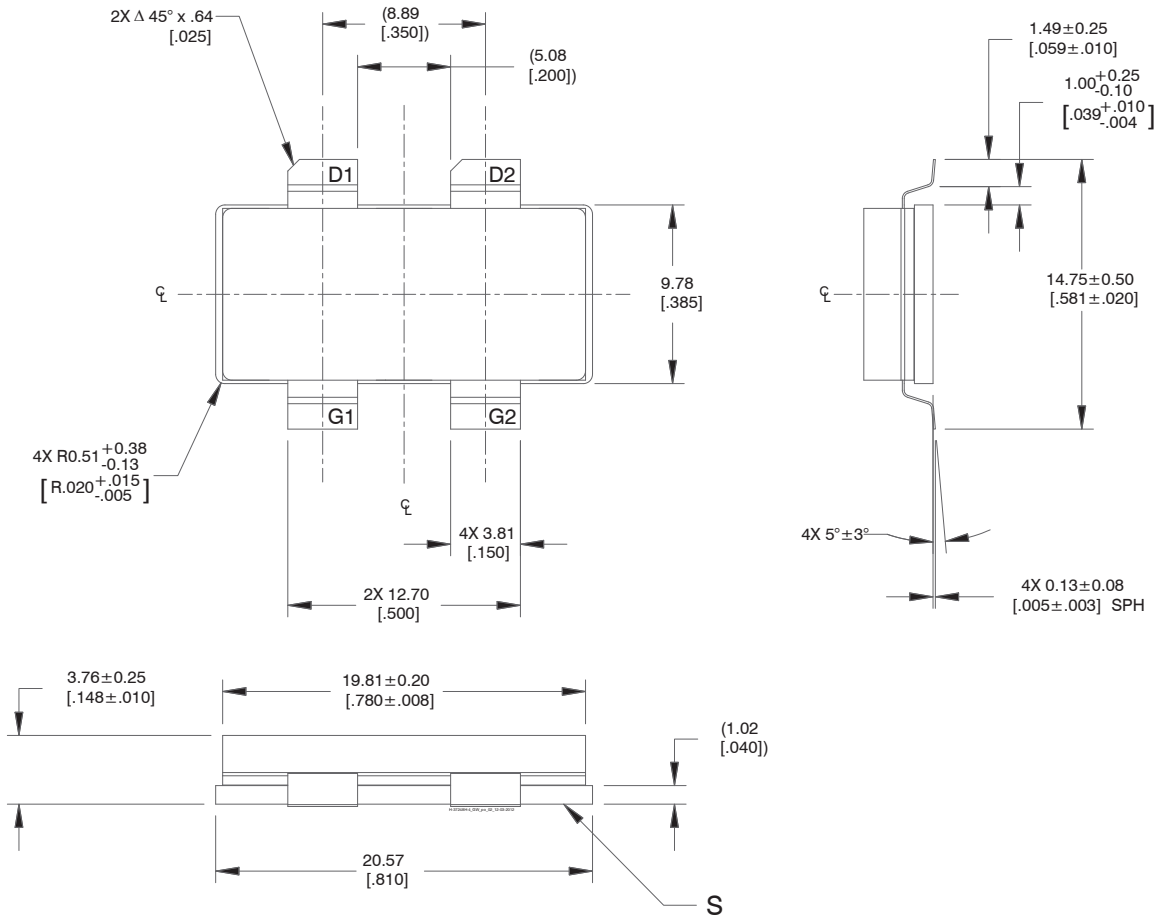


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: D1, D2 – drains; G1, G2 – gates; S – source.
5. Lead thickness: 0.10 + 0.051/-0.025 mm [.004 +0.002/-0.001 inch].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

Find the latest and most complete information about products and packaging at the Infineon Internet page http://www.infineon.com/rfpower

Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2014-04-03	Advance	All	Data Sheet reflects advance specification for product development
02	2015-04-06	Production	All All	Data Sheet reflects released product specification Revised all data and includes updated final specs, typical performance graphs, loadpull, reference circuit, package outline
02.1	2015-06-03	Production	1	Updated single-carrier WCDMA test spec

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