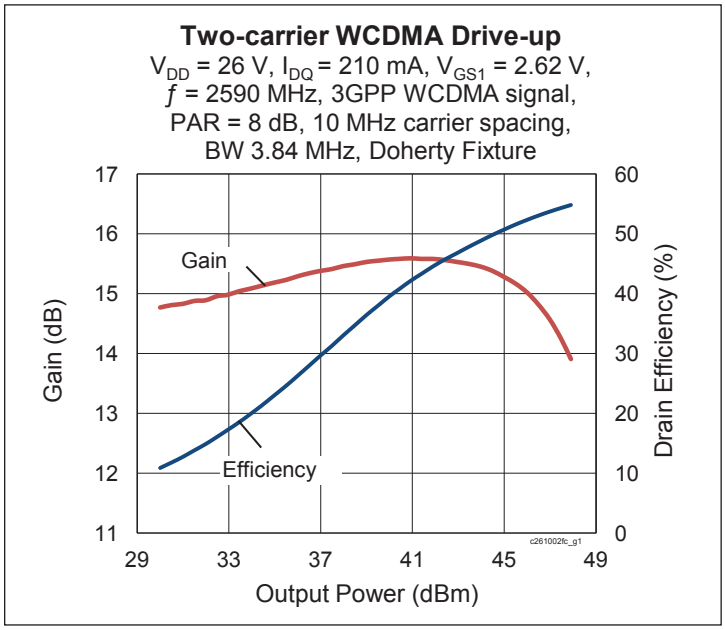
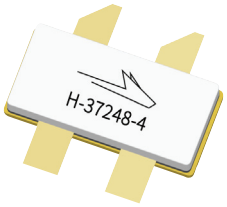
PXAC261002FC

Thermally-Enhanced High Power RF LDMOS FET
100 W, 28 V, 2490 – 2690 MHz

Description

The PXAC261002FC is a 100-watt LDMOS FET with an asymmetric design intended for use in multi-standard cellular power amplifier applications in the 2496 to 2690 MHz frequency band. Features include dual-path design, high gain and a thermally-enhanced package with earless flanges. Manufactured with Wolfspeed's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.





PXAC261002FC
Package H-37248-4

Features

- Broadband internal input and output matching
- Asymmetric design
  - Main: P1dB = 40 W Typ
  - Peak: P1dB = 70 W Typ
- Typical Pulsed CW performance, 2590 MHz, 26 V, 160 µs, 10% duty cycle, Doherty Configuration
  - Output power at P_{1dB} = 46.5 dBm
  - Output power at P_{3dB} = 50.1 dBm
- Capable of handling 10:1 VSWR @28 V, 100 W (CW) output power
- Integrated ESD protection : Human Body Model, Class 1C (per JESD22-A114)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Two-carrier WCDMA Specifications (tested in Wolfspeed production Doherty test fixture)
V_{DD} = 26 V, I_{DQ} = 210 mA, P_{OUT} = 18 W avg, V_{GS2} = 1.4 V, f_1 = 2550 MHz, f_2 = 2590 MHz, 3GPP signal, 3.84 MHz channel bandwidth, 8 dB peak/average @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	14.1	15.1	—	dB
Drain Efficiency	η_D	46	49	—	%
Intermodulation Distortion	IMD	—	–22	–21	dBc
Output PAR at 0.01% probability on CCDF (one-carrier WCDMA, 2585 MHz, 10 dB PAR)	OPAR	7.5	—	—	dB

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics (each side)

Characteristic		Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage		V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current		V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1	µA
		V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10	µA
Gate Leakage Current		V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1	µA
On-State Resistance	(main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.3	—	Ω
	(peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.16	—	Ω
Operating Gate Voltage	(main)	V_{DS} = 26 V, I_{DQ} = 210 mA	V_{GS}	2.1	2.6	3.1	V
	(peak)	V_{DS} = 26 V, I_{DQ} = 0 mA	V_{GS}	0.9	1.4	1.9	V

Maximum Ratings

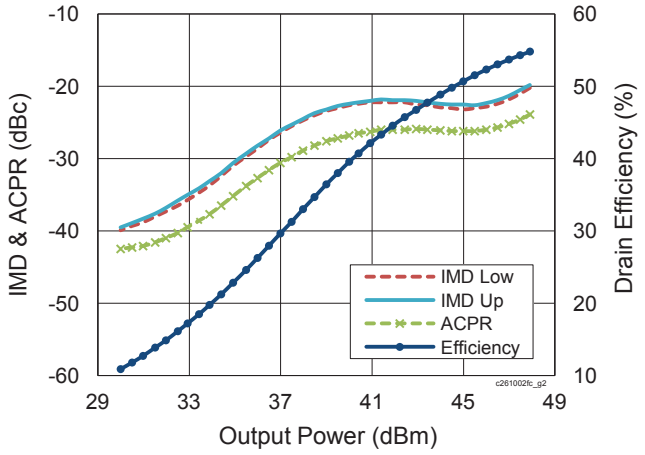
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–6 to +10	V
Operating Voltage	V_{DD}	0 to +32	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C
Thermal Resistance (Doherty, T_{CASE} = 70°C, 100 W CW)	$R_{\theta JC}$	0.6	°C/W

Ordering Information

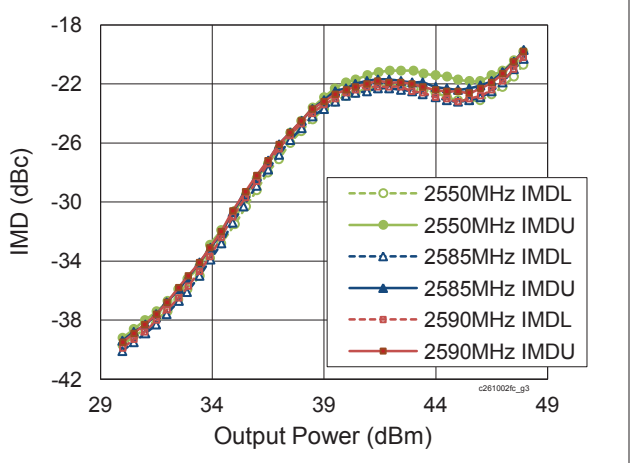
Type and Version	Order Code	Package and Description	Shipping
PXAC261002FC V1 R0	PXAC261002FC-V1-R0	H-37248-4, open-cavity, push-pull, earless flange	Tape & Reel, 50 pcs
PXAC261002FC V1 R250	PXAC261002FC-V1-R250	H-37248-4, earless flange push-pull, earless flange	Tape & Reel, 250 pcs

Typical Performance (data taken in a production Doherty test fixture)

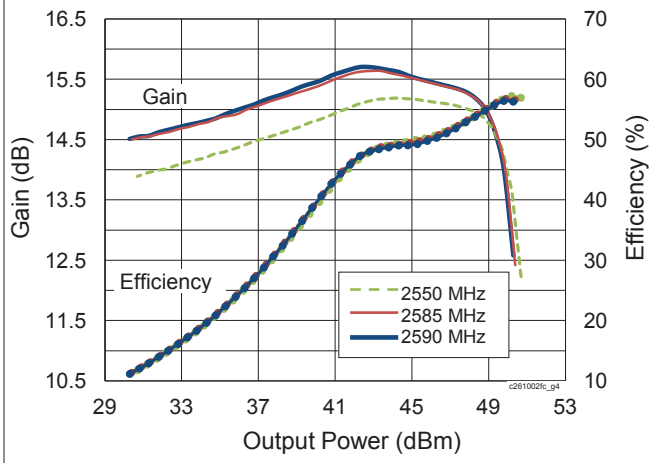
Two-carrier WCDMA Drive-up
V_{DD} = 26 V, I_{DQ} = 210 mA, V_{GS1} = 2.62 V,
f = 2590 MHz, 3GPP WCDMA signal,
PAR = 8 dB, 10 MHz carrier spacing,
BW 3.84 MHz



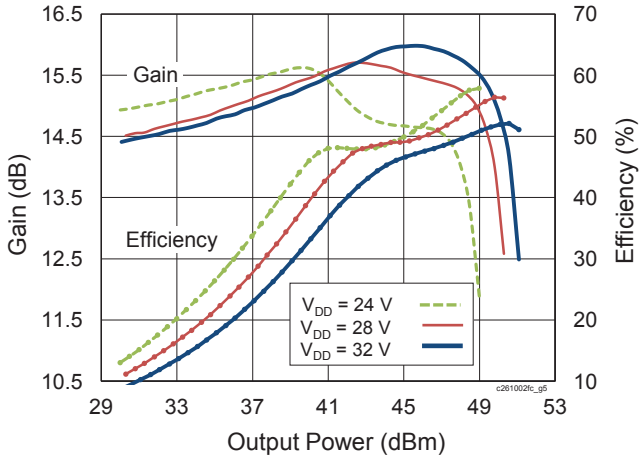
Two-carrier WCDMA Drive-up
V_{DD} = 26 V, I_{DQ} = 210 mA, V_{GS1} = 2.62 V,
3GPP WCDMA signal, PAR = 8 dB,
10 MHz carrier spacing, BW 3.84 MHz



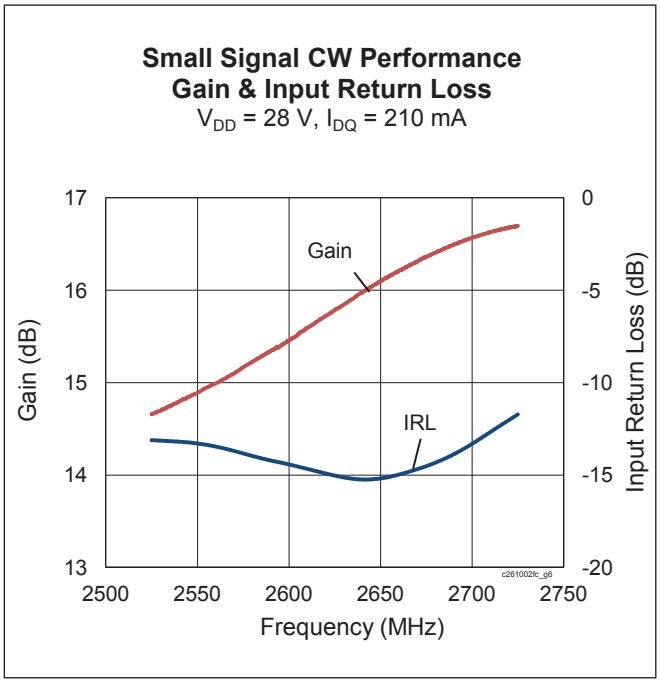
Power Sweep, CW
V_{DD} = 26 V, I_{DQ} = 210 mA, V_{GS1} = 2.62 V



CW Performance
at various V_{DD}
I_{DQ} = 210 mA, f = 2590 MHz



Typical Performance (cont.)



Load Pull Performance

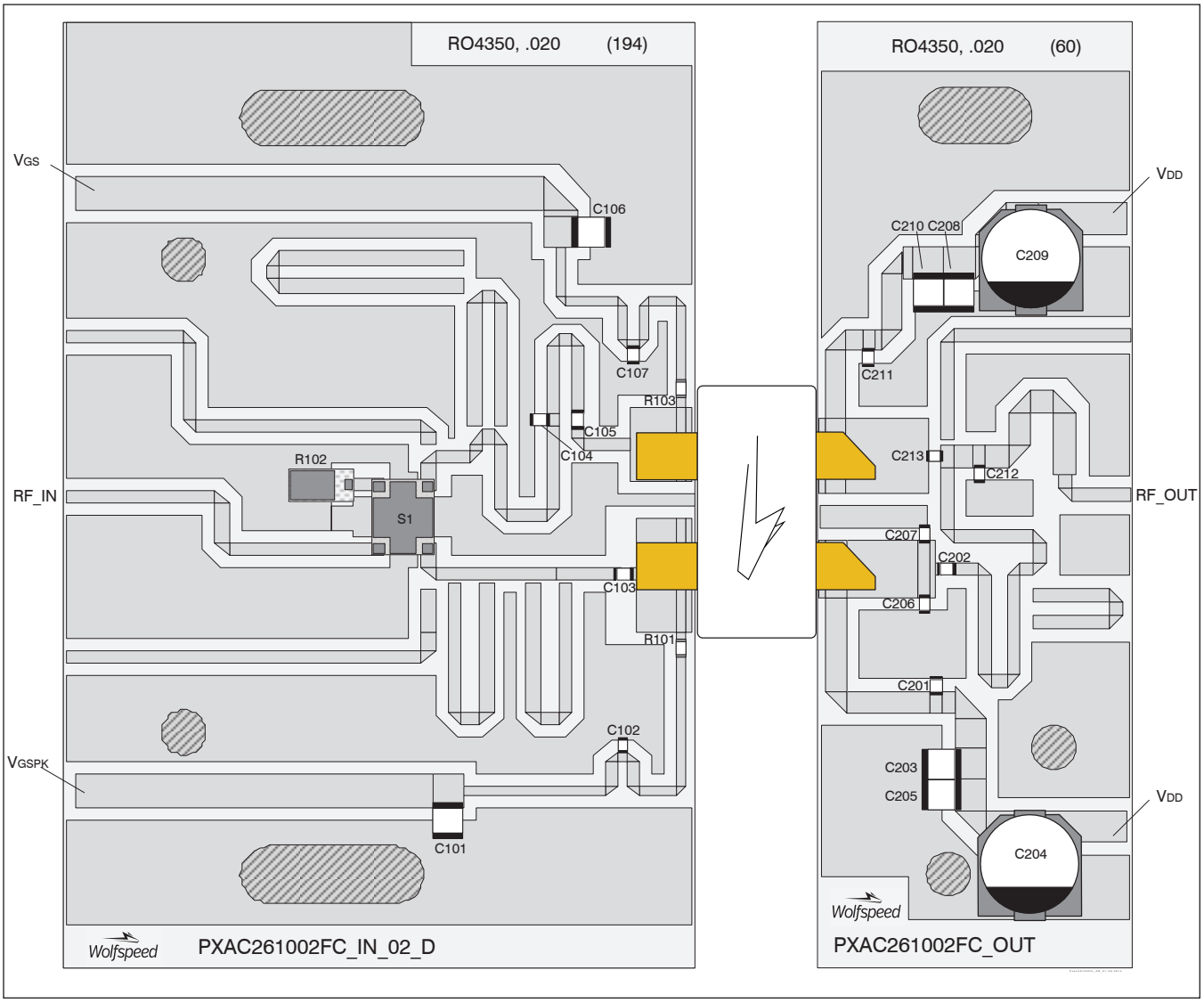
Main Side Load Pull Performance – Pulsed CW signal: 160 µs, 10% duty cycle, V_{DD} = 28 V, I_{DQ} = 240 mA

		P_{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
2540	13.3 – j23.8	5.7 – j10.9	16.8	46.58	45	50.3	10.9 – j7.1	19.1	45.1	32	59.5
2590	16.5 – j22.0	5.9 – j11.5	16.7	46.44	44	50.3	9.7 – j7.6	18.7	45.3	34	58.5
2640	21 – j24.7	6.4 – j11.5	16.8	46.35	43	50.0	10 – j6.2	19.1	44.9	31	58.0

Peak Side Load Pull Performance – Pulsed CW signal: 160 µs, 10% duty cycle, 28 V, V_{GS1} = 1.4 V

		P_{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
2540	3.8-j12.1	11.8-j7.3	13.0	50	100	53.5	5.2-j5.3	14.4	48.4	69	63.4
2590	5.2-j12.8	13-j5.4	12.8	50	100	53.4	5.7-j5.6	14.2	48.5	71	62.2
2640	5.8-j13.3	14-j3.9	12.8	49.9	98	52.9	6.6-j6	14.2	48.4	69	61.0

Reference Circuit, 2545 – 2595 MHz



Reference circuit assembly diagram (not to scale)

Reference Circuit (cont.)

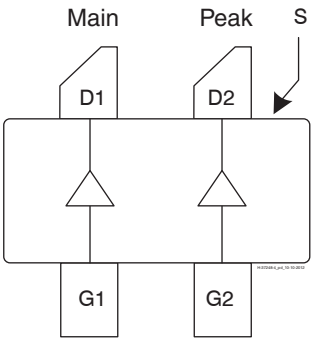
Reference Circuit Assembly

DUT	PXAC261002FC V1
Test Fixture Part No.	LTA/PXAC261002FC V1
PCB	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, ε_r = 3.66, f = 2545 – 2595 MHz
Find Gerber files for this test fixture on the Wolfspeed Web site at **http://www.wolfspeed.com/RF**	

Components Information

Component	Description	Suggested Manufacturer	P/N
Input			
C101, C106	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T
C102	Capacitor, 18 pF	ATC	ATC800A180JT250T
C103	Capacitor, 1.6 pF	ATC	ATC800A1R6CT250T
C104	Capacitor, 0.6 pF	ATC	ATC800A0R6CT250T
C105, C107	Capacitor, 12 pF	ATC	ATC800A120JT250T
R101, R103	Resistor, 10 ohm	Panasonic Electronic Components	ERJ-3GEYJ100V
R102	Resistor, 50 ohm	Anaren	C16A50Z4
S1	Hybrid coupler	Anaren	X3C26P1-03S
Output			
C201, C202	Capacitor, 12 pF	ATC	ATC800A120KT250T
C203, C205, C208, C210	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T
C204, C209	Capacitor, 220 µF	Panasonic Electronic Components	EEE-FP1V221A
C206	Capacitor, 0.5 pF	ATC	ATC800A0R5CT250T
C207	Capacitor, 0.6 pF	ATC	ATC800A0R6CT250T
C211	Capacitor, 12 pF	ATC	ATC800A120JT250T
C212	Capacitor, 0.4 pF	ATC	ATC800A0R4CT250T
C213	Capacitor, 3.9 pF	ATC	ATC800A3R9CT250T

Pinout Diagram (top view)



Pin	Description
D1	Drain device 1 (Main)
D2	Drain device 2 (Peak)
G1	Gate device 1 (Main)
G2	Gate device 2 (Peak)
S	Source (flange)

Lead connections for PXAC261002FC

Package Outline Specifications

Package H-37248-4

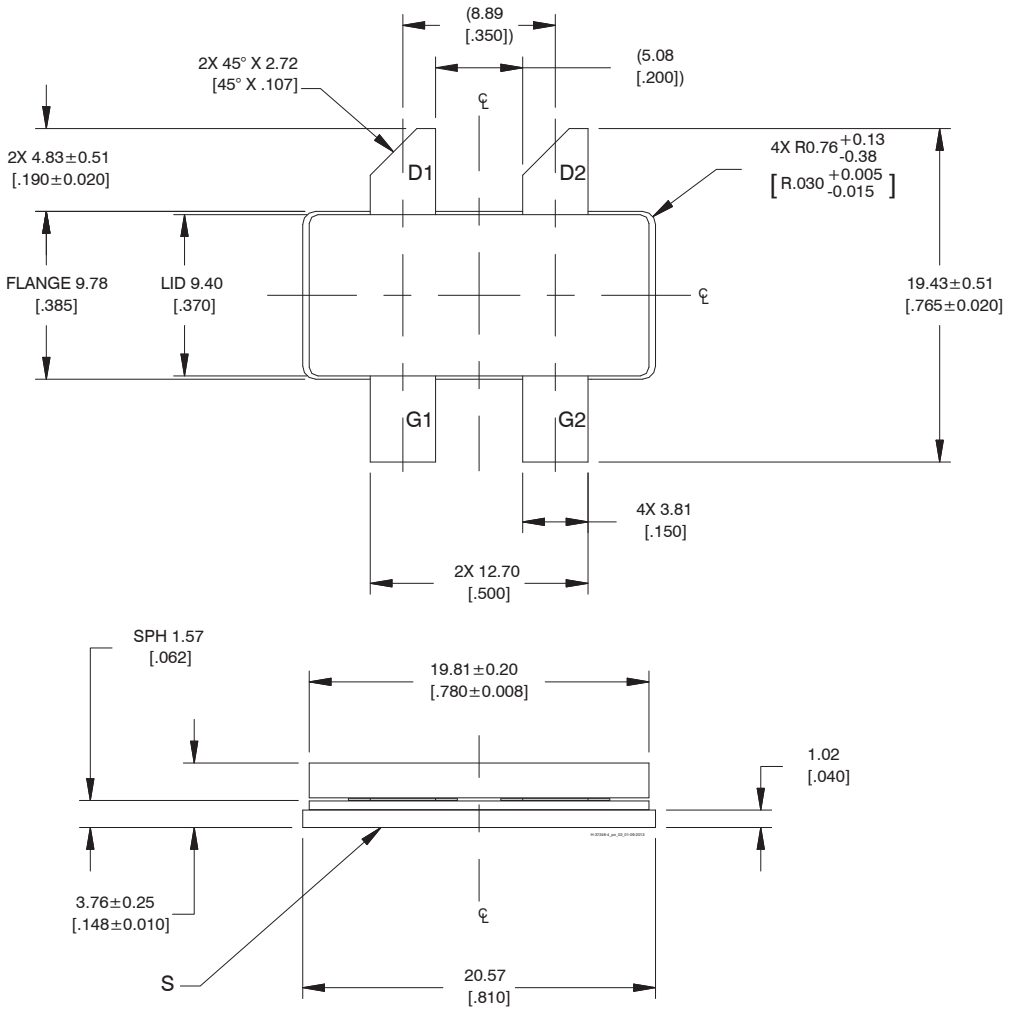


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: D1, D2 – drains; G1, G2 – gates; S – source.
5. Lead thickness: 0.10 + 0.076/–0.025 mm [0.004+0.003/–0.001 inch].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2013-11-01	Advance	All	Data Sheet reflects advance specification for product development
02	2014-01-28	Production	All All	Data Sheet reflects released product specification Revised all data and includes final specs, typical performance graphs, loadpull, reference circuit
03	2014-03-26	Production	1	Corrected frequency range. Removed "doherty" from second feature. Updated feature 2.
03.1	2014-04-04	Production	1	Removed bullet point 4 (extra lines) from Features section.
03.2	2016-06-07	Production	1	Added OPAR to RF table.
03.3	2016-06-15	Production	1	Adjust OPAR information.
04	2018-07-03	Production	All	Converted to Wolfspeed Data Sheet.

For more information, please contact:

4600 Silicon Drive
Durham, North Carolina, USA 27703
www.wolfspeed.com/RF

Sales Contact
RFSales@wolfspeed.com

RF Product Marketing Contact
RFMarketing@wolfspeed.com
919.407.7816

Notes

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