



PY32F403 Datasheet

32-bit ARM® Cortex-M4F Microcontroller



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Features

- Cores and Systems
 - 32-bit ARM® Cortex-M4F processor core with FPU and DSP instruction support
 - Typical operating frequency up to 144 MHz
- Memory
 - Up to 384 KB of flash program memory
 - Up to 64 KB of SRAM
- Clock, reset and power management
 - 1.8 V ~ 3.6 V supply
 - Power-on/power-off reset (POR/PDR), programmable voltage monitor (PVD)
 - External 4 ~ 32 MHz high-speed crystal oscillator
 - Built-in factory-tuned 8 MHz high-speed oscillator
 - PLL supports CPU operation at up to 144 MHz
 - External 32.768 kHz low-speed oscillator
- Low power consumption
 - Sleep, shutdown and standby modes
 - V_{BAT} to power RTC and back-up registers
- 3 x 12-bit analogue-to-digital converters, 1 μ s conversion time (up to 18 input channels)
 - Conversion range: 0 ~ V_{CCA}
 - Support for sample time and resolution configuration
 - Supports single, continuous, sweep and discontinuous conversion modes
 - On-chip temperature sensor
 - On-chip voltage sensor
- 2 x 12-bit digital-to-analog converters
 - Output range: 0 ~ V_{REF+}
 - Independent output channels
 - Support Timer, EXTI triggering
- 12 - channel DMA controller
 - Supported peripherals: Timer, ADC, UART, I²C, I2S, SPI, SDIO
- Up to 80 fast I/O ports:
 - All I/O ports can be imaged to 16 external interrupts
 - Some ports support 5 V input
- Debug modes
 - Serial single wire debug (SWD) or JTAG interface
- Up to 17 timers
 - 2 x 16-bit advanced control timers with 4 channels of PWM outputs, as well as deadband generation and emergency stop functions
 - 10 16-bit general purpose timers with up to 4 independent channels for input capture/output comparison, the general purpose timers also support an encoder interface for two inputs using a quadrature decoder
 - 2 x 16-bit basic timers
 - 2 watchdog timers (standalone and windowed)
 - System time timer: 24-bit self-subtracting counter
- Up to 13 communication interfaces
 - 5 UART interfaces
 - 2 I²C interfaces
 - 3 SPI interfaces
 - 1 ESMC interface
 - 1 CANFD interface
 - 1 USB interface
 - 1 SDIO interface
- 96-bit unique chip ID (UID)
- In LQFP100, LQFP64, LQFP48, QFN48, QFN32(4*4) packages

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1. Introduction

The PY32F403 series microcontrollers are high performance 32-bit ARM® Cortex®-M4F core MCUs with up to 384 KB Flash and 64 KB SRAM memory and a maximum operating frequency of 144 MHz. Multiple I²C, SPI and USART communication peripherals, 3 x 12-bit ADCs, 17 timers, 1 x USB 2.0 and 1 x CANFD are integrated.

The PY32F403 series microcontrollers are available in the operating temperature range of - 40 °C to 85 °C and the operating voltage range of 1.8 V to 3.6 V. The chips provide Sleep, Stop and Standby low power modes to meet different low power applications.

The PY32F403 series microcontrollers are suitable for a wide range of applications such as controllers, handheld devices, PC peripherals, gaming and GPS platforms, industrial applications, etc.

Table 1-1 PY32F403 series planning and features

| Peripherals | | PY32F403 V1DT | PY32F403 R1DT | PY32F403 R2DT | PY32F403 R1CT | PY32F403 C1BT | PY32F403 C1CT | PY32F403 C1DT | PY32F403 C2DT | PY32F403 C1CU | PY32F403 K1BU | PY32F403 K1CU | |
|-----------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|--|
| Flash (KB) | | 384 | 384 | 384 | 256 | 128 | 256 | 384 | 384 | 256 | 128 | 256 | |
| SRAM (KB) | | 64 | 64 | 64 | 64 | 64 | 64 | 64 | 64 | 64 | 32 | 64 | |
| Timers | General timer | | | | | | | 10 | | | | | |
| | Advanced timer | | | | | | | 2 | | | | | |
| | SysTick | | | | | | | 1 | | | | | |
| | Basic timer | | | | | | | 2 | | | | | |
| | Watch dog | | | | | | | 2 | | | | | |
| Communication Port | USART | 5 | 5 | 5 | 5 | 3 | 3 | 3 | 3 | 2 | 2 | 2 | |
| | I ² C | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 1 | 1 | 1 | |
| | SPI | 3 | 3 | 2 | 3 | 3 | 3 | 3 | 3 | 3 | 2 | 2 | |
| | I2S | 3 | 2 | 3 | 2 | 1 | 1 | 1 | 3 | 1 | 1 | 1 | |
| | CANFD | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | - | - | |
| | USB D | | | | | | | 1 | | | | | |
| | SDIO | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | - | - | |
| DMA | | | | | | | | 12ch | | | | | |
| RTC | | | | | | | | Yes | | | | | |
| GPIO | | 80 | 51 | 49 | 51 | 37 | 37 | 37 | 37 | 41 | 26 | 26 | |
| ESMC | | | | | | | | 1 | | | | | |
| EXTI | | | | | | | | 16 | | | | | |
| ADC (Channels) | | 3 (16) | 3 (16) | 3 (16) | 3 (16) | 3 (10) | 3 (10) | 3 (10) | 3 (10) | 3 (11) | 3 (10) | 3 (10) | |
| Operating Voltage | | | | | | | | 1.8 ~ 3.6 V | | | | | |
| Max. CPU frequency | | | | | | | | 144 MHz | | | | | |
| Operating Temperature | | | | | | | | - 40 ~ 85 C° | | | | | |
| Package | | LQFP100 | | LQFP64 | | | LQFP48 | | | QFN48 | | QFN32 | |

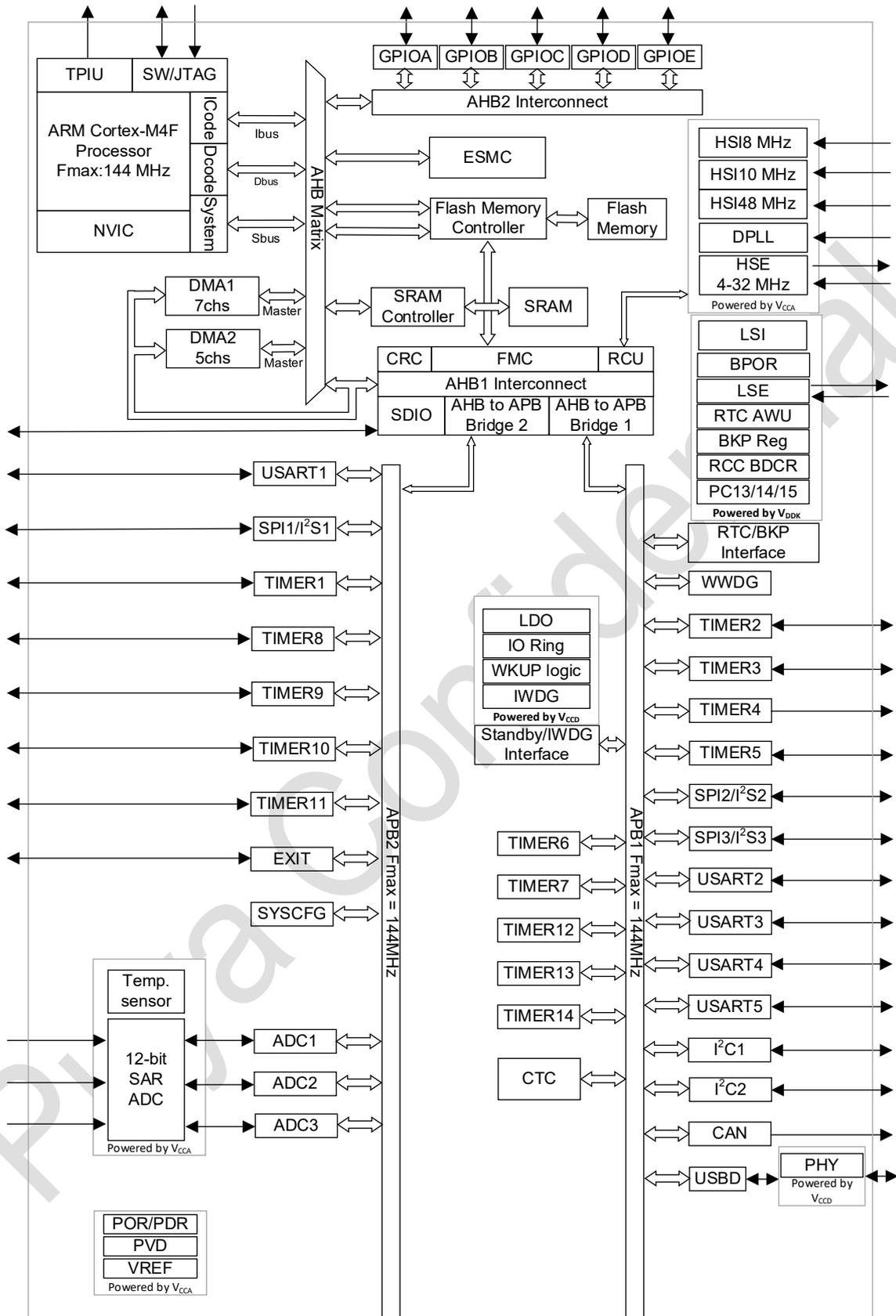


Figure 1-1 Functional modules

2. Functional overview

2.1. Arm® Cortex®-M4F processor

ARM®'s Cortex®-M4F processor is a high performance embedded 32-bit RISC processor supporting DSP instructions and FPU floating point operations, offering excellent code efficiency and the high performance of the ARM core using the memory space normally available in 8 and 16-bit devices. The processor supports a set of DSP instructions that enable efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) accelerates development and prevents saturation through the use of meta-language development tools. Provides a low cost platform for MCUs, low pin count, low power consumption, while providing excellent computational performance and advanced interrupt system response. Compatible with all ARM tools and software.

Cortex®-M4F processor for 32-bit ARM®

- supports 144 MHz operation
- single-cycle multiplier and hardware divider
- Integrated DSP instructions
- Nested interrupt vector control
- 24-bit system tick timer

The ARM® Cortex®-M4F processor is based on the ARMv7-M architecture and supports the Thumb and Thumb-2 instruction sets.

- Internal bus matrix connecting the I-Code bus, D-Code bus, system bus, private peripheral bus (PPB) and debug access (AHB-AP)
- Nested Vector Interrupt Controller (NVIC)
- Flash Patches and Breakpoints (FPB)
- Data Watchpoint and Trace (DWT)
- Instrumentation Trace Macrocell (ITM)
- Serial Line JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)
- Floating Point Unit (FPU)
- Memory Protection Unit (MPU)

2.2. Memories

The on-chip SRAM is accessible by bytes (8 bits), half - word (16 bits) or word (32 bits).

The on-chip Flash is integrated and consists of two different physical areas:

- Main flash area, which contains application and user data
- Information area, 24 KB, which contains the following sections:
 - Option bytes

- UID bytes
- System memory

The protection of the Flash main memory consists of the following mechanisms:

- Read protection (RDP) to prevent access from outside.
- Write protection (WRP) control, to prevent unwanted write operations (due to confusion of the program memory pointer PC). The minimum protection unit for write protection is 8 KB.
- Option byte write protection, specially designed for unlocking.

2.3. Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage CPU access to memory and to prevent one task from accidentally damaging memory or resources used by another active task. This memory area is organized into up to 8 protected areas, which can also be subdivided into up to 8 sub areas in turn. The size of the protected area can be from 32 bytes up to the entire 4G bytes of addressable memory. The MPU is particularly useful if there is critical or certified code in the application that must be protected from the misbehavior of other tasks. It is usually managed by a real time operating system (RTOS). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the settings of the MPU area based on the executing process. the MPU is optional and can be bypassed if not required by the application.

2.4. Flash accelerator (ACC)

In order to exploit the full performance of the processor, the accelerator will implement instruction prefetch queues and branch caching, thereby increasing the speed of program execution in Flash. According to CoreMark benchmark tests, the performance obtained by this accelerator needs to reach the equivalent of Flash executing programs in wait cycles at CPU frequencies up to 144 MHz.

- ICODE enables instruction prefetching
- Instruction cache of 64 branches with 128-bit data width
- Data cache of 16 branches with 128-bit data width

2.5. Boot modes

With the BOOT0 pin and BOOT1 pin, three different boot modes can be selected, as shown in the following table:

Table 2-1 Boot configuration

| Boot mode configuration | | Mode |
|-------------------------|-----------|------------------------------------|
| BOOT1 Pin | BOOT0 pin | |
| X | 0 | Select Main flash as the boot area |
| 0 | 1 | Select System memory as boot area |
| 1 | 1 | Select SRAM as boot area |

The boot loader program is stored in the System memory and is used to download the Flash program via the USART and USB interface.

2.6. Backup register (BKP)

The backup registers are 42 16-bit registers that can be used to store 84 bytes of user application data. The modules are in the backup domain and when the V_{DD} power is cut, they are still maintained by V_{BAT} for power supply. They are also not reset when the system is woken up in standby mode, or when a system reset or power reset (POR) is performed.

- supports 84 bytes of data back-up registers
- Status/control register for managing anti-intrusion detection and with interrupt function
- Checksum register for storing RTC checksum values
- Outputs RTC calibration clock, RTC alarm pulses or second pulses on pin PC13 (when this pin is not used for intrusion detection)

2.7. Clock management

The default system clock frequency is HSI 8 MHz after the CPU has been booted, and the system clock frequency and system clock source can be reconfigured after the program has been run. The following high frequency clocks can be selected:

- an 8 MHz internal high precision HSI clock.
- A 40 kHz configurable internal LSI clock.
- A 4 ~ 32 MHz HSE clock, and the CSS function can be enabled to detect HSE. If CSS fails, the hardware automatically converts the system clock to HSI, the HSI frequency is configured by software, and the CPU NMI interrupt is generated.
- A 32.768 KHz LSE clock.
- PLL clock, PLL source can be selected as HSE. If HSE source is selected, when CSS is enabled and CSS fails, PLL and HSE are turned off and the hardware selects the system clock source as HSI.

The AHB clock can be divided based on the system clock and the APB clock can be divided based on the AHB clock. The AHB and APB clock frequencies are up to 144 MHz.

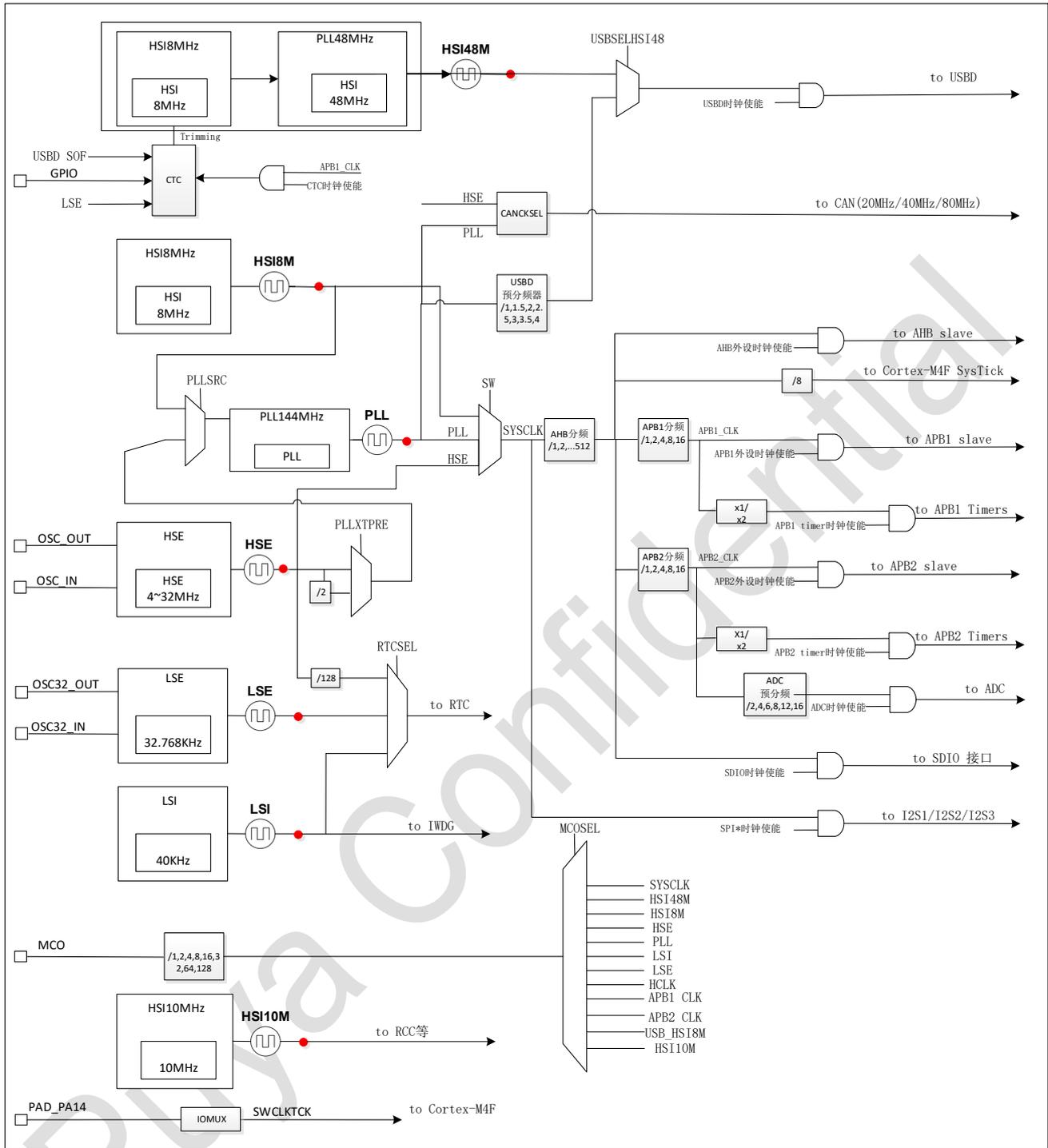


Figure 2-1 System clock structure diagram

2.8. Power management

2.8.1. Power block diagram

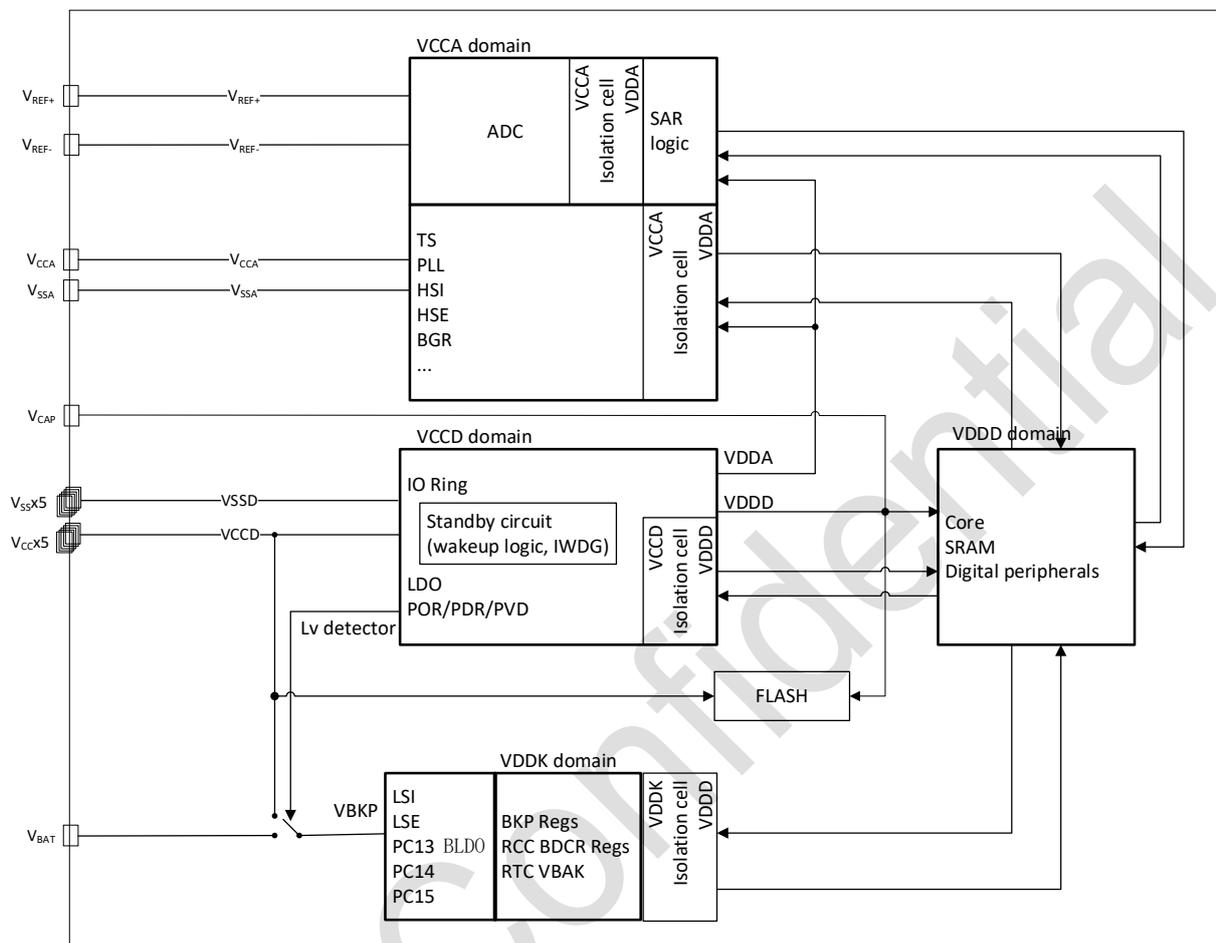


Figure 2-2 Power block diagram

Table 2-2 Power block diagram

| No. | Power supply | Power value | Description |
|-----|---------------------------------|---------------|--|
| 1 | V _{CC} | 1.8 V - 3.6 V | Power is supplied to the chip via the power pin. |
| 2 | V _{CAP} ⁽¹⁾ | 1.1 V | The output from the VR supplies power to the main logic circuits and SRAM inside the chip. When MR is powered, the output is 1.1 V. When in stop mode, the output can be powered by MR or LPR, depending on the software configuration, and the LPR output is depending on the software configuration. |
| 3 | V _{CCA} | 1.8 V - 3.6 V | The power supply pin provides power to the chip's analogue circuitry. |
| 4 | V _{BAT} | 1.65 - 3.6 V | Power is supplied for RTC and BKP register. |

1. Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} and ESR is specified in the follow table :

Table 2-3 V_{CAP} operating conditions

| Symbol | Parameters | Minimum | Maximum | Unit |
|------------------|-----------------------------------|---------|---------|------|
| C _{EXT} | Capacitance of external capacitor | 0.1 | 1 | μF |
| ESR | ESR of external capacitor | - | 0.5 | Ω |

2.8.2. Power monitoring

2.8.2.1. Power on/power off reset (POR/PDR)

The Power on reset (POR) / Power down reset (PDR) module is designed to provide a power up and power down reset for the chip. This module remains operational in all modes.

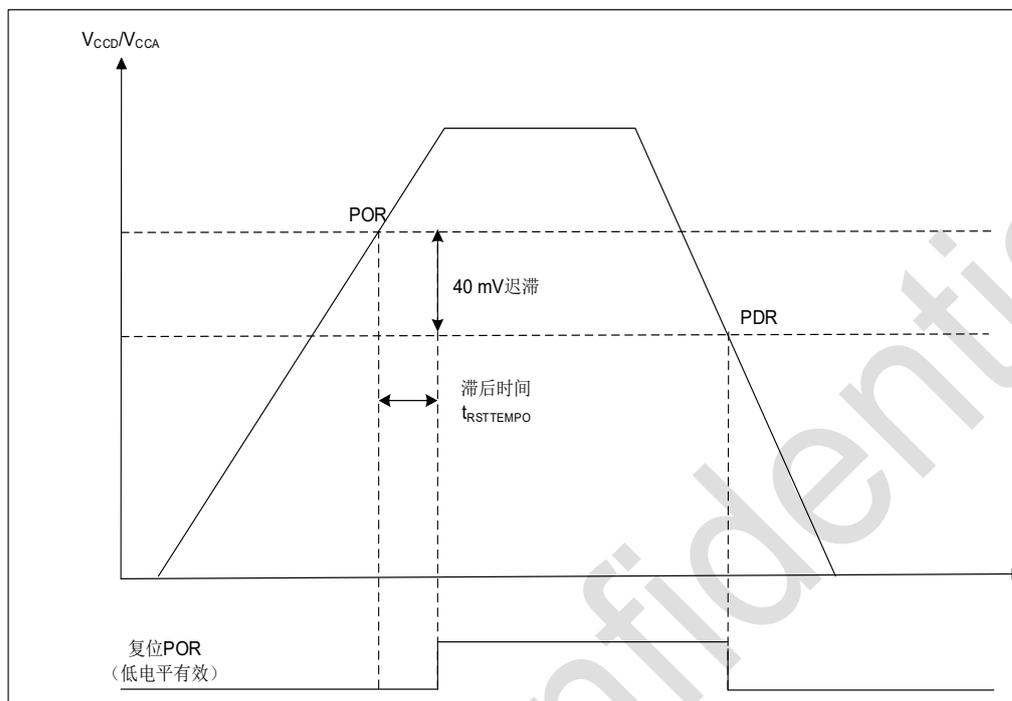


Figure 2-3 POR/PDR Threshold

2.8.2.2. Voltage detection (PVD)

The programmable voltage detector (PVD) module can be used to detect the V_{CC} supply, the detection point can be configured via a register. When V_{CC} is above or below the PVD detection point, a corresponding reset flag is generated.

The event is internally connected to EXTI line 16 and depending on the EXTI line 16 rising/falling edge configuration, an interrupt is generated when V_{CC} rises above the PVD detection point, or when V_{CC} falls below the PVD detection point.

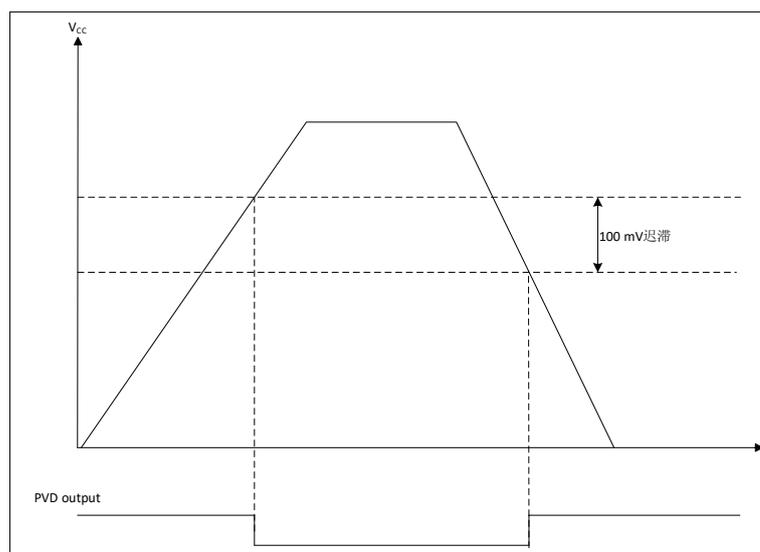


Figure 2-4 PVD threshold

2.8.3. Voltage regulator

The chip is designed with three voltage regulators:

- The main regulator (MR) remains active during the normal operating state of the chip.
- Low power regulator (LPR) provides a lower power consumption option in the stop mode.
- Off mode for CPU standby mode. (LDO output high resistance, core power cut off, registers and SRAM contents lost)

2.8.4. Low power modes

The chip has 3 low power modes in addition to the normal operating modes:

- Sleep mode: CPU clock is switched off (NVIC, SysTick, etc. work), peripherals can be configured to keep working. (It is recommended to only enable modules that have to work and to switch off the module when it has finished working)
- Stop mode: In this mode the contents of SRAM and registers are held, the high speed clocks PLL, HSI and HSE are switched off and most of the module clocks in the V_{DD} domain are disabled. GPIO, PVD and RTC can be woken up in stop mode.
- Standby mode: The chip has a V_{BAT} power supply, so when V_{CC} is powered down, the chip only works in the V_{BKP} domain. There are four conditions for exiting from standby mode: external reset on NRST, IWDG reset, RTC alarm on time, rising edge on the WKUP pin.

2.9. Reset

Three types of reset are designed into the chip: power reset, system reset and backup domain reset.

2.9.1. Power reset

The power reset is generated in the following situations:

- Power On / Power Off Reset (POR / PDR)
- When exiting Standby mode

2.9.2. System reset

A system reset is generated when the following events are generated:

- Reset of NRST pin
- Window watchdog reset (WWDG)
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load reset (OBL)

2.9.3. Backup domain reset

A backup domain reset is generated whenever one of the following events occurs:

- Software reset: Triggered by setting the BDRST bit in the RCC backup domain control register (RCC_BDCR).
- Power reset: When both V_{CC} and V_{BAT} lose power and either one is subsequently powered up again.

2.10. General purpose inputs/outputs (GPIOs)

Each GPIO can be configured by software as an output (push - pull or open drain), input (floating, pull - up / down and analog), peripheral multiplexing function, and a locking mechanism that freezes the I/O port configuration function. The GPIO functions are summarized as follows:

- register supports IO Port / AHB bus read/write
- Output status: push-pull or open-drain + pull-up/down
- Data output from data registers (GPIOx_ODR) or peripherals (multiplexed function outputs)
- Speed selectable per I/O
- Input states: float, pull-up/pull-down, analog
- Data input to input data register (GPIOx_IDR) or peripheral (multiplexed function input)
- Position bit/reset register (GPIOx_BSRR), allows bit write access to GPIOx_ODR
- Locking mechanism (GPIOx_LCKR) will freeze the I/O port configuration function
- Analog functions
- Multiplexed function selection register (up to 16 multiplexed functions per IO port)
- Highly flexible I/O multiplexer function allows I/O ports to function as GPIOs, or as various peripheral interfaces

2.11. DMA

Direct memory access (DMA) is used to provide high-speed data transfer between peripherals and memory or between memory and memory. Moving data without CPU intervention, data can be moved quickly via DMA, which saves CPU resources for other operations. The device has two general purpose dual-port DMAs (DMA1 and DMA2) with seven and five channels respectively, each dedicated to managing requests for memory access from one or more peripherals. There is also an arbiter to coordinate the priority of individual DMA requests.

The main functions are as follows:

- single AHB master

- supports peripheral to memory, memory to peripheral, memory to memory and peripheral to peripheral data transfers
- On-chip memory devices such as Flash, SRAM, AHB and APB peripherals, as source and destination
- All DMA channels can be configured independently:
 - Each channel is either associated with a DMA request signal from a peripheral or with a software trigger in a memory-to-memory transfer. This configuration is done by software.
 - The priority between requests is programmable by software (4 levels per channel: very high, high, medium, low) and in case of equality by hardware (e.g. requests for channel 1 have priority over requests for channel 2).
 - The source and destination transfer sizes are independent (byte, half-word, word), simulating packetisation and unpacketisation. Source and destination addresses must be aligned by data size.
 - Programmable number of data transfers: 0 to 65535
- Generates one interrupt request per channel. Each interrupt request is caused by any one of three DMA events: transfer complete, half-transfer or transfer error.

2.12. Interrupts and events

The PY32F403 handles exceptions via the vector interrupt controller (NVIC) and an extended interrupt/event controller (EXTI) embedded in the Cortex-M4F processor.

2.12.1. Nested vectored interrupt controller (NVIC)

The NVIC is a tightly coupled IP inside the Cortex-M4F processor, which can handle NMI (non-maskable interrupts) and maskable external interrupts from outside the processor, as well as Cortex-M4F internal exceptions.

The tight coupling of the processor core to the NVIC greatly reduces the delay between interrupt events and the start of the corresponding interrupt service routines (ISRs), which are listed in a vector table and stored at a base address in the NVIC. The vector address of the ISR to be executed is made up of the vector table base address and the ISR sequence number used as an offset.

If a high priority interrupt event occurs and a low priority interrupt event is waiting for a response, the higher priority interrupt event that arrives later will be responded to first. Another type of optimisation is called tail-chaining. When returning from a high-priority ISR, a pending low-priority ISR is then started, skipping unnecessary processor context stacking and stack popping. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- 4 levels of interrupt priority
- 1 NMI interrupt support
- 57 maskable interrupt channels (not including 16 CPU interrupts)
- High-priority interrupts can interrupt low-priority interrupt responses
- support for tail - chaining optimization

- Hardware interrupt vector retrieval

2.12.2. Extended interrupt/event controller (EXTI)

- EXTI adds flexibility in handling physical line events, as the system can be woken up by GPIO and specified module (PVD/RTC) input events.
- The EXTI controller has multiple channels, including up to 16 GPIOs, one PVD output and RTC wake-up signals. The GPIO, PVD can be configured for rising edge, falling edge or double edge triggering. Any GPIO signal is configured as EXTI0 ~ 15 channels by means of a selection signal.
- Each EXTI line can be masked independently via registers.
- The EXTI controller can capture pulses shorter than the internal clock period.
- Registers in the EXTI controller latch each event, even in stop mode, so that the processor can identify the source of the wake-up call after waking up from stop mode, or identify the GPIO and event that caused the interrupt.

2.13. Analog-to-digital converter (ADC)

- The module has a total of up to 19 channels to be measured, including 16 external channels and 3 internal channels, and performs conversions in single or sweep mode.
- The conversion mode for each channel can be set to single, continuous, scan or discontinuous mode. The conversion results are stored in a left- or right-aligned 16-bit data register.
- The analogue watchdog allows the application to detect if the input voltage exceeds a user defined high or low threshold.
- The ADC enables operation at low frequencies, resulting in very low power consumption. Interrupt requests are generated at the end of sampling, at the end of conversion, at the end of continuous conversion, and when the conversion voltage exceeds the threshold at analog watchdog.

2.14. Timer

The characteristics of the different timers of the PY32F403 are shown in the following table:

Table 2-4 Timer features

| Type | Timer | Bit width | Counting direction | Prescaler | DMA | Capture/compare channel | Complementary output |
|-----------------------|-------------------------------------|-----------|--------------------|-----------|-----|-------------------------|----------------------|
| Advanced Timer | TIM1 | 16 bits | Up, down, up/down | 1 ~ 65536 | Yes | 4 | 3 |
| | TIM8 | 16 bits | Up, down, up/down | 1 ~ 65536 | Yes | 4 | 3 |
| General Purpose Timer | TIM2 | 16 bits | Up, down, up/down | 1 ~ 65536 | Yes | 4 | - |
| | TIM3 | 16 bits | Up, down, up/down | 1 ~ 65536 | Yes | 4 | - |
| | TIM4 | 16 bits | Up, down, up/down | 1 ~ 65536 | Yes | 4 | - |
| | TIM5 | 16 bits | Up, down, up/down | 1 ~ 65536 | Yes | 4 | - |
| General purpose timer | TIM10/ TIM11/ TIM13/ TIM14 | 16 bits | Up | 1 ~ 65536 | - | 1 | - |

| Type | Timer | Bit width | Counting direction | Prescaler | DMA | Capture/compare channel | Complementary output |
|-----------------------|----------------|-----------|--------------------|-----------|-----|-------------------------|----------------------|
| General purpose timer | TIM9/ TIM12 | 16 bits | Up | 1 ~ 65536 | - | 2 | - |
| Basic Timer | TIM6,TIM7 | 16 bits | Up | 1 ~ 65536 | Yes | - | - |

2.14.1. Advanced-control timer

The advanced-control timer (TIM1/TIM8) consists of a 16-bit auto-load counter driven by a programmable divider. It can be used in various scenarios, including: pulse length measurement of the input signal (input capture) or to generate output waveforms (output comparison, output PWM, complementary PWM with deadband insertion).

TIM1/TIM8 include 4 independent channels used as

- input capture
- output compare
- PWM generation (edge or center aligned mode)
- single pulse mode output

If the TIM1/TIM8 is configured as a standard 16-bit timer, it has the same characteristics as the TIMx timer. If configured as a 16-bit PWM generator, it has full modulation capability (0 - 100%).

In MCU debug mode, TIM1/TIM8 can freeze the count.

The timer features with the same architecture are shared so that TIM1/TIM8 can work together with other timers via the timer link function for synchronisation or event linking.

TIM1/TIM8 support the DMA function.

2.14.2. General-purpose timers

2.14.2.1. TIM2/TIM3/TIM4/TIM5

The TIM2/TIM3/TIM4/TIM5 general purpose timers consist of a 16-bit automatic reload counter driven by a 16-bit programmable divider. There are four independent channels, each for input capture/output comparison, PWM or single pulse mode output.

- can work with TIM1 via the timer link function
- supports DMA functions
- Capable of handling quadrature (incremental) encoder signals and digital outputs from 1 to 3 Hall effect sensors
- In MCU debug mode, TIM2/TIM3/TIM4/TIM5 can freeze the count

2.14.2.2. TIM10/ TIM11/ TIM13/TIM14

- The general purpose timer TIM10/TIM11/TIM13/TIM14 consists of a 16-bit upward auto-loading counter driven by a programmable prescaler.
- TIM10/TIM11/TIM13/TIM14 have 1 independent channel for input capture/output comparison, PWM or single pulse mode output.
- In MCU debug mode, TIM10/TIM11/TIM13/TIM14 can freeze the count.

2.14.2.3. TIM9/TIM12

- TIM9 and TIM12 consist of 16-bit upward auto-loading counters driven by programmable

prescalers.

- TIM9 and TIM12 have 2 independent channels for input capture/output comparison, PWM or single pulse mode output.
- TIM9 and TIM12 have complementary outputs with deadband.
- In MCU debug mode, TIM9 and TIM12 can freeze the count.

2.14.3. Basic timers TIM6/TIM7

- The basic timers TIM6/TIM7 contain a 16-bit auto-load counter driven by the respective programmable prescaler.
- 16-bit auto load counter.
- Generates an interrupt/DMA request on the occurrence of an update event (counter overflow).

2.14.4. IWDG

An Independent watchdog (IWDG) is integrated into the chip, which is characterized by a high level of security, timing accuracy and flexibility. IWDG detects and resolves functional disruptions due to software failures and triggers a system reset when the counter reaches a specified timeout value.

- The IWDG is clocked by a separate RC oscillator and can be operated in STOP and STANDBY modes.
- The IWDG is best suited for applications that require a watchdog as a separate process from the main application and do not have high timing accuracy constraints.
- The IWDG hardware mode can be enabled by option byte control.
- IWDG is the wakeup source for the stop mode and wakes up the stop mode with a reset.
- In MCU debug mode, IWDG can freeze the count value.

2.14.5. WWDG

The system window watchdog is based on a 7-bit downstream counter and can be set to free run. It can be used as a watchdog to reset the system in case of a problem. The counter clock is the APB clock (PCLK). It has a warning interrupt capability and the counter can be frozen in MCU debug mode.

2.14.6. SysTick timer

SysTick counters are designed for use with real time operating systems (RTOS), but can also be used as standard down counters.

SysTick features:

- 24-bit down counter
- Self-loading capability
- Interrupts can be generated when the counter reaches 0 (maskable)

2.15. Real-time clock RTC

The real time clock (RTC) is an independent timer, the RTC module has a set of continuous counters which, when configured with the appropriate software, provide the function of a clock calendar. Modifying the counter values resets the current time and date of the system.

- The RTC is a 32-bit programmable counter with a prescale factor of up to 2^{20} .
- The RTC counter clock source can be the LSE, LSI and HSE clock divided by 128 and can be used as a stop wake-up source.
- The RTC can generate alarm interrupts, second interrupts and overflow interrupts (maskable).
- RTC supports clock calibration.
- In MCU debug mode, the RTC can freeze the count.

2.16. Cyclic redundancy check calculation unit (CRC)

The cyclic redundancy checks (CRC) calculation unit is a 32-bit CRC calculation based on a fixed generating polynomial. Among other applications, CRC technology is used to verify the correctness and integrity of data transmission or data storage. The CRC calculation unit contains a 32-bit data register:

- A write operation to this register serves as an input register for entering new data for the CRC calculation.
- A read of this register returns the result of the last CRC calculation.
- Each time a data register is written, the result of the calculation is a combination of the previous CRC calculation and the new calculation (CRC calculation is performed on the entire 32-bit word rather than byte by byte).
- can reset the register CRC_DR to 0xFFFF FFFF by setting the RESET bit of the register CRC_CR. This operation does not affect the data in the register CRC_IDR.
- supports the configuration of the initial CRC value.

2.17. Clock trimming controller (CTC)

The clock trimming controller (CTC) uses hardware to automatically calibrate the internal RC crystal configured at 48 MHz and used as the clock source for the USB module. The CTC module calibrates the HSI clock frequency based on an external high precision reference source and adjusts the calibration value automatically or manually to obtain an accurate PLL48M clock.

The CTC module performs the following functions:

- Three external reference sources: GPIO, LSE clock, USB_SOF.
- provides software reference synchronisation pulses.
- Hardware auto-calibration, no software required.
- 16-bit calibration counter with reference signal source capture and reload function.
- 8-bit clock calibration base for frequency evaluation and automatic calibration.
- Flag bits and interrupts to indicate the status of the clock calibration: calibration success (CKOKIF), warning status (CKWARNIF) and error status (ERRIF).

2.18. System Configuration Controller SYSCFG

The SYSCFG module performs the following functions:

- I²C fast mode plus, enabling/disabling some IO ports.
- Mapping of the initial program area according to the different boot modes.
- DMA peripheral channel selection control.
- TIMx cascade control.

2.19. Debug support (DBG)

The MCU DBG module assists the debugger by providing the following features:

- supports sleep mode, stop mode and standby mode
- Timer and watchdog stop counting or continue counting when CPU enters HALT
- CPU enters HALT to prevent I2C1 and I2C2 SMBUS timeout
- Prevent CANFD receive register update when CPU enters HALT
- Assign trace pins

The MCUIDBG register also provides the chip ID code. This ID code can be accessed using the JTAG or SW debug interface, or by the user program.

2.20. SDIO

The SD/SDIO MMC card host module (SDIO) provides an operational interface between the AHB peripheral bus and multimedia cards (MMC), SD memory cards, SDIO cards and CE-ATA devices.

The following functions are supported:

- Support for SD card version 2.0
- Support for SD I/O cards version 2.0
- supports MMC version 4.2
- Support for CE-ATA version 1.1
- Support for command completion signals and interrupts to the host processor
- Command completion signal off function

SDIO does not support SPI mode communication mode, only I/O mode for the I/O portion of the SD card or composite card, and cannot support many commands in SD memory devices, such as the erase command. In addition, some commands in SD memory cards and SD I/O cards are different, and SDIO does not support these commands.

2.21. I²C interface

The I²C (inter-integrated circuit) bus interface connects the microcontroller to the serial I²C bus. It provides multi-host functionality and controls all I²C bus specific sequences, protocols, arbitration and timing. Standard (Sm) and Fast (FM) are supported.

I²C features:

- 2 I²C interfaces, supports Slave and Master modes
- Multi-host function: Master and Slave
- Support for different communication speeds
 - Standard mode (Sm): up to 100 kHz

- Fast mode (FM): up to 400 kHz
- as Master
 - Clock generation
 - Start and Stop generation
- as slave
 - Programmable I²C address detection
 - Dual address capability to respond to 2 slave addresses
 - Stop bit discovery
- 7-bit/10-bit addressing mode
- General call
- Status flag bit
 - Transmit/receive mode flag bit
 - Byte transfer complete flag bit
 - I²C busy flag bit
- Error flag bit
 - Master arbitration loss
 - ACK failure after address/data transfer
 - Start/Stop error
 - Overrun/Underrun (clock stretching function disable)
- Optional clock stretching function
- DMA-capable single-byte buffer
- Software reset
- Analogue noise filtering function
- SMBus support

2.22. Universal synchronous/asynchronous receiver transmitter

(USART)

The PY32F403 contains 5 universal synchronous/asynchronous receivers transmitters (USARTs), supporting ISO7816, LIN and IrDA.

The USART provides a flexible method of exchanging full duplex data with external devices using the industry standard NRZ asynchronous serial data format. USART provides a wide range of baud rate options using a fractional baud rate generator.

It supports synchronous unidirectional communication and half-duplex single-line communication, and it also allows multi-processor communication.

Automatic baud rate detection is supported.

High speed data communication is possible using the DMA method with multi-buffer configuration.

USART features:

- Full duplex asynchronous communication
- NRZ standard format
- Configurable with 16x or 8x oversampling for increased flexibility in speed and clock tolerance

- Shared programmable baud rate for transmit and receive, up to 4.5 Mbit/s
- Automatic baud rate detection
- Programmable data length of 8 or 9 bits
- Configurable stop bits (0.5, 1, 1.5 or 2 stop bits supported)
- Transmitter provides clock for synchronous transmission
- Single-wire half-duplex communication
- Separate transmit and receive enable bits
- Hardware flow control
- Receive/send bytes buffered via DMA
- Detect flag
 - Receive buffer full
 - Send buffer empty
 - End of transfer
- Parity control
 - Send parity bit
 - Check summing of received data
- Interrupt source with flags
 - CTS change
 - Send register empty
 - Send complete
 - Receive data register full
 - Bus idle detected
 - Overflow error
 - Frame error
 - Noise operation
 - Checksum error
 - LIN disconnecter detection
- Multiprocessor communication
 - Silent mode if address does not match
- Wake up from silent mode: two ways of waking up the receiver by idle detection and address flag detection: address bit (MSB, bit 9), bus idle.

2.23. Serial peripheral interface (SPI)

The PY32F403 contains three SPI's. The serial peripheral interface (SPI) allows the chip to communicate with external devices in half duplex, full duplex and simplex synchronous serial mode. The interface can be configured in master mode and provides a serial clock (SCK) for external slave devices. The interface can also operate in a multi-master configuration.

The SPI features are as follows:

- Master or Slave mode
- 3-wire full duplex synchronous transmission

- 2-wire half-duplex synchronous transmission (with bi-directional data lines)
- 2-wire simplex synchronous transmission (no bidirectional data lines)
- 8-bit or 16-bit transmission frame selection
- Multi-master mode support
- 8 master mode baud rate prescale factors (max. $f_{PCLK}/4$)
- Slave mode frequency (up to $f_{PCLK}/4$)
- NSS management by software or hardware in both master and slave modes: dynamic change of master/slave operation mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flags
- Motorola mode
- Master mode faults, overloads that can cause interrupts
- 2 DMA-capable 64-bit Rx and Tx FIFOs

2.24. Inter-integrated sound (I²S)

- 3 I²S bus interfaces with sampling rates from 8 kHz to 192 kHz
- Supports master and slave modes, full duplex and simplex communication modes

The I²S bus provides a standard communication interface for digital audio applications over a 3-wire serial line. Contains two I²S bus interfaces that can operate in master or slave mode at 16/32-bit resolution, with pins multiplexed with SPI1 and SPI2 Audio sampling frequencies from 8 kHz to 192 kHz are supported with an accuracy error of less than 0.5%. All I²S interfaces can be used with a DMA controller.

2.25. External serial memory controller (ESMC)

The external serial memory controller (ESMC) is a dedicated communication interface for single SPI, dual SPI, quad SPI and dual-quad SPI channel SPI interface memories (NOR Flash, PSRAM, etc.). It can operate in either of the following two modes:

- Indirect mode: all operations are performed using the QUADSPI registers (indirect mode)
- memory mapped mode: the external flash is mapped to the device address space and the system treats it as internal memory (memory mapped mode)

Using dual memory mode, i.e. accessing two Quad SPI memories at the same time, can achieve twice the throughput and storage capacity similar to the Octal SPI memory.

- Two functional modes: indirect and memory mapped
- Simultaneous transmit/receive of 8 bits
- Dual Flash mode with simultaneous send/receive of 8 bits by accessing two Flash memories in parallel
- SDR and DDR support
- Fully programmable opcodes for indirect and memory mapped modes
- Fully programmable frame format for indirect and memory mapped modes

- Integrated FIFO for receive and transmit
- Allows 32-bit data access only
- DMA channel for indirect mode operation
- Interrupt generation on completion of FIFO operations

2.26. USB 2.0 full speed module

The PY32F403 contains a USB 2.0 Full Speed module, a USB peripheral that interfaces between the USB 2.0 Full Speed bus and the APB1 bus. It supports USB suspend/resume operation and can stop the device clock to achieve low power consumption. Key features are as follows:

- Conforms to the USB 2.0 Full Speed Device specification
- Configurable from 1 to 8 USB endpoints
- CRC (cyclic redundancy check) generation/checking, reverse non-zero (NRZI) encoding/decoding and bit padding
- Support for simultaneous transfers
- Dual buffer mechanism with support for bulk/synchronous endpoints
- Support for USB suspend/resume operations
- frame-locked clock pulse generation

2.27. CANFD

The PY32F403 contains a CANFD communication interface module.

The CAN (Controller Area Network) bus is a bus standard that enables microprocessors or devices to communicate with each other without a host. the CAN FD controller follows the CAN bus CAN 2.0 (2.0A, CAN 2.0B) and the CAN FD protocol.

The CAN bus controller can handle the sending and receiving of data on the bus. In this product, the CAN FD controller has 12 groups of filters. The filters are used to select the messages to be received for the application.

The application in the CAN FD controller can send transmit data to the bus via one high-priority Primary Transmit Buffer (hereinafter referred to as PTB) and three Secondary Transmit Buffers (hereinafter referred to as STB), with the transmit scheduler determining the order in which mailboxes are sent. The three STBs and the three RBs can be understood as a 3-stage FIFO and a 3-stage FIFO, which are fully controlled by the hardware.

The CAN FD bus controller can also support time-trigger communication.

- fully supports CAN2.0A/ CAN2.0B/ CANFD protocols
- CAN2.0 supports a maximum communication baud rate of 1 Mbit/s
- Supports prescaling of baud rates from 1 to 1/ 32 for flexible baud rate configuration
- 3 receive buffers
 - FIFO method
 - Errors or non-received data do not overwrite stored messages
- 1 high priority primary transmit buffer PTB
- 3 sub-send buffers STB

- FIFO method
- Priority arbitration method
- 12 independent filter groups
 - Supports 11-bit standard ID and 29-bit extended ID
 - Programmable ID CODE bits and MASK bits
- PTB/STB both support single send mode
- Silent mode support
- Supports loopback mode
- Support for capturing the type of error transmitted and locating the location of the arbitration failure
- Programmable error warning values
- Support for ISO 11898 - 4 time triggered CANFD and receive timestamps

2.28. SWD

The ARM SWD interface allows serial debugging tools to be connected to the PY32F403.

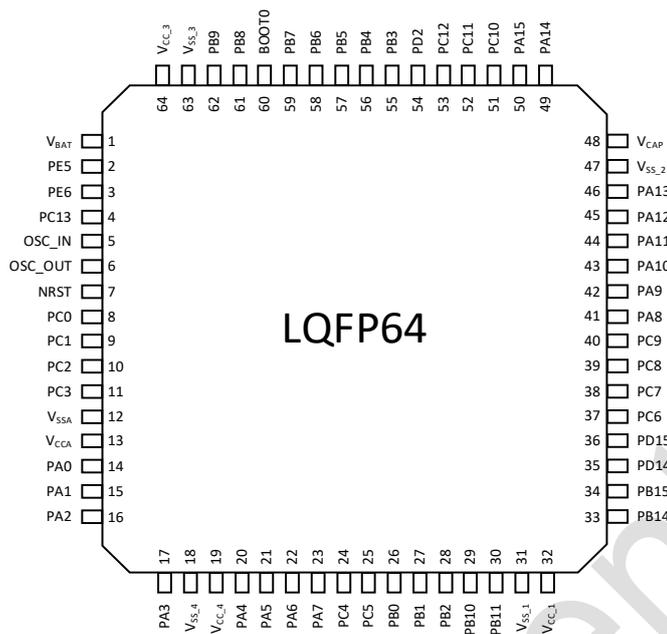


Figure 3-3 LQFP64 PY32F403R2xT Pinout2 (Top View)

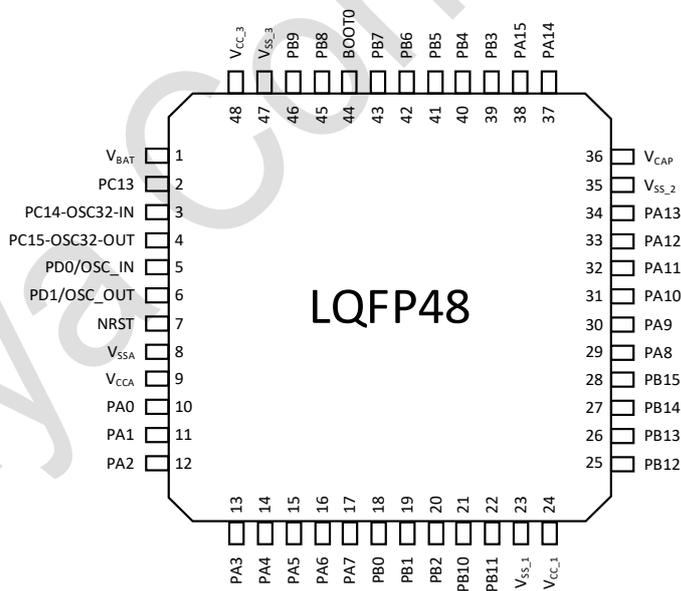


Figure 3-4 LQFP48 PY32F403C1xT Pinout1 (Top View)

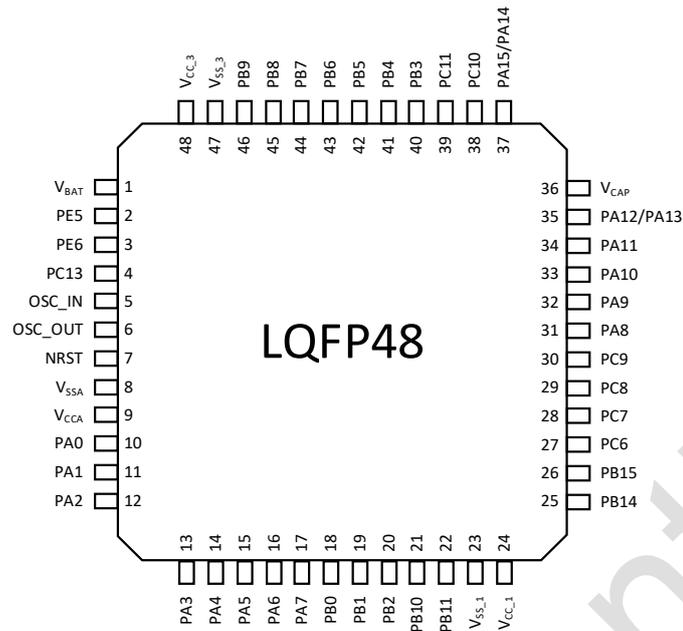


Figure 3-5 LQFP48 PY32F403C2xT Pinout2 (Top View)

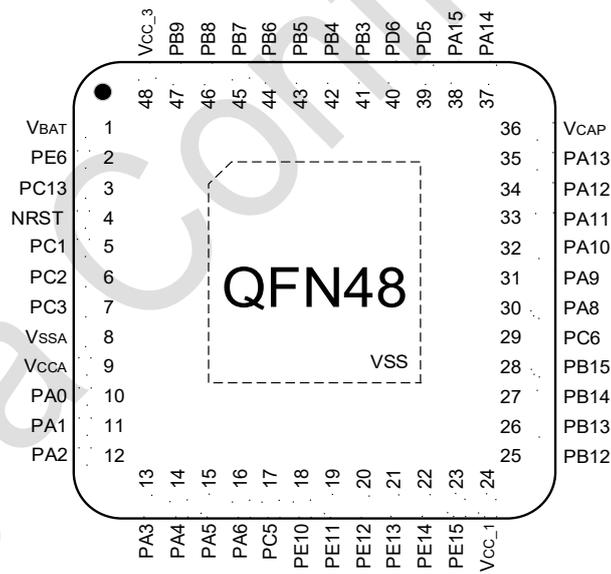


Figure 3-6 QFN48 PY32F403C1xU Pinout1 (Top View)

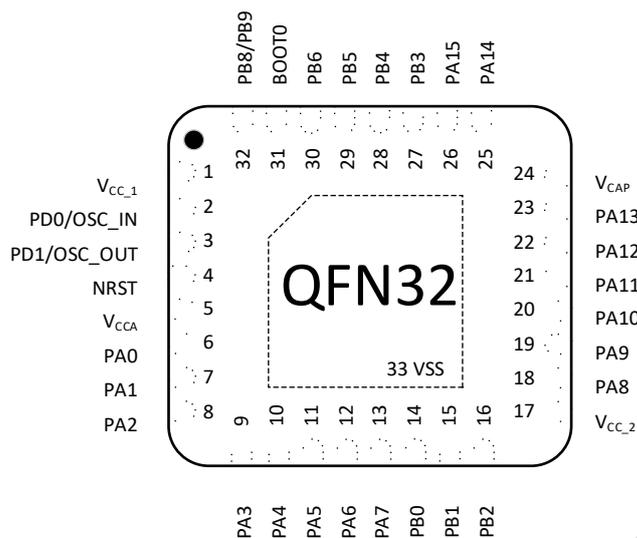


Figure 3-7 QFN32 PY32F403K1xU Pinout1 (Top View)

Table 3-1 Legend/abbreviations used in pinout table

| Type | Symbol | Definition | |
|---------------|----------------------|---|--|
| Pin type | S | Supply pin | |
| | G | Ground pin | |
| | I | Input - only pin | |
| | I/O | Input/ output pin | |
| | NC | No internal connection | |
| I/O structure | FT | 5 V-tolerant port | |
| | FT_u | 5 V-tolerant port with USB | |
| | TT | 3.3 V-tolerant port | |
| | TT_a | 3.3 V-tolerant port with analog switch function | |
| | NRST | Bidirectional reset pin with embedded weak pull-up resistor. Analog input or output is not supported. | |
| Note | - | Unless otherwise specified, all ports are used as floating inputs between and after reset. | |
| Pin functions | Alternate functions | - | Function selected through GPIOx_AFR register |
| | Additional functions | - | Functions directly selected/enabled through peripheral registers |

Table 3-2 Pin definitions

| Package Type | | | | | | | Reset | Pin type | I/O structure | Reset func-tion ⁽¹⁾ | Pin function | |
|--------------|-----------|-----------|-----------|-----------|----------|----------|---|----------|---------------|--------------------------------|----------------------------------|---------------------|
| LQFP100 V1 | LQFP64 R1 | LQFP64 R2 | LQFP48 C1 | LQFP48 C2 | QFN48 C1 | QFN32 K1 | | | | | Alternate function | Additional function |
| 1 | - | - | - | - | - | - | PE2 | I/O | FT | PE2 | TRACECK EVENT_OUT | - |
| 2 | - | - | - | - | - | - | PE3 | I/O | FT | PE3 | TRACED0 EVENT_OUT | - |
| 3 | - | - | - | - | - | - | PE4 | I/O | FT | PE4 | TRACED1 EVENT_OUT | - |
| 4 | - | 2 | - | 2 | - | - | PE5 | I/O | FT | PE5 | TRACED2 TIM9_CH1 EVENT_OUT | - |
| 5 | - | 3 | - | 3 | 2 | - | PE6 | I/O | FT | PE6 | TRACED3 TIM9_CH2 ENENT_OUT | WKUP3 |
| 6 | 1 | 1 | 1 | 1 | 1 | - | V _{BAT} | S | - | V _{BAT} | - | - |
| 7 | 2 | 4 | 2 | 4 | 3 | - | PC13-TAMPER RTC ⁽²⁾ ⁽³⁾⁽⁵⁾ | I/O | TT | PC13 | EVENT_OUT | TAMPER-RTC WKUP2 |
| 8 | 3 | - | 3 | - | - | - | PC14- OSC32_IN ⁽²⁾⁽³⁾ | I/O | TT | PC14 | EVENT_OUT | OSC32_IN |
| 9 | 4 | - | 4 | - | - | - | PC15- OSC32_OUT ⁽²⁾⁽³⁾ | I/O | TT | PC15 | EVENT_OUT | OSC32_OUT |
| 10 | - | - | - | - | - | - | V _{SS_5} | G | - | V _{SS_5} | - | - |
| 11 | - | - | - | - | - | - | V _{CC_5} | S | - | V _{CC_5} | - | - |
| 12 | 5 | 5 | 5 | 5 | - | 2 | OSC_IN | I | - | OSC_IN | - | - |
| 13 | 6 | 6 | 6 | 6 | - | 3 | OSC_OUT | O | - | OSC_OUT | - | - |
| 14 | 7 | 7 | 7 | 7 | 4 | 4 | NRST | I/O | - | NRST | - | - |

| Package Type | | | | | | | Reset | Pin type | I/O structure | Reset func-tion ⁽¹⁾ | Pin function | |
|--------------|-----------|-----------|-----------|-----------|----------|----------|-------------------|----------|---------------|--------------------------------|--|---------------------|
| LQFP100 V1 | LQFP64 R1 | LQFP64 R2 | LQFP48 C1 | LQFP48 C2 | QFN48 C1 | QFN32 K1 | | | | | Alternate function | Additional function |
| 15 | 8 | 8 | - | - | - | - | PC0 | I/O | TT_a | PC0 | EVENT_OUT | ADC123_IN10 |
| 16 | 9 | 9 | - | - | 5 | - | PC1 | I/O | TT_a | PC1 | ESMC_IO4 EVENT_OUT | ADC123_IN11 |
| 17 | 10 | 10 | - | - | 6 | - | PC2 | I/O | TT_a | PC2 | ESMC_IO5 EVENT_OUT | ADC123_IN12 |
| 18 | 11 | 11 | - | - | 7 | - | PC3 | I/O | TT_a | PC3 | ESMC_IO6 EVENT_OUT | ADC123_IN13 |
| 19 | 12 | 12 | 8 | 8 | 8 | - | V _{SSA} | G | - | V _{SSA} | - | - |
| 20 | - | - | - | - | - | - | V _{REF-} | S | - | V _{REF-} | - | - |
| 21 | - | - | - | - | - | - | V _{REF+} | S | - | V _{REF+} | - | - |
| 22 | 13 | 13 | 9 | 9 | 9 | 5 | V _{CCA} | S | - | V _{CCA} | - | - |
| 23 | 14 | 14 | 10 | 10 | 10 | 6 | PA0-WKUP1 | I/O | TT_a | PA0 | WKUP1 USART2_CTS TIM8_ETR TIM2_CH1_ETR TIM5_CH1 EVENT_OUT | ADC123_IN0 WKUP1 |
| 24 | 15 | 15 | 11 | 11 | 11 | 7 | PA1 | I/O | TT_a | PA1 | USART2_RTS TIM2_CH2 TIM5_CH2 EVENT_OUT | ADC123_IN1 |
| 25 | 16 | 16 | 12 | 12 | 12 | 8 | PA2 | I/O | TT_a | PA2 | USART2_TX TIM2_CH3 | ADC123_IN2 WKUP4 |

| Package Type | | | | | | | Reset | Pin type | I/O structure | Reset func-tion ⁽¹⁾ | Pin function | |
|--------------|-----------|-----------|-----------|-----------|----------|----------|-------------------|----------|---------------|--------------------------------|--------------------|---------------------|
| LQFP100 V1 | LQFP64 R1 | LQFP64 R2 | LQFP48 C1 | LQFP48 C2 | QFN48 C1 | QFN32 K1 | | | | | Alternate function | Additional function |
| | | | | | | | | | | | TIM5_CH3 | |
| | | | | | | | | | | | TIM9_CH1 | |
| | | | | | | | | | | | ESMC_SS0 | |
| | | | | | | | | | | | EVENT_OUT | |
| 26 | 17 | 17 | 13 | 13 | 13 | 9 | PA3 | I/O | TT_a | PA3 | USART2_RX | ADC123_IN3 |
| | | | | | | | | | | | TIM2_CH4 | |
| | | | | | | | | | | | TIM5_CH4 | |
| | | | | | | | | | | | TIM9_CH2 | |
| | | | | | | | | | | | ESMC_CLK | |
| | | | | | | | | | | | EVENT_OUT | |
| 27 | 18 | 18 | - | - | - | - | V _{SS_4} | G | - | V _{SS_4} | - | - |
| 28 | 19 | 19 | - | - | - | - | V _{CC_4} | S | - | V _{CC_4} | - | - |
| 29 | 20 | 20 | 14 | 14 | 14 | 10 | PA4 | I/O | TT_a | PA4 | USART2_CK | ADC12_IN4 |
| | | | | | | | | | | | SPI1_NSS | |
| | | | | | | | | | | | EVENT_OUT | |
| 30 | 21 | 21 | 15 | 15 | 15 | 11 | PA5 | I/O | TT_a | PA5 | SPI1_SCK | ADC12_IN5 |
| | | | | | | | | | | | EVENT_OUT | |
| 31 | 22 | 22 | 16 | 16 | 16 | 12 | PA6 | I/O | TT_a | PA6 | SPI1_MISO | ADC12_IN6 |
| | | | | | | | | | | | TIM8_BKIN | |
| | | | | | | | | | | | TIM3_CH1 | |
| | | | | | | | | | | | TIM13_CH1 | |
| | | | | | | | | | | | ESMC_IO3 | |
| | | | | | | | | | | | EVENT_OUT | |

| Package Type | | | | | | | Reset | Pin type | I/O structure | Reset func-tion ⁽¹⁾ | Pin function | |
|--------------|-----------|-----------|-----------|-----------|----------|----------|-------|----------|---------------|--------------------------------|----------------------|---------------------|
| LQFP100 V1 | LQFP64 R1 | LQFP64 R2 | LQFP48 C1 | LQFP48 C2 | QFN48 C1 | QFN32 K1 | | | | | Alternate function | Additional function |
| 32 | 23 | 23 | 17 | 17 | - | 13 | PA7 | I/O | TT_a | PA7 | SPI1_MOSI | ADC12_IN7 |
| | | | | | | | | | | | TIM8_CH1N | |
| | | | | | | | | | | | TIM14_CH1 | |
| | | | | | | | | | | | ESMC_IO2 | |
| | | | | | | | | | | | EVENT_OUT | |
| 33 | 24 | 24 | - | - | - | - | PC4 | I/O | TT_a | PC4 | ESMC_IO7 | ADC12_IN14 |
| | | | | | | | | | | | EVENT_OUT | |
| 34 | 25 | 25 | - | - | 17 | - | PC5 | I/O | TT_a | PC5 | EVENT_OUT | ADC12_IN15 WKUP5 |
| 35 | 26 | 26 | 18 | 18 | - | 14 | PB0 | I/O | TT_a | PB0 | TIM1_CH2N | ADC12_IN8 |
| | | | | | | | | | | | TIM8_CH2N | |
| | | | | | | | | | | | TIM3_CH3 | |
| | | | | | | | | | | | ESMC_IO1 | |
| | | | | | | | | | | | I ² S3_CK | |
| | | | | | | | | | | | EVENT_OUT | |
| 36 | 27 | 27 | 19 | 19 | - | 15 | PB1 | I/O | TT_a | PB1 | TIM1_CH3N | ADC12_IN9 |
| | | | | | | | | | | | TIM8_CH3N | |
| | | | | | | | | | | | ESMC_IO0 | |
| | | | | | | | | | | | EVENT_OUT | |
| 37 | 28 | 28 | 20 | 20 | - | 16 | PB2 | I/O | FT | PB2/BOOT1 | EVENT_OUT | BOOT1 |
| 38 | - | - | - | - | - | - | PE7 | I/O | FT | PE7 | TIM1_ETR | - |
| 39 | - | - | - | - | - | - | PE8 | I/O | FT | PE8 | TIM1_CH1N | - |
| 40 | - | - | - | - | - | - | PE9 | I/O | FT | PE9 | TIM1_CH1 | - |

| Package Type | | | | | | | Reset | Pin type | I/O structure | Reset func-tion ⁽¹⁾ | Pin function | |
|--------------|-----------|-----------|-----------|-----------|----------|----------|-------|----------|---------------|--------------------------------|---|---------------------|
| LQFP100 V1 | LQFP64 R1 | LQFP64 R2 | LQFP48 C1 | LQFP48 C2 | QFN48 C1 | QFN32 K1 | | | | | Alternate function | Additional function |
| 41 | - | - | - | - | 18 | - | PE10 | I/O | FT | PE10 | TIM1_CH2N ESMC_CLK EVENT_OUT | - |
| 42 | - | - | - | - | 19 | - | PE11 | I/O | FT | PE11 | TIM1_CH2 ESMC_SS3 EVENT_OUT | - |
| 43 | - | - | - | - | 20 | - | PE12 | I/O | FT | PE12 | TIM1_CH3N ESMC_IO0 EVENT_OUT | - |
| 44 | - | - | - | - | 21 | - | PE13 | I/O | FT | PE13 | TIM1_CH3 ESMC_IO1 EVENT_OUT | - |
| 45 | - | - | - | - | 22 | - | PE14 | I/O | FT | PE14 | TIM1_CH4 ESMC_IO2 EVENT_OUT | - |
| 46 | - | - | - | - | 23 | - | PE15 | I/O | FT | PE15 | TIM1_BKIN ESMC_IO3 EVENT_OUT | - |
| 47 | 29 | 29 | 21 | 21 | - | - | PB10 | I/O | FT | PB10 | I ² C2_SCL USART3_TX TIM2_CH3 ESMC_CLK EVENT_OUT | - |

| Package Type | | | | | | | Reset | Pin type | I/O structure | Reset func-tion ⁽¹⁾ | Pin function | |
|--------------|-----------|-----------|-----------|-----------|----------|----------|-------------------|----------|---------------|--------------------------------|------------------------|---------------------|
| LQFP100 V1 | LQFP64 R1 | LQFP64 R2 | LQFP48 C1 | LQFP48 C2 | QFN48 C1 | QFN32 K1 | | | | | Alternate function | Additional function |
| 48 | 30 | 30 | 22 | 22 | - | - | PB11 | I/O | FT | PB11 | I ² C2_SDA | - |
| | | | | | | | | | | | USART3_RX | |
| | | | | | | | | | | | TIM2_CH4 | |
| | | | | | | | | | | | ESMC_SS1 | |
| | | | | | | | | | | | EVENT_OUT | |
| 49 | 31 | 31 | 23 | 23 | - | - | V _{SS_1} | G | - | V _{SS_1} | - | - |
| 50 | 32 | 32 | 24 | 24 | 24 | 1 | V _{CC_1} | S | - | V _{CC_1} | - | - |
| 51 | 33 | - | 25 | - | 25 | - | PB12 | I/O | FT | PB12 | I ² C2_SMBA | - |
| | | | | | | | | | | | USART3_CK | |
| | | | | | | | | | | | SPI2_NSS | |
| | | | | | | | | | | | TIM1_BKIN | |
| | | | | | | | | | | | I ² S2_WS | |
| | | | | | | | | | | | EVENT_OUT | |
| 52 | 34 | - | 26 | - | 26 | - | PB13 | I/O | FT | PB13 | USART3_CTS | - |
| | | | | | | | | | | | SPI2_SCK | |
| | | | | | | | | | | | TIM1_CH1N | |
| | | | | | | | | | | | I ² S2_CK | |
| | | | | | | | | | | | EVENT_OUT | |
| 53 | 35 | 33 | 27 | 25 | 27 | - | PB14 | I/O | FT | PB14 | USART3_RTS | - |
| | | | | | | | | | | | SPI2_MISO | |
| | | | | | | | | | | | TIM1_CH2N | |
| | | | | | | | | | | | TIM12_CH1 | |
| | | | | | | | | | | | EVENT_OUT | |

| Package Type | | | | | | | Reset | Pin type | I/O structure | Reset func-tion ⁽¹⁾ | Pin function | |
|--------------|-----------|-----------|-----------|-----------|----------|----------|-------|----------|---------------|--------------------------------|----------------------|---------------------|
| LQFP100 V1 | LQFP64 R1 | LQFP64 R2 | LQFP48 C1 | LQFP48 C2 | QFN48 C1 | QFN32 K1 | | | | | Alternate function | Additional function |
| 54 | 36 | 34 | 28 | 26 | 28 | - | PB15 | I/O | FT | PB15 | SPI2_MOSI | - |
| | | | | | | | | | | | TIM1_CH3N | |
| | | | | | | | | | | | TIM12_CH2 | |
| | | | | | | | | | | | I ² S2_SD | |
| | | | | | | | | | | | EVENT_OUT | |
| 55 | - | - | - | - | - | - | PD8 | I/O | FT | PD8 | USART3_TX | - |
| | | | | | | | | | | | EVENT_OUT | |
| 56 | - | - | - | - | - | - | PD9 | I/O | FT | PD9 | USART3_RX | - |
| | | | | | | | | | | | EVENT_OUT | |
| 57 | - | - | - | - | - | - | PD10 | I/O | FT | PD10 | USART3_CK | - |
| | | | | | | | | | | | EVENT_OUT | |
| 58 | - | - | - | - | - | - | PD11 | I/O | FT | PD11 | USART3_CTS | - |
| | | | | | | | | | | | EVENT_OUT | |
| 59 | - | - | - | - | - | - | PD12 | I/O | FT | PD12 | TIM4_CH1 | - |
| | | | | | | | | | | | USART3_RTS | |
| | | | | | | | | | | | EVENT_OUT | |
| 60 | - | - | - | - | - | - | PD13 | I/O | FT | PD13 | TIM4_CH2 | - |
| | | | | | | | | | | | EVENT_OUT | |
| 61 | - | 35 | - | - | - | - | PD14 | I/O | FT | PD14 | TIM4_CH3 | - |
| | | | | | | | | | | | EVENT_OUT | |
| 62 | - | 36 | - | - | - | - | PD15 | I/O | FT | PD15 | TIM4_CH4 | - |
| | | | | | | | | | | | EVENT_OUT | |
| 63 | 37 | 37 | - | 27 | 29 | - | PC6 | I/O | FT | PC6 | USART4_CK | - |

| Package Type | | | | | | | Reset | Pin type | I/O structure | Reset func-tion ⁽¹⁾ | Pin function | |
|--------------|-----------|-----------|-----------|-----------|----------|----------|-------|----------|---------------|--------------------------------|-----------------------|---------------------|
| LQFP100 V1 | LQFP64 R1 | LQFP64 R2 | LQFP48 C1 | LQFP48 C2 | QFN48 C1 | QFN32 K1 | | | | | Alternate function | Additional function |
| | | | | | | | | | | | TIM8_CH1 | |
| | | | | | | | | | | | TIM3_CH1 | |
| | | | | | | | | | | | SDIO_D6 | |
| | | | | | | | | | | | I ² S2_MCK | |
| | | | | | | | | | | | EVENT_OUT | |
| 64 | 38 | 38 | - | 28 | - | - | PC7 | I/O | FT | PC7 | USART4_CTS | |
| | | | | | | | | | | | TIM8_CH2 | |
| | | | | | | | | | | | TIM3_CH2 | |
| | | | | | | | | | | | SDIO_D7 | - |
| | | | | | | | | | | | I ² S3_MCK | |
| | | | | | | | | | | | EVENT_OUT | |
| 65 | 39 | 39 | - | 29 | - | - | PC8 | I/O | FT | PC8 | USART4_RTS | |
| | | | | | | | | | | | TIM8_CH3 | |
| | | | | | | | | | | | TIM3_CH3 | |
| | | | | | | | | | | | SDIO_D0 | - |
| | | | | | | | | | | | EVENT_OUT | |
| 66 | 40 | 40 | - | 30 | - | - | PC9 | I/O | FT | PC9 | TIM8_CH4 | |
| | | | | | | | | | | | TIM3_CH4 | |
| | | | | | | | | | | | SDIO_D1 | - |
| | | | | | | | | | | | EVENT_OUT | |
| 67 | 41 | 41 | 29 | 31 | 30 | 18 | PA8 | I/O | FT | PA8 | MCO | |
| | | | | | | | | | | | USART1_CK | - |
| | | | | | | | | | | | TIM1_CH1 | |

| Package Type | | | | | | | Reset | Pin type | I/O structure | Reset func-tion ⁽¹⁾ | Pin function | |
|--------------|-----------|-----------|-----------|-----------|----------|----------|---------------------------------|----------|---------------|--------------------------------|--------------------|---------------------|
| LQFP100 V1 | LQFP64 R1 | LQFP64 R2 | LQFP48 C1 | LQFP48 C2 | QFN48 C1 | QFN32 K1 | | | | | Alternate function | Additional function |
| | | | | | | | | | | | EVENT_OUT | |
| 68 | 42 | 42 | 30 | 32 | 31 | 19 | PA9 | I/O | FT | PA9 | USART1_TX | - |
| | | | | | | | | | | | TIM1_CH2 | |
| | | | | | | | | | | | EVENT_OUT | |
| 69 | 43 | 43 | 31 | 33 | 32 | 20 | PA10 | I/O | FT | PA10 | USART1_RX | - |
| | | | | | | | | | | | CTC_SYNC | |
| | | | | | | | | | | | TIM1_CH3 | |
| | | | | | | | | | | | EVENT_OUT | |
| 70 | 44 | 44 | 32 | 34 | 33 | 21 | PA11 | I/O | FT_u | PA11 | USART1_CTS | USB_DM |
| | | | | | | | | | | | TIM1_CH4 | |
| | | | | | | | | | | | CAN_RX | |
| | | | | | | | | | | | EVENT_OUT | |
| 71 | 45 | 45 | 33 | 35 | 34 | 22 | PA12 | I/O | FT_u | PA12 | USART1_RTS | USB_DP |
| | | | | | | | | | | | TIM1_ETR | |
| | | | | | | | | | | | CAN_TX | |
| | | | | | | | | | | | EVENT_OUT | |
| 72 | 46 | 46 | 34 | 35 | 35 | 23 | PA13 | I/O | FT | JTMS-SWDIO | JTMS-SWDIO | - |
| | | | | | | | | | | | EVENT_OUT | |
| 73 | 48 | 48 | 36 | 36 | 36 | 24 | V _{CAP} ⁽⁴⁾ | - | - | V _{CAP} | - | - |
| 74 | 47 | 47 | 35 | - | - | - | V _{SS_2} | G | - | V _{SS_2} | - | - |
| 75 | - | - | - | - | - | 17 | V _{CC_2} | S | - | V _{CC_2} | - | - |
| 76 | 49 | 49 | 37 | 37 | 37 | 25 | PA14 | I/O | FT | JTCK-SWCLK | JTCK-SWCLK | - |
| | | | | | | | | | | | EVENT_OUT | |

| Package Type | | | | | | | Reset | Pin type | I/O structure | Reset func-tion ⁽¹⁾ | Pin function | |
|--------------|-----------|-----------|-----------|-----------|----------|----------|-------|----------|---------------|--------------------------------|----------------------|---------------------|
| LQFP100 V1 | LQFP64 R1 | LQFP64 R2 | LQFP48 C1 | LQFP48 C2 | QFN48 C1 | QFN32 K1 | | | | | Alternate function | Additional function |
| 77 | 50 | 50 | 38 | 37 | 38 | 26 | PA15 | I/O | FT | JTDI | JTDI | - |
| | | | | | | | | | | | SPI3_NSS | |
| | | | | | | | | | | | SPI1_NSS | |
| | | | | | | | | | | | TIM2_CH1_ETR | |
| | | | | | | | | | | | I ² S3_WS | |
| | | | | | | | | | | | EVENT_OUT | |
| 78 | 51 | 51 | - | 38 | - | - | PC10 | I/O | FT | PC10 | USART4_TX | - |
| | | | | | | | | | | | USART3_TX | |
| | | | | | | | | | | | SDIO_D2 | |
| | | | | | | | | | | | EVENT_OUT | |
| 79 | 52 | 52 | - | 39 | - | - | PC11 | I/O | FT | PC11 | USART4_RX | - |
| | | | | | | | | | | | USART3_RX | |
| | | | | | | | | | | | SDIO_D3 | |
| | | | | | | | | | | | EVENT_OUT | |
| 80 | 53 | 53 | - | - | - | - | PC12 | I/O | FT | PC12 | USART5_TX | - |
| | | | | | | | | | | | USART3_CK | |
| | | | | | | | | | | | SDIO_CK | |
| | | | | | | | | | | | EVENT_OUT | |
| 81 | 5 | - | 5 | - | - | 2 | PD0 | I/O | FT | - | CAN_RX | - |
| | | | | | | | | | | | EVENT_OUT | |
| 82 | 6 | - | 6 | - | - | 3 | PD1 | I/O | FT | - | CAN_TX | - |
| | | | | | | | | | | | EVENT_OUT | |
| 83 | 54 | 54 | - | - | - | - | PD2 | I/O | FT | PD2 | TIM3_ETR | - |

| Package Type | | | | | | | Reset | Pin type | I/O structure | Reset func-tion ⁽¹⁾ | Pin function | |
|--------------|-----------|-----------|-----------|-----------|----------|----------|-------|----------|---------------|--------------------------------|--------------------|---------------------|
| LQFP100 V1 | LQFP64 R1 | LQFP64 R2 | LQFP48 C1 | LQFP48 C2 | QFN48 C1 | QFN32 K1 | | | | | Alternate function | Additional function |
| | | | | | | | | | | | USART5_RX | |
| | | | | | | | | | | | SDIO_CMD | |
| | | | | | | | | | | | EVENT_OUT | |
| 84 | - | - | - | - | - | - | PD3 | I/O | FT | PD3 | USART2_CTS | - |
| | | | | | | | | | | | USART5_CK | |
| | | | | | | | | | | | ESMC_SS2 | |
| | | | | | | | | | | | EVENT_OUT | |
| 85 | - | - | - | - | - | - | PD4 | I/O | FT | PD4 | USART2_RTS | - |
| | | | | | | | | | | | USART5_CTS | |
| | | | | | | | | | | | ESMC_IO4 | |
| | | | | | | | | | | | EVENT_OUT | |
| 86 | - | - | - | - | 39 | - | PD5 | I/O | FT | PD5 | USART2_TX | - |
| | | | | | | | | | | | USART5_RTS | |
| | | | | | | | | | | | ESMC_IO5 | |
| | | | | | | | | | | | EVENT_OUT | |
| 87 | - | - | - | - | 40 | - | PD6 | I/O | FT | PD6 | USART2_RX | - |
| | | | | | | | | | | | ESMC_IO6 | |
| | | | | | | | | | | | EVENT_OUT | |
| 88 | - | - | - | - | - | - | PD7 | I/O | FT | PD7 | USART2_CK | - |
| | | | | | | | | | | | ESMC_IO7 | |
| | | | | | | | | | | | EVENT_OUT | |
| 89 | 55 | 55 | 39 | 40 | 41 | 27 | PB3 | I/O | FT | JTDO | JTDO-TRACESWO | - |
| | | | | | | | | | | | SPI3_SCK | |

| Package Type | | | | | | | Reset | Pin type | I/O structure | Reset func-tion ⁽¹⁾ | Pin function | |
|--------------|-----------|-----------|-----------|-----------|----------|----------|-------|----------|---------------|--------------------------------|------------------------|---------------------|
| LQFP100 V1 | LQFP64 R1 | LQFP64 R2 | LQFP48 C1 | LQFP48 C2 | QFN48 C1 | QFN32 K1 | | | | | Alternate function | Additional function |
| | | | | | | | | | | | SPI1_SCK | |
| | | | | | | | | | | | TIM2_CH2 | |
| | | | | | | | | | | | EVENT_OUT | |
| 90 | 56 | 56 | 40 | 41 | 42 | 28 | PB4 | I/O | FT | NJTRST | NJTRST | - |
| | | | | | | | | | | | SPI3_MISO | |
| | | | | | | | | | | | SPI1_MISO | |
| | | | | | | | | | | | TIM3_CH1 | |
| | | | | | | | | | | | EVENT_OUT | |
| 91 | 57 | 57 | 41 | 42 | 43 | 29 | PB5 | I/O | TT | PB5 | PB5 | - |
| | | | | | | | | | | | I ² C1_SMBA | |
| | | | | | | | | | | | SPI3_MOSI | |
| | | | | | | | | | | | SPI1_MOSI | |
| | | | | | | | | | | | TIM3_CH2 | |
| | | | | | | | | | | | I ² S3_SD | |
| | | | | | | | | | | | EVENT_OUT | |
| 92 | 58 | 58 | 42 | 43 | 44 | 30 | PB6 | I/O | FT | PB6 | PB6 | - |
| | | | | | | | | | | | I ² C1_SCL | |
| | | | | | | | | | | | USART1_TX | |
| | | | | | | | | | | | TIM4_CH1 | |
| | | | | | | | | | | | EVENT_OUT | |
| 93 | 59 | 59 | 43 | 44 | 45 | - | PB7 | I/O | FT | PB7 | PB7 | - |
| | | | | | | | | | | | I ² C1_SDA | |
| | | | | | | | | | | | USART1_RX | |
| | | | | | | | | | | | TIM4_CH2 | |
| | | | | | | | | | | | EVENT_OUT | |
| 94 | 60 | 60 | 44 | - | - | 31 | BOOT0 | I | - | BOOT0 | BOOT0 | - |

| Package Type | | | | | | | Reset | Pin type | I/O structure | Reset func-tion ⁽¹⁾ | Pin function | |
|--------------|-----------|-----------|-----------|-----------|----------|----------|-------------------|----------|---------------|--------------------------------|-----------------------|---------------------|
| LQFP100 V1 | LQFP64 R1 | LQFP64 R2 | LQFP48 C1 | LQFP48 C2 | QFN48 C1 | QFN32 K1 | | | | | Alternate function | Additional function |
| 95 | 61 | 61 | 45 | 45 | 46 | 32 | PB8 | I/O | FT | PB8 | I ² C1_SCL | - |
| | | | | | | | | | | | TIM4_CH3 | |
| | | | | | | | | | | | TIM10_CH1 | |
| | | | | | | | | | | | CAN_RX | |
| | | | | | | | | | | | SDIO_D4 | |
| | | | | | | | | | | | EVENT_OUT | |
| 96 | 62 | 62 | 46 | 46 | 47 | 32 | PB9 | I/O | FT | PB9 | I ² C1_SDA | - |
| | | | | | | | | | | | TIM4_CH4 | |
| | | | | | | | | | | | TIM11_CH1 | |
| | | | | | | | | | | | CAN_TX | |
| | | | | | | | | | | | SDIO_D45 | |
| | | | | | | | | | | | EVENT_OUT | |
| 97 | - | - | - | - | - | - | PE0 | I/O | FT | PE0 | TIM4_ETR | - |
| | | | | | | | | | | | EVENT_OUT | |
| 98 | - | - | - | - | - | - | PE1 | I/O | FT | PE1 | EVENT_OUT | - |
| 99 | 63 | 63 | 47 | 47 | - | - | V _{SS_3} | G | - | V _{SS_3} | - | - |
| 100 | 64 | 64 | 48 | 48 | 48 | - | V _{CC_3} | S | - | V _{CC_3} | - | - |

- The available functions depend on the selected device. If multiple peripherals share the same I/O pins, to avoid conflicts between these alternate functions, only one peripheral can be enabled at a time via the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
- PC13, PC14 and PC15 are powered via a power switch. Due to the limited current fill capability of this switch (3 mA), the following limitations exist when using GPIO PC13 to PC15 in output mode:
 - the rate must not exceed 2 MHz and the maximum load is 30 pF.

- 2) These I/Os cannot be used as current sources (e.g. for driving LEDs).
3. The main function after the first backup domain power-up. After this it depends on the contents of the backup registers, even after a reset (as these registers are not controlled by the main area reset).
4. LDO core-powered output (internal circuits only, external 0.1 ~ 1 μ F decoupling capacitor required).
5. When only V_{BAT} is powered, PC13 may be in one of the following states: analog mode, input mode, push-pull with pull-up, or push-pull with pull-down. Design recommendations:
 - a) Add a 1–10 M Ω resistor to ground on PC13 to prevent leakage current when the pin is in input mode.
 - b) Resistor selection (as in recommendation a) should account for the output current when PC13 is configured as push-pull with pull-up.

3.1. Port A multiplexed function mapping

Table 3-3 Port A multiplexed function mapping

| PortA | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|-------|------------|-----|------------|-----------|----------|-----------|--------------|----------|-----------|-----|----------|------|------|------|---------|-----------|
| PA0 | - | - | USART2_CTS | - | - | TIM8_ETR | TIM2_CH1_ETR | TIM5_CH1 | - | - | - | - | - | - | - | EVENT_OUT |
| PA1 | - | - | USART2_RTS | - | - | - | TIM2_CH2 | TIM5_CH2 | - | - | - | - | - | - | - | EVENT_OUT |
| PA2 | - | - | USART2_TX | - | - | - | TIM2_CH3 | TIM5_CH3 | TIM9_CH1 | - | ESMC_SS0 | - | - | - | - | EVENT_OUT |
| PA3 | - | - | USART2_RX | - | - | - | TIM2_CH4 | TIM5_CH4 | TIM9_CH2 | - | ESMC_CLK | - | - | - | - | EVENT_OUT |
| PA4 | - | - | USART2_CK | SPI1_NSS | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PA5 | - | - | - | SPI1_SCK | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PA6 | - | - | - | SPI1_MISO | - | TIM8_BKIN | TIM3_CH1 | - | TIM13_CH1 | - | ESMC_IO3 | - | - | - | - | EVENT_OUT |
| PA7 | - | - | - | SPI1_MOSI | - | TIM8_CH1N | - | - | TIM14_CH1 | - | ESMC_IO2 | - | - | - | - | EVENT_OUT |
| PA8 | MCO | - | USART1_CK | - | TIM1_CH1 | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PA9 | - | - | USART1_TX | - | TIM1_CH2 | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PA10 | - | - | USART1_RX | CTC_SYNC | TIM1_CH3 | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PA11 | - | - | USART1_CTS | - | TIM1_CH4 | - | - | - | - | - | CAN_RX | - | - | - | - | EVENT_OUT |
| PA12 | - | - | USART1_RTS | - | TIM1_ETR | - | - | - | - | - | CAN_TX | - | - | - | - | EVENT_OUT |
| PA13 | JTMS-SWDIO | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PA14 | JTCK-SWCLK | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PA15 | JTDI | - | SPI3_NSS | SPI1_NSS | - | - | TIM2_CH1_ETR | - | - | - | - | - | - | - | I2S3_WS | EVENT_OUT |

3.2. Port B multiplexed function mapping

Table 3-4 Port B multiplexed function mapping

| PortB | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|-------|---------------|-----|-----------|-----------|-----------|-----------|----------|-----|-----|-----|----------|------|------|------|---------|-----------|
| PB0 | - | - | - | - | TIM1_CH2N | TIM8_CH2N | TIM3_CH3 | - | - | - | ESMC_IO1 | - | - | - | I2S3_CK | EVENT_OUT |
| PB1 | - | - | - | - | TIM1_CH3N | TIM8_CH3N | - | - | - | - | ESMC_IO0 | - | - | - | - | EVENT_OUT |
| PB2 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PB3 | JTDO-TRACESWO | - | SPI3_SCK | SPI1_SCK | - | - | TIM2_CH2 | - | - | - | - | - | - | - | - | EVENT_OUT |
| PB4 | NJTRST | - | SPI3_MISO | SPI1_MISO | - | - | TIM3_CH1 | - | - | - | - | - | - | - | - | EVENT_OUT |

| PortB | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|-------|-----|------------------------|------------|-----------|-----------|-----|----------|----------|-----------|-----|----------|---------|------|------|----------------------|-----------|
| PB5 | - | I ² C1_SMBA | SPI3_MOSI | SPI1_MOSI | - | - | TIM3_CH2 | - | - | - | - | - | - | - | I2S3_SD | EVENT_OUT |
| PB6 | - | I ² C1_SCL | USART1_TX | - | - | - | TIM4_CH1 | - | - | - | - | - | - | - | - | EVENT_OUT |
| PB7 | - | I ² C1_SDA | USART1_RX | - | - | - | TIM4_CH2 | - | - | - | - | - | - | - | - | EVENT_OUT |
| PB8 | - | I ² C1_SCL | - | - | - | - | TIM4_CH3 | - | TIM10_CH1 | - | CAN_RX | SDIO_D4 | - | - | - | EVENT_OUT |
| PB9 | - | I ² C1_SDA | - | - | - | - | TIM4_CH4 | - | TIM11_CH1 | - | CAN_TX | SDIO_D5 | - | - | - | EVENT_OUT |
| PB10 | - | I ² C2_SCL | USART3_TX | - | - | - | TIM2_CH3 | - | - | - | ESMC_CLK | - | - | - | - | EVENT_OUT |
| PB11 | - | I ² C2_SDA | USART3_RX | - | - | - | TIM2_CH4 | - | - | - | ESMC_SS1 | - | - | - | - | EVENT_OUT |
| PB12 | - | I ² C2_SMBA | USART3_CK | SPI2_NSS | TIM1_BKIN | - | - | TIM5_ETR | - | - | - | - | - | - | I ² S2_WS | EVENT_OUT |
| PB13 | - | - | USART3_CTS | SPI2_SCK | TIM1_CH1N | - | - | - | - | - | - | - | - | - | I ² S2_CK | EVENT_OUT |
| PB14 | - | - | USART3_RTS | SPI2_MISO | TIM1_CH2N | - | - | - | TIM12_CH1 | - | - | - | - | - | - | EVENT_OUT |
| PB15 | - | - | - | SPI2_MOSI | TIM1_CH3N | - | - | - | TIM12_CH2 | - | - | - | - | - | I ² S2_SD | EVENT_OUT |

3.3. Port C multiplexing function mapping

Table 3-5 Port C multiplexing function mapping

| PortC | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|-------|-----|------------|-----------|-----|-----|----------|----------|-----|-----|-----|----------|---------|------|------|----------|-----------|
| PC0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PC1 | - | - | - | - | - | - | - | - | - | - | ESMC_IO4 | - | - | - | - | EVENT_OUT |
| PC2 | - | - | - | - | - | - | - | - | - | - | ESMC_IO5 | - | - | - | - | EVENT_OUT |
| PC3 | - | - | - | - | - | - | - | - | - | - | ESMC_IO6 | - | - | - | - | EVENT_OUT |
| PC4 | - | - | - | - | - | - | - | - | - | - | ESMC_IO7 | - | - | - | - | EVENT_OUT |
| PC5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | I2S1_MCK | EVENT_OUT |
| PC6 | - | USART4_CK | - | - | - | TIM8_CH1 | TIM3_CH1 | - | - | - | - | SDIO_D6 | - | - | I2S2_MCK | EVENT_OUT |
| PC7 | - | USART4_CTS | - | - | - | TIM8_CH2 | TIM3_CH2 | - | - | - | - | SDIO_D7 | - | - | I2S3_MCK | EVENT_OUT |
| PC8 | - | USART4_RTS | - | - | - | TIM8_CH3 | TIM3_CH3 | - | - | - | - | SDIO_D0 | - | - | - | EVENT_OUT |
| PC9 | - | - | - | - | - | TIM8_CH4 | TIM3_CH4 | - | - | - | - | SDIO_D1 | - | - | - | EVENT_OUT |
| PC10 | - | USART4_TX | USART3_TX | - | - | - | - | - | - | - | - | SDIO_D2 | - | - | I2S1_CK | EVENT_OUT |
| PC11 | - | USART4_RX | USART3_RX | - | - | - | - | - | - | - | - | SDIO_D3 | - | - | I2S1_WS | EVENT_OUT |
| PC12 | - | USART5_TX | USART3_CK | - | - | - | - | - | - | - | - | SDIO_CK | - | - | I2S1_SD | EVENT_OUT |
| PC13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |

| PortC | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|-------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|------|------|-----------|
| PC14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PC15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |

3.4. Port D multiplexing function mapping

Table 3-6 Port D multiplexing function mapping

| PortD | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|-------|-----|------------|------------|-----|-----|-----|----------|----------|-----|-----|----------|----------|------|------|------|-----------|
| PD0 | - | - | - | - | - | - | - | - | - | - | CAN_RX | - | - | - | - | EVENT_OUT |
| PD1 | - | - | - | - | - | - | - | - | - | - | CAN_TX | - | - | - | - | EVENT_OUT |
| PD2 | - | USART5_RX | - | - | - | - | TIM3_ETR | - | - | - | - | SDIO_CMD | - | - | - | EVENT_OUT |
| PD3 | - | USART5_CK | USART2_CTS | - | - | - | - | - | - | - | ESMC_SS2 | - | - | - | - | EVENT_OUT |
| PD4 | - | USART5_CTS | USART2_RTS | - | - | - | - | - | - | - | ESMC_IO4 | - | - | - | - | EVENT_OUT |
| PD5 | - | USART5_RTS | USART2_TX | - | - | - | - | - | - | - | ESMC_IO5 | - | - | - | - | EVENT_OUT |
| PD6 | - | - | USART2_RX | - | - | - | - | - | - | - | ESMC_IO6 | - | - | - | - | EVENT_OUT |
| PD7 | - | - | USART2_CK | - | - | - | - | - | - | - | ESMC_IO7 | - | - | - | - | EVENT_OUT |
| PD8 | - | - | USART3_TX | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PD9 | - | - | USART3_RX | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PD10 | - | - | USART3_CK | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PD11 | - | - | USART3_CTS | - | - | - | - | TIM5_ETR | - | - | - | - | - | - | - | EVENT_OUT |
| PD12 | - | - | USART3_RTS | - | - | - | TIM4_CH1 | - | - | - | - | - | - | - | - | EVENT_OUT |
| PD13 | - | - | - | - | - | - | TIM4_CH2 | - | - | - | - | - | - | - | - | EVENT_OUT |
| PD14 | - | - | - | - | - | - | TIM4_CH3 | - | - | - | - | - | - | - | - | EVENT_OUT |
| PD15 | - | - | - | - | - | - | TIM4_CH4 | - | - | - | - | - | - | - | - | EVENT_OUT |

3.5. Port E multiplexing function mapping

Table 3-7 Port E multiplexing function mapping

| PortE | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|-------|-----|-----|-----|-----|-----|-----|----------|-----|-----|-----|------|------|------|------|------|-----------|
| PE0 | - | - | - | - | - | - | TIM4_ETR | - | - | - | - | - | - | - | - | EVENT_OUT |
| PE1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |

| PortE | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|-------|---------|-----|-----|-----|-----------|-----|-----|-----|----------|-----|----------|------|------|------|------|-----------|
| PE2 | TRACECK | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PE3 | TRACED0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PE4 | TRACED1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PE5 | TRACED2 | - | - | - | - | - | - | - | TIM9_CH1 | - | - | - | - | - | - | EVENT_OUT |
| PE6 | TRACED3 | - | - | - | - | - | - | - | TIM9_CH2 | - | - | - | - | - | - | EVENT_OUT |
| PE7 | - | - | - | - | TIM1_ETR | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PE8 | - | - | - | - | TIM1_CH1N | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PE9 | - | - | - | - | TIM1_CH1 | - | - | - | - | - | - | - | - | - | - | EVENT_OUT |
| PE10 | - | - | - | - | TIM1_CH2N | - | - | - | - | - | ESMC_CLK | - | - | - | - | EVENT_OUT |
| PE11 | - | - | - | - | TIM1_CH2 | - | - | - | - | - | ESMC_SS3 | - | - | - | - | EVENT_OUT |
| PE12 | - | - | - | - | TIM1_CH3N | - | - | - | - | - | ESMC_IO0 | - | - | - | - | EVENT_OUT |
| PE13 | - | - | - | - | TIM1_CH3 | - | - | - | - | - | ESMC_IO1 | - | - | - | - | EVENT_OUT |
| PE14 | - | - | - | - | TIM1_CH4 | - | - | - | - | - | ESMC_IO2 | - | - | - | - | EVENT_OUT |
| PE15 | - | - | - | - | TIM1_BKIN | - | - | - | - | - | ESMC_IO3 | - | - | - | - | EVENT_OUT |

4. Memory mapping

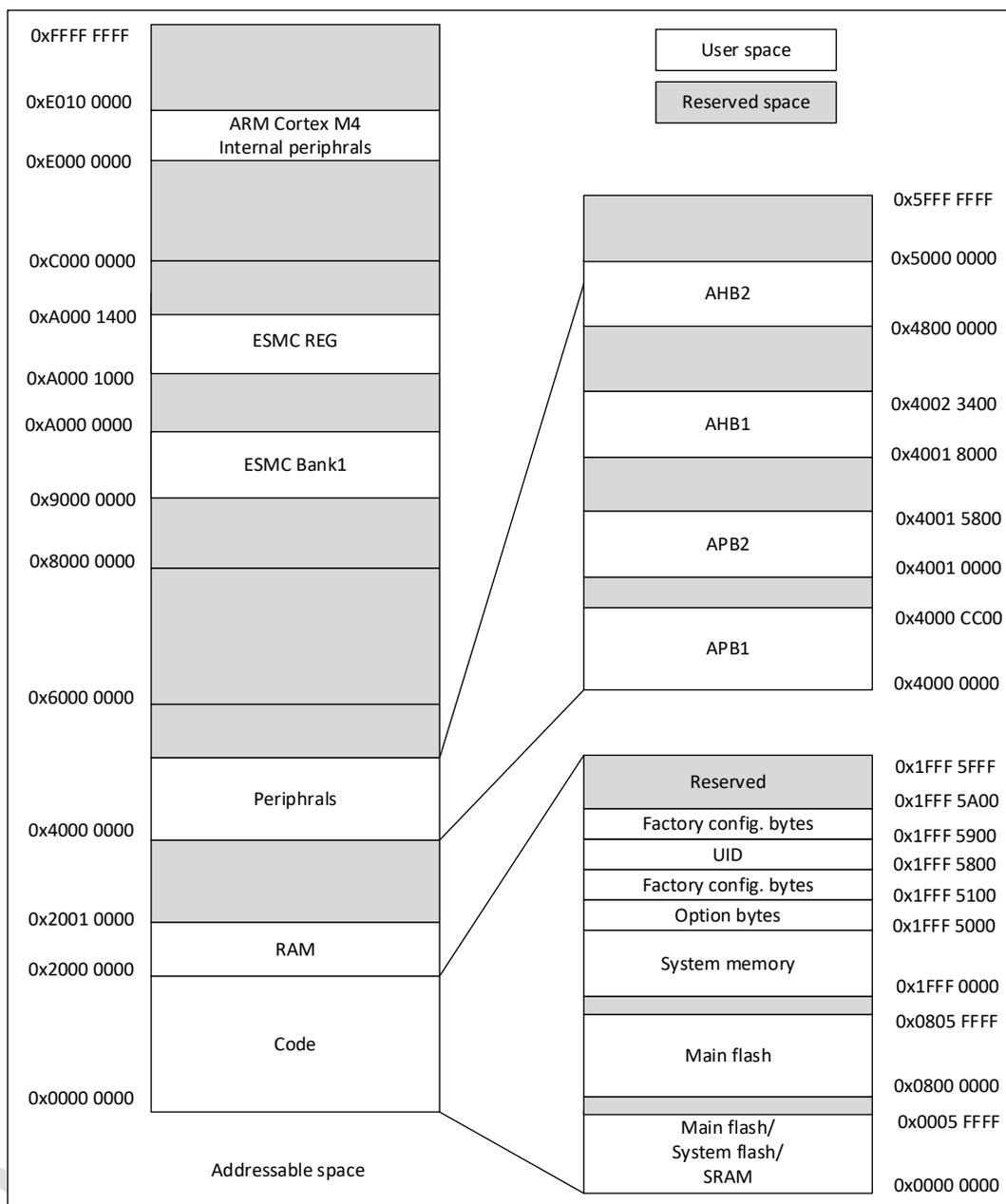


Figure 4-1 Memory Map

Table 4-1 Memory Address

| Type | Boundary Address | Size | Memory Area | Description |
|------|-------------------------|-----------|---|---|
| SRAM | 0x2001 0000-0x3FFF FFFF | - | Reserved | 1. Response error is generated when the CPU reads or writes to the space, which leads to a HardFault exception; 2. TEIF status bit is generated during DMA access; |
| | 0x2000 0000-0x2000 FFFF | 64 KB | SRAM | If the hardware power-up configures the SRAM to 64 KB, then the SRAM address space is 0x2000 0000-0x2000 FFFF |
| Code | 0x1FFF 5A00-0x1FFF 5FFF | - | Reserved | - |
| | 0x1FFF 5900-0x1FFF 59FF | 256 Bytes | Factory config. bytes | - |
| | 0x1FFF 5800-0x1FFF 58FF | 256 Bytes | UID bytes | Unique ID |
| | 0x1FFF 5700-0x1FFF 57FF | 256 Bytes | Factory config. bytes | - |
| | 0x1FFF 5600-0x1FFF 56FF | 256 Bytes | HSI8M Trim | - |
| | 0x1FFF 5500-0x1FFF 55FF | 256 Bytes | Factory config. bytes | - |
| | 0x1FFF 5400-0x1FFF 54FF | 256 Bytes | Factory config. bytes | - |
| | 0x1FFF 5300-0x1FFF 53FF | 256 Bytes | Factory config. bytes | - |
| | 0x1FFF 5200-0x1FFF 52FF | 256 Bytes | Factory config. bytes | - |
| | 0x1FFF 5100-0x1FFF 51FF | 256 Bytes | Factory config. bytes | - |
| | 0x1FFF 5000-0x1FFF 50FF | 256 Bytes | Option bytes | Chip hardware and software option bytes information; |
| | 0x1FFF 0000-0x1FFF 4FFF | 24 KB | System memory | Store the boot loader |
| | 0x0806 0000-0x1FFE FFFF | - | Reserved | - |
| | 0x0800 0000-0x0805 FFFF | 384 KB | Main flash memory | - |
| | 0x0006 0000-0x07FF FFFF | - | Reserved | 1. Response error is generated when the CPU reads or writes to the space, which leads to a HardFault exception; 2. TEIF status bit is generated during DMA access; |
| | 0x0000 0000-0x0005 FFFF | 384 KB | The choices according to Boot configuration are: 1) Main flash memory 2) System memory 3) SRAM | - |

1. Except for the above space, the rest of the space marked as reserved cannot be written, read as 0, and generate a response error.

Table 4-2 Peripheral register address

| Memory start and stop addresses | Peripherals | Bus | Register Map |
|---------------------------------|-------------|------|--------------|
| 0xA000 1000 - 0xA000 13FF | ESMC | AHB | - |
| 0x4002 3400 - 0x5FFF FFFF | Reserved | AHB2 | - |
| 0x4800 1000 - 0x4800 13FF | GPIOE | | - |
| 0x4800 0C00 - 0x4800 0FFF | GPIOD | | - |
| 0x4800 0800 - 0x4800 0BFF | GPIOC | | - |
| 0x4800 0400 - 0x4800 07FF | GPIOB | | - |
| 0x4800 0000 - 0x4800 03FF | GPIOA | | - |
| 0x4002 3400 - 0x47FF FFFF | Reserved | | AHB1 |
| 0x4002 3000 - 0x4002 33FF | CRC | - | |
| 0x4002 2400 - 0x4002 2FFF | Reserved | - | |
| 0x4002 2000 - 0x4002 23FF | FMC | - | |

| Memory start and stop addresses | Peripherals | Bus | Register Map |
|---------------------------------|----------------------------------|------|--------------|
| 0x4002 1400 - 0x4002 1FFF | Reserved | | - |
| 0x4002 1000 - 0x4002 13FF | RCC | | - |
| 0x4002 0800 - 0x4002 0FFF | Reserved | | - |
| 0x4002 0400 - 0x4002 07FF | DMA2 | | - |
| 0x4002 0000 - 0x4002 03FF | DMA1 | | - |
| 0x4001 8400 - 0x4001 FFFF | Reserved | | - |
| 0x4001 8000 - 0x4001 83FF | SDIO | | - |
| 0x4001 5800 - 0x4001 7FFF | Reserved | | - |
| 0x4001 5400 - 0x4001 57FF | TIMER11 | | - |
| 0x4001 5000 - 0x4001 53FF | TIMER10 | | - |
| 0x4001 4C00 - 0x4001 4FFF | TIMER9 | | - |
| 0x4001 4000 - 0x4001 4BFF | Reserved | | - |
| 0x4001 3C00 - 0x4001 3FFF | ADC3 | | - |
| 0x4001 3800 - 0x4001 3BFF | USART1 | | - |
| 0x4001 3400 - 0x4001 37FF | TIMER8 | APB2 | - |
| 0x4001 3000 - 0x4001 33FF | SPI1 | | - |
| 0x4001 2C00 - 0x4001 2FFF | TIMER1 | | - |
| 0x4001 2800 - 0x4001 2BFF | ADC2 | | - |
| 0x4001 2400 - 0x4001 27FF | ADC1 | | - |
| 0x4001 0800 - 0x4001 23FF | Reserved | | - |
| 0x4001 0400 - 0x4001 07FF | EXTI | | - |
| 0x4001 0000 - 0x4001 03FF | SYSCFG | | - |
| 0x4000 CC00 - 0x4000 FFFF | Reserved | | - |
| 0x4000 C800 - 0x4000 CBFF | CTC | | - |
| 0x4000 7800 - 0x4000 C7FF | Reserved | | - |
| 0x4000 7400 - 0x4000 77FF | Reserved | | - |
| 0x4000 7000 - 0x4000 73FF | PWR | | - |
| 0x4000 6C00 - 0x4000 6FFF | BKP | | - |
| 0x4000 6800 - 0x4000 6BFF | Reserved | | - |
| 0x4000 6400 - 0x4000 67FF | CANFD | | - |
| 0x4000 6000 - 0x4000 63FF | USBD/CANFD shared 512 Bytes SRAM | | - |
| 0x4000 5C00 - 0x4000 5FFF | USBD | | - |
| 0x4000 5800 - 0x4000 5BFF | I ² C2 | | - |
| 0x4000 5400 - 0x4000 57FF | I ² C1 | APB1 | - |
| 0x4000 5000 - 0x4000 53FF | UASRT5 | | - |
| 0x4000 4C00 - 0x4000 4FFF | UASRT4 | | - |
| 0x4000 4800 - 0x4000 4BFF | USART3 | | - |
| 0x4000 4400 - 0x4000 47FF | USART2 | | - |
| 0x4000 4000 - 0x4000 43FF | Reserved | | - |
| 0x4000 3C00 - 0x4000 3FFF | SPI3/I2S | | - |
| 0x4000 3800 - 0x4000 3BFF | SPI2/I2S | | - |
| 0x4000 3400 - 0x4000 37FF | Reserved | | - |
| 0x4000 3000 - 0x4000 33FF | IWDG | | - |
| 0x4000 2C00 - 0x4000 2FFF | WWDG | | - |
| 0x4000 2800 - 0x4000 2BFF | RTC | | - |
| 0x4000 2400 - 0x4000 27FF | Reserved | | - |

| Memory start and stop addresses | Peripherals | Bus | Register Map |
|---------------------------------|-------------|-----|--------------|
| 0x4000 2000 - 0x4000 23FF | TIMER14 | | - |
| 0x4000 1C00 - 0x4000 1FFF | TIMER13 | | - |
| 0x4000 1800 - 0x4000 1BFF | TIMER12 | | - |
| 0x4000 1400 - 0x4000 17FF | TIMER7 | | - |
| 0x4000 1000 - 0x4000 13FF | TIMER6 | | - |
| 0x4000 0C00 - 0x4000 0FFF | TIMER5 | | - |
| 0x4000 0800 - 0x4000 0BFF | TIMER4 | | - |
| 0x4000 0400 - 0x4000 07FF | TIMER3 | | - |
| 0x4000 0000 - 0x4000 03FF | TIMER2 | | - |

1. The above table AHB marked as Reserved address space, can not write operation, read back to 0, and generate hardfault.
2. Not only supports 32-bit word access, but also supports half-word and byte access.
3. Not only supports 32-bit word access, but also supports half-word access.

5. Electrical characteristics

5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

5.1.1. Minimum and maximum values

Unless otherwise specified, all devices have been tested during production at $T_A = 25\text{ °C}$ and $T_A = T_{Amax}$ (depending on the temperature range of the selected device) for minimum and maximum values that can be guaranteed under worst-case ambient temperature, supply voltage and clock frequency conditions.

The data based on characterization results, design simulations and/or technical characteristics are described in the footnotes of the tables and have not been tested in production. On the basis of the characterization, the minimum and maximum values are obtained by averaging the sample tests plus or minus three times the standard deviation (mean $\pm 3\sigma$).

5.1.2. Typical values

Unless otherwise noted, typical data is measured at $T_A = 25\text{ °C}$ and $V_{CC} = 3.3\text{ V}$ (for the $2.0\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ voltage range). These data are untested and are for design reference only.

Typical ADC accuracy values are determined by sampling a standard diffusion batch and performing a characterization over the entire temperature range, where 95% of the devices have an error less than or equal to the specified value (mean $\pm 2\sigma$).

5.2. Absolute maximum ratings

If the absolute maximum values given in the table below are exceeded, permanent damage to the chip may result. This is only a list of the strength levels that can be withstood, and does not mean that the device will function without error under these conditions. Prolonged operation at the maximum values may affect the reliability of the chip.

Table 5-1 Voltage Characteristics ⁽¹⁾

| Symbol | Description | Minimum | Maximum | Unit |
|--------------------|---|----------------|---------|------|
| $V_{CC}-V_{SS}$ | External power supply voltage (Including V_{CC} , V_{CCA} , V_{BAT}) ⁽¹⁾ | -0.3 | 4.0 | V |
| $V_{IN}^{(2)}$ | FT pin input voltage | $V_{SS} - 0.3$ | 5.5 | |
| | All other input pin input voltages | $V_{SS} - 0.3$ | 4.0 | |
| $ DV_{CCx} $ | Voltage variation between different V_{CC} pins | - | 50 | mV |
| $ V_{SSx}-V_{SS} $ | Voltage variation between different ground pins | - | 50 | |

1. The power V_{CC} and ground V_{SS} pins must always be connected to a supply system within the external allowable range.
2. The maximum value of V_{IN} must always follow the maximum allowed injected current value, as shown in the following table.

Table 5-2 Current Characteristics

| Symbol | Description | Maximum | Unit |
|-------------------------|---|----------|------|
| I_{VCC} | Total current flowing into all V_{CC} / V_{CCA} power lines (pull current) ⁽¹⁾ | 150 | mA |
| I_{VSS} | Total current flowing out of all V_{SS} grounding wires (irrigation current) ⁽¹⁾ | 150 | |
| I_{IO} | Output potting current for arbitrary I/O and control pins | 25 | |
| | Output pull current for arbitrary I/O and control pins | -25 | |
| $I_{INJ(PIN)}^{(2)(6)}$ | 5 V-tolerant pin injection current ⁽³⁾ | -5/+0 | |
| | All other pins inject current ⁽⁴⁾ | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current on all I/O and control pins ⁽⁵⁾ | ± 25 | |

1. The power V_{CC} and ground V_{SS} pins must always be connected to an external supply system within the allowed range.
2. The IO type can be referred to the terminology and symbols of the pin definition.
3. Reverse injection of current can interfere with the analog performance of the device.
4. Forward injection is not possible on these I/Os and will not occur when the input voltage is below a specified maximum.
5. Forward injection current occurs when $V_{IN} > V_{CCA}$; reverse injection current occurs when $V_{IN} < V_{SS}$.
6. When multiple inputs have simultaneous injection currents, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the sum of the absolute values of the forward injection current and the reverse injection current (instantaneous value).

Table 5-3 Temperature Characteristics

| Symbol | Description | Maximum | Unit |
|-----------|------------------------------|-----------|------|
| T_{STG} | Storage temperature range | -65 ~ 150 | °C |
| T_J | Maximum junction temperature | 150 | °C |

5.3. Operating conditions

5.3.1. General working conditions

Table 5-4 General working conditions

| Symbol | Parameter | Condition | Minimum | Maximum | Unit |
|-------------|----------------------------------|--|---------|---------|------|
| f_{HCLK} | AHB clock frequency | - | 0 | 144 | MHz |
| f_{PCLK1} | APB1 clock frequency | - | 0 | 144 | |
| f_{PCLK2} | APB2 clock frequency | - | 0 | 144 | |
| V_{CC} | Operating Voltage | - | 2.0 | 3.6 | V |
| V_{CCA} | Analog circuit operating voltage | Must be the same as V_{CC} | 2.0 | 3.6 | V |
| V_{BAT} | Backup section operating voltage | - | 2.0 | 3.6 | V |
| T_A | Environmental temperature | Maximum power consumption when operating | -40 | 85 | °C |
| | | Lowest power consumption operation | -40 | 105 | |
| T_J | Junction temperature range | Maximum power consumption when operating | -40 | 90 | °C |
| | | Lowest power consumption operation | -40 | 110 | |

5.3.2. Operating conditions at power-up / power-down

Table 5-5 Operating conditions at power-up / power-down

| Symbol | Parameter | Condition | Minimum | Maximum | Unit |
|-----------|-------------------------|---|---------|----------|-----------------|
| t_{VCC} | V_{CC} rise time rate | - | 0 | ∞ | $\mu\text{s/V}$ |
| | V_{CC} fall time rate | V_{CC} , V_{BAT} drop synchronously | 20 | ∞ | |
| | | V_{CC} drops, V_{BAT} holds | 100 | ∞ | |

5.3.3. Reset and voltage control module features

Table 5-6 Reset and voltage control module features

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Unit |
|-----------------------------|---|-----------------------------|---------|---------|---------|------|
| V_{PVD} | Programmable voltage detector level selection | PLS[2:0]=000 (Rising edge) | 1.7 | 1.8 | 1.9 | V |
| | | PLS[2:0]=000 (Falling edge) | 1.6 | 1.7 | 1.8 | V |
| | | PLS[2:0]=001 (Rising edge) | 1.9 | 2 | 2.1 | V |
| | | PLS[2:0]=001 (Falling edge) | 1.8 | 1.9 | 2 | V |
| | | PLS[2:0]=010 (Rising edge) | 2.1 | 2.2 | 2.3 | V |
| | | PLS[2:0]=010 (Falling edge) | 2 | 2.1 | 2.2 | V |
| | | PLS[2:0]=011 (Rising edge) | 2.3 | 2.4 | 2.5 | V |
| | | PLS[2:0]=011 (Falling edge) | 2.2 | 2.3 | 2.4 | V |
| | | PLS[2:0]=100 (Rising edge) | 2.5 | 2.6 | 2.7 | V |
| | | PLS[2:0]=100 (Falling edge) | 2.4 | 2.5 | 2.6 | V |
| | | PLS[2:0]=101 (Rising edge) | 2.7 | 2.8 | 2.9 | V |
| | | PLS[2:0]=101 (Falling edge) | 2.6 | 2.7 | 2.8 | V |
| | | PLS[2:0]=110 (Rising edge) | 2.9 | 3 | 3.1 | V |
| | | PLS[2:0]=110 (Falling edge) | 2.8 | 2.9 | 3 | V |
| | | PLS[2:0]=111 (Rising edge) | 3.1 | 3.2 | 3.3 | V |
| PLS[2:0]=111 (Falling edge) | 3 | 3.1 | 3.2 | V | | |
| $V_{PVDhyst}^{(1)}$ | PVD hysteresis | - | - | 100 | - | mV |
| $V_{POR/PDR}$ | Power-up/power-down reset threshold | Falling edge | 1.58 | 1.63 | 1.68 | V |
| | | Rising edge | 1.56 | 1.61 | 1.66 | V |
| $V_{PDRhyst}^{(1)}$ | PDR hysteresis | - | - | 20 | - | mV |
| $T_{RSTTEMPO}^{(2)}$ | Reset duration | - | 1 | 2.5 | 4.5 | ms |

1. Guaranteed by design, not tested in production.
2. Reset duration is measured from power-up (POR reset or wake-up from V_{BAT}) to the moment the first instruction is read by the user application code.

5.3.4. Operating current characteristics

Current consumption is affected by several parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switching rate, location of the program in memory, and the code executed. Current consumption measurements for the various modes of operation described in this section are derived from a streamlined set of code.

Maximum current consumption

The microcontroller is in the following conditions:

- All I/O pins are in input mode with static values (no load) on V_{CC} or V_{SS} .

- All peripherals are off, unless otherwise noted.
- Flash memory access time is adjusted to the frequency of f_{HCLK} (0 wait cycles at 0 ~ 28 MHz, 1 wait cycle at 28 ~ 60 MHz, 3 wait cycles at 60 ~ 90 MHz, 4 wait cycles at 90 ~ 120 MHz, 5 wait cycles at 120 ~ 140 MHz, and 6 wait cycles at greater than 140 MHz).
- Unless otherwise noted, V_{CC} = 3.6 V, maximum at maximum ambient temperature (T_A), typical value is T_A = 25°C and V_{CC} = 3.3 V.
- Command Prefetch is on. When the peripheral is on: f_{PCLK1} = f_{HCLK}.

Note: The command prefetch function must be set before setting the clock and bus divider.

Table 5-7 Flash down operation mode current

| Symbol | Parameter | Condition | Frequency f _{HCLK} | Typical | Maximum ⁽¹⁾ | | Unit |
|-----------------|----------------------------------|--|--------------------------------|-----------------------|------------------------|------------------------|------|
| | | | | T _A = 25°C | T _A = 85°C | T _A = 105°C | |
| I _{CC} | Supply current in operation mode | External clock ⁽²⁾ , All peripheral enable , Flash operation | 144 MHz | 25.60 | - | - | mA |
| | | | 96 MHz | 18.24 | - | - | |
| | | | 64 MHz | 13.20 | - | - | |
| | | | 48 MHz | 11.32 | - | - | |
| | | | 32 MHz | 8.31 | - | - | |
| | | | 16 MHz | 5.43 | - | - | |
| | | | 8 MHz | 1.99 | - | - | |
| | | External clock ⁽²⁾ , All peripherals disabled, Flash running | 144 MHz | 15.09 | - | - | |
| | | | 96 MHz | 11.07 | - | - | |
| | | | 64 MHz | 8.37 | - | - | |
| | | | 48 MHz | 7.50 | - | - | |
| | | | 32 MHz | 5.71 | - | - | |
| | | | 16 MHz | 3.91 | - | - | |
| | | | 8 MHz | 1.35 | - | - | |

Table 5-8 Operating mode current under SRAM

| Symbol | Parameter | Condition ⁽³⁾ | Frequency f _{HCLK} | Typical | Maximum ⁽¹⁾ | | Unit |
|-----------------|----------------------------------|--|--------------------------------|-----------------------|------------------------|------------------------|------|
| | | | | T _A = 25°C | T _A = 85°C | T _A = 105°C | |
| I _{CC} | Supply current in operation mode | External clock ⁽²⁾ , All peripheral enable | 144 MHz | 24.61 | - | - | mA |
| | | | 96 MHz | 17.55 | - | - | |
| | | | 64 MHz | 12.78 | - | - | |
| | | | 48 MHz | 10.83 | - | - | |
| | | | 32 MHz | 7.99 | - | - | |
| | | | 16 MHz | 3.92 | - | - | |
| | | | 8 MHz | 2.09 | - | - | |
| | | External clock ⁽²⁾ , All peripherals disabled | 144 MHz | 14.39 | - | - | |
| | | | 96 MHz | 10.68 | - | - | |
| | | | 64 MHz | 8.07 | - | - | |
| | | | 48 MHz | 7.33 | - | - | |
| | | | 32 MHz | 5.65 | - | - | |
| | | | 16 MHz | 2.68 | - | - | |
| | | | 8 MHz | 1.49 | - | - | |

1. Derived from feature evaluation, not tested in production.
2. External clock is 16 MHz and PLL is enabled when f_{HCLK} > 8 MHz.

3. 8 MHz is the internal HSI clock.

Table 5-9 sleep mode current

| Symbol | Parameter | Condition | Frequency f_{HCLK} | Maximum ⁽¹⁾ | | | Unit |
|----------|-------------------------|--|-------------------------|-------------------------------------|--------------------------|---------------------------|------|
| | | | | Typical $T_A = 25^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ | $T_A = 105^\circ\text{C}$ | |
| I_{CC} | Sleep mode power supply | External clock, All peripheral enable | 144 MHz | 19.37 | - | - | mA |
| | | | 96 MHz | 14.07 | - | - | |
| | | | 64 MHz | 10.44 | - | - | |
| | | | 48 MHz | 7.21 | - | - | |
| | | | 32 MHz | 5.45 | - | - | |
| | | | 16 MHz | 3.32 | - | - | |
| | | | 8 MHz | 1.82 | - | - | |
| | | External clock, All peripherals disabled | 144 MHz | 6.60 | - | - | |
| | | | 96 MHz | 4.98 | - | - | |
| | | | 64 MHz | 3.95 | - | - | |
| | | | 48 MHz | 3.41 | - | - | |
| | | | 32 MHz | 2.86 | - | - | |
| | | | 16 MHz | 1.95 | - | - | |
| | | | 8 MHz | 1.07 | - | - | |

1. The data is based on assessment results and is not tested in production.

Table 5-10 Shutdown and standby mode current

| Symbol | Parameter | Condition | Typical ⁽¹⁾ | | | Maximum ⁽²⁾ | | Unit |
|----------|-----------------------------------|--|---------------------------------|---------------------------------|---------------------------------|--------------------------|---------------------------|------|
| | | | $V_{CC}/V_{BAT} = 2.0\text{ V}$ | $V_{CC}/V_{BAT} = 2.4\text{ V}$ | $V_{CC}/V_{BAT} = 3.3\text{ V}$ | $T_A = 85^\circ\text{C}$ | $T_A = 105^\circ\text{C}$ | |
| I_{CC} | Shutdown mode supply current | LDO operation mode, internal high-speed oscillator, internal low-speed oscillator and high-speed oscillator off, $f_{CK} = 8\text{ MHz}$ | 432.00 | - | - | - | - | uA |
| | | LDO low power mode, internal high speed oscillator, internal low speed oscillator and high speed oscillator off | 370.00 | - | - | - | - | |
| | Standby mode power supply current | Internal low-speed oscillator and IWDG on | 4.80 | - | - | - | - | |
| | | Internal low-speed oscillator on, IWDG off | 4.80 | - | - | - | - | |
| | | Internal low-speed RC oscillator and IWDG off, low-speed oscillator and RTC off | 4.70 | - | - | - | - | |
| | I_{CC_VBAT} | Backup domain power supply current | Low-speed oscillator and RTC on | 4.80 | - | - | - | |

1. Typical values are tested at $T_A = 25^\circ\text{C}$.

- Derived from characterization, not tested in production.

5.3.5. Low power mode wake-up time

Table 5-11 Low power mode wake-up time⁽²⁾

| Symbol | Parameter | Typ ⁽³⁾ | Unit |
|---------------------|---|--------------------|---------|
| $t_{WUSLEEP}^{(1)}$ | Wake up from sleep mode | 3.20 | μs |
| $t_{WUSTOP}^{(1)}$ | Wake-up from shutdown mode (LDO operation mode) | 6.88 | μs |
| | Wake-up from shutdown mode (LDO low-power mode) | 10.66 | |
| $t_{WUSTDBY}^{(1)}$ | Wake up from standby mode | 79.50 | μs |

- The wake-up time is measured from the start of the wake-up time until the first instruction is read by the user program.
- The data is based on the test results and is not tested in production.
- Test data is based on HSI 8 M conditions.

5.3.6. External clock source characteristics

5.3.6.1. External high-speed clock

In the bypass mode of HSE (HSEBYP of RCC_CR is set), the high-speed oscillation circuit inside the chip stops working, and the corresponding IOs are used as standard GPIO.

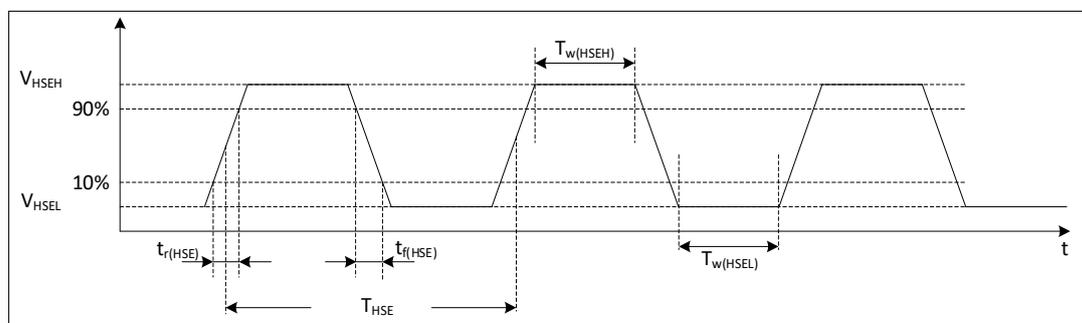


Figure 5-1 External high-speed clock timing diagram

Table 5-12 External high-speed clock characteristics

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Unit |
|-------------------------|---|----------------------------------|--------------|---------|--------------|---------|
| f_{HSE_ext} | User external clock frequency ⁽¹⁾ | | 4 | 8 | 32 | MHz |
| V_{HSEH} | OSC_IN input pin high level voltage | | $0.7 V_{CC}$ | - | V_{CC} | V |
| V_{HSEL} | OSC_IN input pin low level voltage | - | V_{SS} | - | $0.3 V_{CC}$ | |
| $t_{w(HSE)}$ | OSC_IN input pin high low time ⁽¹⁾ | | 5 | - | - | ns |
| $t_{r(HSE)}/t_{f(HSE)}$ | OSC_IN input pin rise or fall time ⁽¹⁾ | | - | - | 20 | |
| $C_{in(HSE)}$ | OSC_IN input pin capacitance ⁽¹⁾ | - | - | 5 | - | pF |
| DuCy _(HSE) | Duty Cycle | - | 45 | - | 55 | % |
| I_L | OSC_IN input pin leakage current | $V_{SS} \leq V_{IN} \leq V_{CC}$ | - | - | ± 1 | μA |

1. Guaranteed by design, not tested in production.

5.3.6.2. External low-speed clock

In the bypass mode of LSE (LSEBYP of RCC_BDCR is set), the low-speed start circuit in the chip stops working and the corresponding IOs are used as standard GPIO.

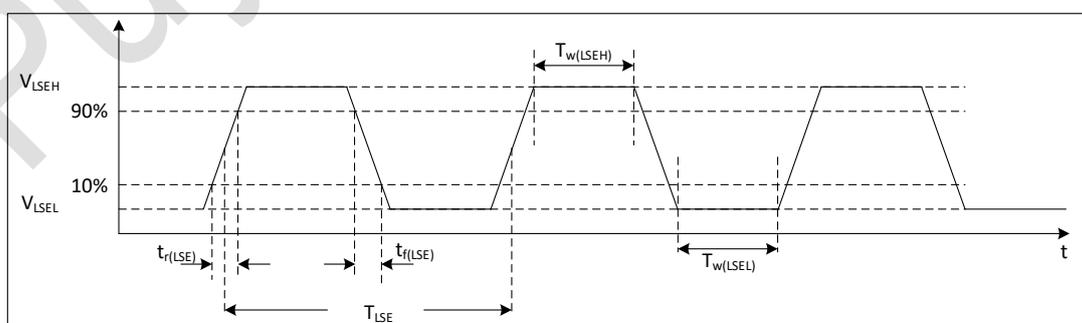


Figure 5-2 External low-speed clock timing diagram

Table 5-13 External low-speed clock characteristics

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Unit |
|-------------------------|---|----------------------------------|--------------|---------|--------------|---------|
| f_{LSE_ext} | User external clock frequency ⁽¹⁾ | - | - | 32.768 | 1000 | kHz |
| V_{LSEH} | OSC32_IN input pin high level voltage | | $0.7 V_{CC}$ | - | V_{CC} | V |
| V_{LSEL} | OSC32_IN input pin low level voltage | | V_{SS} | - | $0.3 V_{CC}$ | |
| $t_{w(LSE)}$ | OSC32_IN input pin high low time ⁽¹⁾ | | 450 | - | - | ns |
| $t_{r(LSE)}/t_{f(LSE)}$ | OSC32_IN input pin rise or fall time ⁽¹⁾ | | - | - | 50 | |
| $C_{in(LSE)}$ | OSC32_IN input pin capacitance ⁽¹⁾ | - | - | 5 | - | pF |
| DuCy _(LSE) | Duty Cycle | - | 30 | - | 70 | % |
| I_L | OSC32_IN input pin leakage current | $V_{SS} \leq V_{IN} \leq V_{CC}$ | - | - | ± 1 | μA |

1. Guaranteed by design, not tested in production.

5.3.6.3. External high-speed crystal

This can be done with an external 32 MHz crystal/ceramic resonator. In this application, the crystal and load capacitor should be as close to the pin as possible to minimize output distortion and start-up stabilization time.

Table 5-14 External high-speed crystal characteristics

| Symbol | Parameter | Condition | Minimum | Typical ⁽¹⁾ | Maximum | Unit | |
|---------------------|-------------------------|---------------------------------------|-----------------|------------------------|---------|------------|------|
| f_{OSC_IN} | Oscillator frequency | - | 4 | 8 | 32 | MHz | |
| R_F | Feedback Resistor | - | - | 200 | - | k Ω | |
| I_{CC} | HSE power consumption | CL=12 pF, 32 MHz , HSE_DRV[1:0]=01 | - | - | 1 | mA | |
| g_m | Oscillator Transduction | Start up | HSE_DRV[1:0]=00 | 3.5 | - | - | mA/V |
| | | | HSE_DRV[1:0]=01 | 5 | - | - | |
| | | | HSE_DRV[1:0]=10 | 7.5 | - | - | |
| | | | HSE_DRV[1:0]=11 | 10 | - | - | |
| $t_{SU(HSE)}^{(2)}$ | Startup time | V_{CC} is stable | - | 0.7 | - | ms | |

1. Given by characteristic evaluation, not tested in production.
2. The relatively low RF resistance value provides better protection against problems due to inductive leakage and changes in bias conditions when used in humid environments. However, it is recommended to take this parameter into account when designing the MCU if it is to be used in harsh humidity conditions.

5.3.6.4. External low-speed crystal

This can be done with an external 32.768 kHz crystal/ceramic resonator. In this application, the crystal and load capacitor should be as close to the pin as possible to minimize output distortion and start-up stabilization time.

Table 5-15 External low-speed crystal characteristics

| Symbol | Parameter | Condition | Minimum | Typical ⁽¹⁾ | Maximum | Unit |
|-------------------------------------|-------------------------|---------------------------|---------|------------------------|---------|------|
| RF | Feedback Resistor | - | - | 5 | - | MΩ |
| I _{CC} | LSE current consumption | LSE_DRV_VBKP[1:0]=00 | - | 500 | - | nA |
| | | LSE_DRV_VBKP[1:0]=01 | - | 630 | - | |
| | | LSE_DRV_VBKP[1:0]=10 | - | 250 | - | |
| | | LSE_DRV_VBKP[1:0]=11 | - | 315 | - | |
| g _m | Oscillator Transduction | LSE_DRV_VBKP[1:0]=00 | 8.5 | - | - | μA/V |
| | | LSE_DRV_VBKP[1:0]=01 | 13.5 | - | - | |
| | | LSE_DRV_VBKP[1:0]=10 | 2.5 | - | - | |
| | | LSE_DRV_VBKP[1:0]=11 | 3.75 | - | - | |
| t _{SU(LSE)} ⁽²⁾ | Startup time | V _{CC} is stable | - | 0.5 | - | s |

1. Guaranteed by design, not tested in production.
2. The data is based on assessment results and is not tested in production.

5.3.7. Internal high frequency clock source HSI characteristics

Table 5-16 Internal high frequency clock source characteristics

| Symbol | Parameter | Condition | Minimum (1) | Typical (1) | Maximum (1) | Unit | |
|-------------------------------------|----------------------------------|--|-------------------------------|----------------|------------------|------|---|
| f _{HSI} | Frequency | - | 7.96 | 8 | 8.04 | MHz | |
| DuCy _(HSI) | Duty Cycle | - | 45 | - | 55 | % | |
| ACC _{HSI} | HSI Oscillator Accuracy | User adjustment using RCC_CR register ⁽²⁾ | - | 0.5 | 1 ⁽³⁾ | % | |
| | | Factory calibration ⁽⁴⁾ | T _A = -40 ~ 105 °C | - | - | | - |
| | | | T _A = -10 ~ 85 °C | -2 | - | | 2 |
| | | | T _A = 0 ~ 70 °C | - | - | | - |
| | T _A = 25 °C | -1 | - | 1 | | | |
| t _{SU(HSI)} ⁽³⁾ | HSI oscillator startup time | - | 1 | - | 2 | μs | |
| I _{CC(HSI)} ⁽³⁾ | HSI oscillator power consumption | - | - | 80 | 150 | μA | |

1. Guaranteed by design, not tested in production.
2. V_{CC} = 3.3 V, T_A = -40 ~ 105 °C, unless otherwise noted.
3. Data is based on test results and is not tested in production.

5.3.8. Internal low frequency clock source LSI characteristics

Table 5-17 Internal low frequency clock source LSI characteristics

| Symbol | Parameter | Minimum ⁽¹⁾ | Typical ⁽¹⁾ | Maximum ⁽¹⁾ | Unit |
|-------------------------------------|----------------------------------|------------------------|------------------------|------------------------|------|
| f _{LSI} ⁽²⁾ | Frequency | 30 | 40 | 60 | kHz |
| t _{SU(LSI)} ⁽³⁾ | LSI oscillator startup time | - | - | 85 | μs |
| I _{CC(LSI)} ⁽³⁾ | LSI oscillator power consumption | - | 0.2 | 0.3 | μA |

1. Guaranteed by design, not tested in production.
2. V_{CC} = 3.3 V, T_A = -40 ~ 105 °C, unless otherwise noted.
3. Data is based on test results and is not tested in production.

5.3.9. Phase locked loop (PLL) characteristics

Table 5-18 Phase locked loop characteristics

| Symbol | Parameter | Minimum | Typical | Maximum ⁽¹⁾ | Unit |
|----------------|-----------------------------|---------|---------|------------------------|---------|
| f_{PLL_IN} | PLL input clock | 8 | 24 | 25 | MHz |
| | PLL input clock duty cycle | 40 | - | 60 | % |
| f_{PLL_OUT} | PLL multiplier output clock | 48 | - | 144 | MHz |
| t_{LOCK} | PLL phase lock time | - | 25 | 550 | μ s |
| Jitter | Jittering | - | - | 180 | ps |

1. Guaranteed by design, not tested in production.

5.3.10. Memory characteristics

Table 5-19 Memory characteristics

| Symbol | Parameter | Condition | Minimum ⁽¹⁾ | Typical ⁽¹⁾ | Maximum | Unit |
|--------------|---------------------------|---|------------------------|------------------------|---------|---------|
| PE_{CYC} | Number of erasures | $T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$ | 100 | - | - | kcycles |
| t_{RET} | Data retention time | $T_A = 85^\circ\text{C}$, after 1000 erasures | 20 | - | - | years |
| | | $T_A = 105^\circ\text{C}$, after 1000 erasures | 10 | - | - | |
| | | $T_A = 55^\circ\text{C}$, after 10000 erasures | 10 | - | - | |
| t_{PROG} | Page programming time | $T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$ | - | 1.5 | - | ms |
| t_{ERASE} | Page erase time | $T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$ | - | 5 | - | ms |
| t_{MERASE} | Full chip erase over time | $T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$ | - | 5 | - | ms |

1. Guaranteed by design, not tested in production.

5.3.11. ESMC characteristics

Table 5-20 ESMC characteristics in SDR mode ⁽¹⁾

| Symbol | Parameter | Condition | Minimum ⁽¹⁾ | Typical | Maximum ⁽¹⁾ | Unit |
|--------------|-----------------------------|--------------------------------|------------------------|---------|------------------------|------|
| F(QCK) | SPI clock frequency | $2.0 < V_{CC} < 3.6 \text{ V}$ | - | - | 70 | MHz |
| $t_{w(CKH)}$ | SPI clock high and low time | $2.0 < V_{CC} < 3.6 \text{ V}$ | $t_{CK}/2-0.5$ | - | $t_{CK}/2+1$ | ns |
| $t_{w(CKL)}$ | | | $t_{CK}/2-1$ | - | $t_{CK}/2+0.5$ | |
| $t_{s(IN)}$ | Data input setup time | $2.0 < V_{CC} < 3.6 \text{ V}$ | 1 | - | - | |
| $t_{h(IN)}$ | Data input hold time | $2.0 < V_{CC} < 3.6 \text{ V}$ | 5 | - | - | |
| $t_{v(OUT)}$ | Data output valid time | $2.0 < V_{CC} < 3.6 \text{ V}$ | - | 1 | 1.5 | |
| $t_{h(OUT)}$ | Data output hold time | $2.0 < V_{CC} < 3.6 \text{ V}$ | 0.5 | - | - | |

1. Given by characterization, not tested in production.

Table 5-21 ESMC characteristics in DDR mode ⁽¹⁾

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Unit |
|--------------|---------------------------------------|--------------------------------|----------------|---------|----------------|------|
| F(QCK) | SPI clock frequency | $2.0 < V_{CC} < 3.6 \text{ V}$ | - | - | 70 | MHz |
| $t_{w(CKH)}$ | SPI clock high and low time | $2.0 < V_{CC} < 3.6 \text{ V}$ | $t_{CK}/2-0.5$ | - | $t_{CK}/2+1$ | ns |
| $t_{w(CKL)}$ | | | $t_{CK}/2-1$ | - | $t_{CK}/2+0.5$ | |
| $t_{sr(IN)}$ | Data input setup time on rising edge | $2.0 < V_{CC} < 3.6 \text{ V}$ | 2 | - | - | |
| $t_{sf(IN)}$ | Data input setup time on falling edge | $2.0 < V_{CC} < 3.6 \text{ V}$ | 2 | - | - | |
| $t_{hr(IN)}$ | Data input hold time on rising edge | $2.0 < V_{CC} < 3.6 \text{ V}$ | 5 | - | - | |

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Unit |
|---------------|--|------------------------|---------|---------|---------|------|
| $t_{hf(IN)}$ | Data input hold time on falling edge | $2.0 < V_{CC} < 3.6 V$ | 5 | - | - | |
| $t_{vr(OUT)}$ | Data output valid time on rising edge | $2.0 < V_{CC} < 3.6 V$ | - | - | 9 | |
| $t_{vf(OUT)}$ | Data output valid time on falling edge | $2.0 < V_{CC} < 3.6 V$ | - | - | 11 | |
| $t_{hr(OUT)}$ | Data output hold time rising edge | $2.0 < V_{CC} < 3.6 V$ | 2 | - | - | |
| $t_{hf(OUT)}$ | Data output hold time falling edge | $2.0 < V_{CC} < 3.6 V$ | 3 | - | - | |

1. Given by characterization, not tested in production.

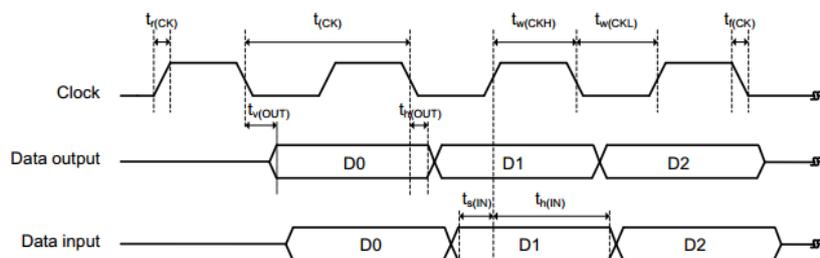


Figure 5-3 ESMC timing diagram – SDR mode

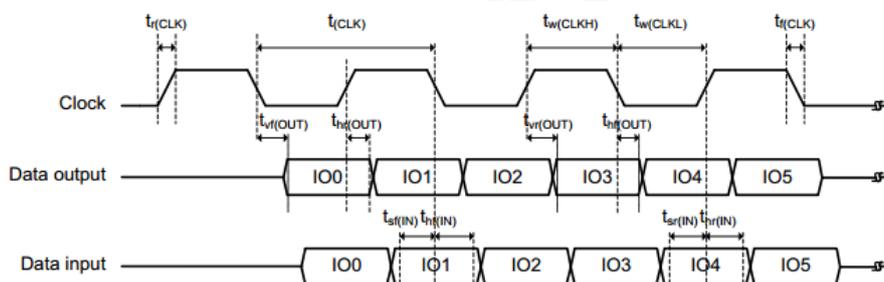


Figure 5-4 ESMC timing diagram – DDR mode2

5.3.12. EMC characteristics

Sensitivity testing is conducted on a sample basis during product characteristic evaluation

EMS (Electromagnetic sensitivity)

When running a simple application (flashing 2 LEDs through the I/O port), the test sample is subjected to 2 types of electromagnetic interference until an error is generated, and the flashing LEDs indicate the generation of the error.

- Electrostatic discharge (ESD) (positive and negative discharge): applied to all pins of the chip until a functional error is generated. This test complies with IEC61000-4-2 standard.
- FTB: A pulse train of transient voltages (forward and reverse) is applied to V_{CC} and V_{SS} through a 100 pF capacitor until a functional error is generated. This test is in accordance with IEC61000-4-4.

A chip reset can restore the system to normal operation.

The test results are listed in the table below. This is a test based on the level and type of EMS defined by AN.

Table 5-22 EMC characteristics

| Symbol | Parameter | Condition | Level / Type |
|------------|--|--|--------------|
| V_{FESD} | Voltage limits applied to any I/O pins that cause functional interference | $V_{CC} = 3.3\text{ V}$, $T_A = +25\text{ }^\circ\text{C}$, $f_{HCLK} = 144\text{ MHz}$, Compliant with IEC 61000-4-2 standard | 2 A |
| V_{FTB} | Fast transient pulse voltage limits applied through 100 pF capacitors on the V_{CC} and V_{SS} pins that cause functional errors | $V_{CC} = 3.3\text{ V}$, $T_A = +25\text{ }^\circ\text{C}$, $f_{HCLK} = 144\text{ MHz}$, Compliant with IEC 61000-4-4 standard | 4 A |

Design solid software to avoid noise problems

The evaluation and optimization of EMC at the device level is performed in a typical application environment. It should be noted that good EMC performance is closely related to the user application and the specific software. Therefore, it is recommended that users implement EMC optimization of the software and perform EMC-related certification tests.

Software suggestions

The flow of the software must contain controls for program runaway, e.g:

- Corrupted program counter
- Unexpected reset
- Corrupted critical data (control registers, etc...)

Pre-certification experiments

Many common failures (unexpected resets and corrupted program counters) can be reproduced by manually introducing a low level on the NRST or a low level on the crystal pin that lasts for 1 second. When performing ESD tests, voltages beyond the application requirements can be applied directly to the chip, and where unexpected actions are detected, the software part needs to be enhanced to prevent unrecoverable errors from occurring.

EMI (Electromagnetic Interference)

The electromagnetic fields emitted by the device are monitored when performing a simple application (switching 2 LEDs through I/O ports). The test complies with the IEC 61967-2 standard, which specifies the test board and pin load.

Table 5-23 EMICharacteristics

| Symbol | Parameter | Condition | Monitoring band | Max vs. [f_{HSE}/f_{HCLK}] | | | Unit |
|-----------|------------|--|-----------------|--------------------------------|----------|-----------|------------|
| | | | | 8/48 MHz | 8/72 MHz | 8/108 MHz | |
| S_{EMI} | Peak value | $V_{CC} = 3.3\text{ V}$, $T_A = +25\text{ }^\circ\text{C}$, Compliant with IEC 61967-2 standard | 0.1 ~ 2 MHz | - | - | - | dB μ V |
| | | | 2 ~ 30 MHz | - | - | - | |
| | | | 30 ~ 130 MHz | - | - | - | |
| | | | 130 MHz ~ 1GHz | - | - | - | |

5.3.13. ESD & LU characteristics

Based on three different tests (ESD, LU), stress tests are applied to the chip using specific measurement methods to determine its performance in terms of electrical sensitivity.

Table 5-24 ESD 特性

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Unit |
|----------------|--|---|---------|---------|-----------|------|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human model) | $T_A=25\text{ }^\circ\text{C}$; JESD22- A114 | - | - | 4000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charged device model) | $T_A=25\text{ }^\circ\text{C}$; JESD22-C101 | - | - | 1000 | V |
| LU | Overcurrent test | $T_A=25\text{ }^\circ\text{C}$; JESD78A | - | - | ± 200 | mA |
| | Overpressure test | | - | - | 5.4 | V |

5.3.14. I/O current injection characteristics

As a general rule, current injection into I/O pins due to external voltages below V_{SS} or above V_{CC} (for standard, 3 V I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in case of abnormal injection accidents, sampling is done during device characterization tests.

Functional sensitivity to I/O current injection

When executing simple applications on the device, stress the device by injecting current into I/O pins configured for input float mode. When current is injected into I/O pins (one at a time), the device is checked for functional faults.

Faults are indicated by out-of-range parameters: ADC errors above a certain limit (>5 LSB TUE), current injection on adjacent pins out of specification, or other functional faults (e.g., reset, oscillator frequency deviation).

Table 5-25 I/O current injection sensitivity

| Symbol | Parameter | Functional sensitivity | | Unit |
|-----------|--|----------------------------|----------------------------|------|
| | | Negative current injection | Positive current injection | |
| I_{INJ} | Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13 pins | 0 | 0 | mA |
| | Injected current on all 5 V tolerance pins | -5 | 0 | |
| | Injected current on all other pins | -5 | 5 | |

5.3.15. EFT characteristics

Table 5-26 EFT characteristics

| Symbol | Parameter | Condition | Level | Typical value | Unit |
|--------------|-----------|--------------|-------|---------------|------|
| EFT to Power | - | IEC61000-4-4 | A | 4 | kV |

5.3.16. Port characteristics

Table 5-27 IO Port Characteristics

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Unit |
|---------------------------------|---|---|----------------------------|---------|----------------------------|------|
| V _{IL} | Standard I/O input low | 2.0 V ≤ V _{CC} ≤ 3.6 V | -0.3 | - | 0.35 V _{CC} -0.06 | V |
| | 5 V-tolerant I/O input low | 2.0 V ≤ V _{CC} ≤ 3.6 V | -0.3 | - | 0.4 V _{CC} -0.04 | V |
| V _{IH} | Standard I/O input high | 2.0 V ≤ V _{CC} ≤ 3.6 V | 0.6 V _{CC} +0.14 | - | V _{CC} +0.3 | V |
| | 5 V-tolerant I/O input high | 2.0 V ≤ V _{CC} ≤ 3.6 V | 0.45 V _{CC} +0.13 | - | 5.5 | V |
| V _{hys} ⁽¹⁾ | Standard I/O Schmitt voltage hysteresis | - | 200 | - | - | mV |
| | 5 V-tolerant I/O Schmitt voltage hysteresis | - | 5% V _{CC} | - | - | mV |
| V _{Ikg} ⁽²⁾ | Input leakage current | V _{SS} ≤ V _{IN} ≤ V _{CC} | - | - | -1 | μA |
| | | Standard I/O | - | - | - | |
| | | V _{IN} = 5 V, | - | - | 3 | μA |
| | | 5 V-tolerant I/O | - | - | - | |
| R _{PU} ⁽³⁾ | Internal pull-up resistor | V _{IN} = V _{SS} | 30 | 40 | 50 | kΩ |
| R _{PD} ⁽³⁾ | Internal pull-down resistor | V _{IN} = V _{CC} | 30 | 40 | 50 | kΩ |
| C _{IO} | I/O pin capacitance | - | - | 5 | - | pF |

1. Guaranteed by design, not tested in production.
2. If there is reverse current backflow on adjacent pins, the leakage current may be higher than the maximum value.
3. The pull-up and pull-down resistors are designed to be implemented as a true resistor in series with a switchable PMOS/NMOS.

Output drive current

GPIO (General Purpose Input/Output Port) can absorb or output up to ±8 mA of current or up to ±20 mA of current (subject to relaxed V_{OL}/V_{OH} specifications.) The three pins PC13, PC14, and PC15 can only absorb or output ±3 mA of current. When PC13, PC14, and PC15 are used as output functions, the I/O speed cannot exceed 2 MHz at an output load of 30 pF.

In user applications, the number of I/O pins must be such that the drive current cannot exceed the absolute maximum rating given by the absolute maximum rating of:

- The sum of the currents drawn from V_{CC} by all I/O ports, plus the maximum operating current drawn by the MCU on V_{CC}, must not exceed the absolute maximum rating I_{VCC}.
- The sum of the currents absorbed by all I/O ports and flowing from V_{SS}, plus the maximum operating current flowing from the MCU on V_{SS}, must not exceed the absolute maximum rating I_{VSS}.

Output Voltage

Unless otherwise noted, the parameters listed in the table below were obtained from tests conducted under general operating conditions TA using ambient temperature and VCC supply voltage conditions.

Table 5-28 Output Voltage Characteristics

| Symbol | Parameter | Condition | Minimum | Typical | Maximum ⁽²⁾ | Unit |
|-----------------|---|--|----------------------|---------|------------------------|------|
| V _{OL} | Output low, 8 pins absorb current simultaneously | 2.7 V ≤ V _{CC} ≤ 3.6 V, I _{IO} = +8 mA | - | - | 0.4 | V |
| | | 2.7 V ≤ V _{CC} ≤ 3.6 V, I _{IO} = +20 mA ⁽¹⁾ | - | - | 1.3 | |
| | | 2.0 V ≤ V _{CC} ≤ 2.7 V, I _{IO} = +6 mA ⁽¹⁾ | - | - | 0.4 | |
| V _{OH} | Output high, 8 pins simultaneously output current | 2.7 V ≤ V _{CC} ≤ 3.6 V, I _{IO} = +8 mA | V _{CC} -0.4 | - | - | |
| | | 2.7 V ≤ V _{CC} ≤ 3.6 V, I _{IO} = +20 mA ⁽¹⁾ | V _{CC} -1.3 | - | - | |
| | | 2.0 V ≤ V _{CC} ≤ 2.7 V, I _{IO} = +6 mA ⁽¹⁾ | V _{CC} -0.4 | - | - | |

1. The IO types can be found in the terminology and symbols of the pin definitions.
2. Data is based on test results and is not tested in production.

5.3.17. NRST pin characteristics

Table 5-29 NRST pin characteristics

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Unit |
|--------------------------------------|---|-----------------------------------|---------|---------|----------------------|------|
| V _{IL(NRST)} ⁽¹⁾ | NRST input low level | - | -0.5 | - | 0.8 | V |
| V _{IH(NRST)} ⁽¹⁾ | NRST input high level | - | 2 | - | V _{CC} +0.5 | |
| V _{hys(NRST)} | NRST Schmidt Hysteresis Voltage | - | - | 200 | - | mV |
| R _{PU} | Weak pull-up equivalent resistance ⁽²⁾ | V _{IN} = V _{SS} | 30 | 40 | 50 | kΩ |
| V _{F(NRST)} ⁽¹⁾ | NRST input filter pulse | - | - | - | 100 | ns |
| V _{NF(NRST)} ⁽¹⁾ | NRST input non-filtered pulse | - | 300 | - | - | ns |

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is designed as a true resistor in series with a switchable PMOS implementation. This PMOS/NMOS switch has a very small resistance (about 10%).

5.3.18. ADC characteristics

Table 5-30 ADC characteristics

| Symbol | Parameter | Condition | Minimum vaule | Typical | Maximum | Unit |
|---------------------------------|--|---------------------------|---|---------|--------------------|--------------------|
| V _{CCA} ⁽³⁾ | Supply voltage | - | 1.8 | - | 3.6 | V |
| V _{REF+} | Positive reference voltage | - | 1.8 | - | V _{CCA} | V |
| I _{VCCA} | V _{CCA} pin current | f _{ADC} = 16 MHz | - | 280 | 370 ⁽¹⁾ | μA |
| I _{VREF} | V _{REF} pin current | f _{ADC} = 16 MHz | - | 8 | 10 ⁽¹⁾ | μA |
| f _{ADC} | ADC clock frequency | - | 0.8 | - | 16 | MHz |
| f _S ⁽²⁾ | Sampling rate | - | 0.05 | - | 1 | MHz |
| V _{AIN} | Conversion voltage range ⁽³⁾ | - | 0 (V _{SSA} or V _{REF-} connected to ground) | - | V _{REF+} | V |
| R _{AIN} ⁽²⁾ | External input resistance | - | - | - | 30.9 | kΩ |
| R _{ADC} ⁽²⁾ | Sampling switch resistance | - | - | - | 1.6 | kΩ |
| C _{ADC} ⁽²⁾ | Internal sampling and holding capacitors | - | - | - | 8 | pF |
| t _{CAL} ⁽²⁾ | Calibration time | f _{ADC} = 16 MHz | 5.6875~8.75 | | | μs |
| | | - | 91 (sampling time of 1clk) ~ 140 (sampling time of 8clk) | | | 1/f _{ADC} |
| t _S ⁽²⁾ | Sampling time | f _{ADC} = 16 MHz | 0.218 | - | 14.968 | μs |
| | | - | 3.5 | - | 239.5 | 1/f _{ADC} |

| Symbol | Parameter | Condition | Minimum vaule | Typical | Maximum | Unit |
|--------------------------|---|-----------------------------------|---|---------|---------|--------------------|
| $t_{\text{samp_setup}}$ | Sampling time for internal channels | - | 20 | - | - | μs |
| $t_{\text{STAB}}^{(2)}$ | Power-up stabilization time | - | 0 | 0 | 1 | μs |
| $t_{\text{CONV}}^{(2)}$ | Total conversion time (including sampling time) | $f_{\text{ADC}} = 16 \text{ MHz}$ | 1 | - | 15.75 | μs |
| | | - | 16 ~ 252 (sampled t_s + 12.5 successive approximations) | | | $1/f_{\text{ADC}}$ |

1. Guaranteed by design, not tested in production.
2. Data is based on test results and is not tested in production.
3. Some package forms $V_{\text{REF+}}$ can be internally connected to V_{CCA} , $V_{\text{REF-}}$ can be internally connected to V_{SSA} , please refer to the pin definition for details.

Table 5-31 R_{AIN} max for $f_{\text{ADC}} = 16 \text{ MHz}^{(1)}$

| T_s (Periodicity) | t_s (μs) | R_{AIN} max (kW) |
|---------------------|-------------------------|---------------------------|
| 3.5 | 0.21 | 0.3 |
| 5.5 | 0.34 | 1.9 |
| 7.5 | 0.46 | 3.5 |
| 13.5 | 0.84 | 8.3 |
| 28.5 | 1.78 | 20.4 |
| 41.5 | 2.59 | 30.9 |
| 134.5 | 8.41 | NA |
| 239.5 | 15.96 | NA |

1. Guaranteed by design, not tested in production.

Table 5-32 ADC Accuracy⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

| Symbol | Parameter | Test condition | Typical | Maximum ⁽³⁾ | Unit |
|--------|------------------------------|---|---------|------------------------|------|
| ET | Total unadjusted error | $1.8 \text{ V} < V_{\text{CCA}}=V_{\text{REF+}} < 3.6 \text{ V}$; $f_{\text{ADC}} = 16 \text{ MHz}; f_s \leq 1 \text{ MSps}$; $T_A = \text{entire range}$ | 7.5 | 15 | LSB |
| EO | Offset error | $V_{\text{CCA}}=V_{\text{REF+}} 3.3 \text{ V}$; $f_{\text{ADC}} = 16 \text{ MHz}; f_s \leq 1 \text{ MSps}$ $T_A = \text{entire range}$ | 2 | 4 | LSB |
| | | $1.8 \text{ V} < V_{\text{CCA}}=V_{\text{REF+}} < 3.6 \text{ V}$; $f_{\text{ADC}} = 16 \text{ MHz}; f_s \leq 1 \text{ MSps}$ $T_A = \text{entire range}$ | 2 | 6 | |
| EG | Gain error | $V_{\text{CCA}}=V_{\text{REF+}} 3.3 \text{ V}$; $f_{\text{ADC}} = 16 \text{ MHz}; f_s \leq 1 \text{ MSps}$ $T_A = \text{entire range}$ | 4 | 5 | LSB |
| | | $1.8 \text{ V} < V_{\text{CCA}}=V_{\text{REF+}} < 3.6 \text{ V}$; $f_{\text{ADC}} = 16 \text{ MHz}; f_s \leq 1 \text{ MSps}$ $T_A = \text{entire range}$ | 4 | 8 | |
| ED | Differential linearity error | $1.8 \text{ V} < V_{\text{CCA}}=V_{\text{REF+}} < 3.6 \text{ V}$; $f_{\text{ADC}} = 16 \text{ MHz}; f_s \leq 1 \text{ MSps}$ $T_A = \text{entire range}$ | 1.2 | 1.5 | LSB |

| Symbol | Parameter | Test condition | Typical | Maximum ⁽³⁾ | Unit |
|--------|--------------------------|--|---------|------------------------|------|
| EL | Integral linearity error | 1.8 V < V _{CCA} = V _{REF+} < 3.6 V; f _{ADC} = 16 MHz; f _s ≤ 1 MSps T _A = entire range | 4 | 6 | LSB |

1. Data is based on test results and is not tested in production.
2. Calibration is done prior to ADC testing.
3. ADC Accuracy vs. Reverse Injected Current: Reverse current injection on any standard analog input pin needs to be avoided, as it can significantly degrade the accuracy of the conversion being performed on the other analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to the standard analog pin where the reverse injection current is likely to occur. If the forward injection current is within the I_{INJ(PIN)} and ΣI_{INJ(PIN)} ranges given in the I/O current injection characteristics, it will not affect the ADC accuracy.
4. Guaranteed by characteristic evaluation, not tested in production.

5.3.19. Temperature sensor characteristics

Table 5-33 Temperature sensor characteristics

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---------------------------------------|--|---------|---------|---------|-------|
| T _L ⁽¹⁾ | V _{SENSE} linearity with respect to temperature | - | ±1 | ±2 | °C |
| Avg_Slope ⁽¹⁾ | Average slope | 2.0 | 2.2 | 2.4 | mV/°C |
| V ₃₀ ⁽¹⁾ | Voltage at 30 °C (±5 °C) | 0.682 | 0.7 | 0.718 | V |
| t _{START} ⁽²⁾ | Start time | 4 | - | 10 | μs |
| T _{S_temp} ⁽²⁾⁽³⁾ | ADC sampling time when reading temperature | 20 | - | - | μs |

1. Guaranteed by design, not tested in production.
2. The data is based on assessment results and is not tested in production.
3. The minimum sampling time can be determined by the application through multiple cycles.

5.3.20. Built-in reference voltage characteristics

Table 5-34 Built-in reference voltage characteristics

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---------------------------------------|---|---------|---------|---------|--------|
| V _{REFINT} | Internal reference voltage | 1.17 | 1.2 | 1.23 | V |
| T _{S_vrefint} ⁽¹⁾ | ADC sampling time when reading the internal reference voltage | 17.1 | - | - | μs |
| V _{REFINT} | Internal reference voltage deviation over the temperature range | - | - | 10 | mV |
| T _{Coeff} | Temperature coefficient | -100 | - | 100 | ppm/°C |

1. Guaranteed by design, not tested in production.

5.3.21. Timer characteristics

Table 5-35 Timer characteristics

| Symbol | Parameter | Condition | Minimum | Maximum | Unit |
|-----------------------|-----------------------------------|--------------------------------|---------|-------------------------|----------------------|
| t _{res(TIM)} | Timer resolution time | - | 1 | - | t _{TIMxCLK} |
| | | f _{TIMxCLK} = 144 MHz | - | - | ns |
| f _{EXT} | Timer external clock frequency on | - | 0 | f _{TIMxCLK} /2 | MHz |

| Symbol | Parameter | Condition | Minimum | Maximum | Unit |
|------------------|---|---------------------------------|---------|----------------------|---------------|
| | CH1 to CH4 | $f_{TIMxCLK} = 144 \text{ MHz}$ | - | - | MHz |
| Res_{TIM} | Timer resolution | - | - | 16 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | - | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK} = 144 \text{ MHz}$ | - | - | μs |
| t_{MAX_COUNT} | Maximum possible count | - | - | 65536×65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK} = 144 \text{ MHz}$ | - | - | s |

Table 5-36 IWDG characteristics (Clock Select LSI)

| Prescaler | PR[2:0] | Minimum overflow | Maximum overflow | Unit |
|-----------|---------|------------------|------------------|------|
| /4 | 0 | 0.122 | 499.712 | ms |
| /8 | 1 | 0.244 | 999.424 | |
| /16 | 2 | 0.488 | 1998.848 | |
| /32 | 3 | 0.976 | 3997.696 | |
| /64 | 4 | 1.952 | 7995.392 | |
| /128 | 5 | 3.904 | 15990.784 | |
| /256 | 6 or 7 | 7.808 | 31981.568 | |

Table 5-37 WWDG characteristics (clock selection 48 MHz PCLK)

| Prescaler | WDGTB[1:0] | Minimum overflow | Maximum overflow | Unit |
|-----------------|------------|------------------|------------------|------|
| 1×4096 | 0 | 0.085 | 5.461 | ms |
| 2×4096 | 1 | 0.171 | 10.923 | |
| 4×4096 | 2 | 0.341 | 21.845 | |
| 8×4096 | 3 | 0.683 | 43.691 | |

5.3.22. Communication port characteristics

5.3.22.1. I²C Interface Features

The I²C interface conforms to the standard I²C communication protocol with the following limitations: SDA and SCL are not true pins and when configured as open-drain outputs, the PMOS tube between the pinout and V_{CC} is turned off, but still present.

Table 5-38 I²C Interface Features

| Symbol | Parameter | Standard I ² C ⁽¹⁾ | | Fast I ² C ⁽¹⁾⁽²⁾ | | Unit |
|---------------------------|--|--|---------------------|---|--------------------|---------------|
| | | Minimum | Maximum | Minimum | Maximum | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | μs |
| $t_{w(SCLH)}$ | SCL clock high time | 4 | - | 0.6 | - | μs |
| $t_{su(SDA)}$ | SDA build time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data retention time | - | 3450 ⁽³⁾ | - | 900 ⁽³⁾ | |
| $t_{r(SDA)} / t_{r(SDL)}$ | SDA and SCL rise time | - | 1000 | - | 300 | |
| $t_{f(SDA)} / t_{f(SDL)}$ | SDA and SCL down time | - | 300 | - | 300 | |
| $t_{h(STA)}$ | Start condition hold time | 4 | - | 0.6 | - | μs |
| $t_{su(STA)}$ | Repeated start condition establishment time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | Stop condition establishment time | 4 | - | 0.6 | - | |
| $t_{w(STO:STA)}$ | Time from stop condition to start condition (bus idle) | 4.7 | - | 1.3 | - | |

| | | Standard I ² C ⁽¹⁾ | | Fast I ² C ⁽¹⁾⁽²⁾ | | |
|-----------------|-----------------------------|--|-------------------|---|-------------------|----|
| C _b | Capacitive load per bus | - | 400 | - | 400 | pF |
| t _{sp} | Noise filtering pulse width | 0 | 50 ⁽⁴⁾ | 0 | 50 ⁽⁴⁾ | μs |

1. Guaranteed by design, not tested in production.
2. To achieve the maximum frequency for standard mode I²C, f_{PCLK1} must be greater than 2 MHz. f_{PCLK1} must be greater than 4 MHz to achieve the maximum frequency for fast mode I²C.
3. A hold time of at least 300 nS on the SDA signal must be ensured internally to avoid data changes on the SDA bus during SCL low at data output.
4. The noise pulse width is suppressed by the analog filter.

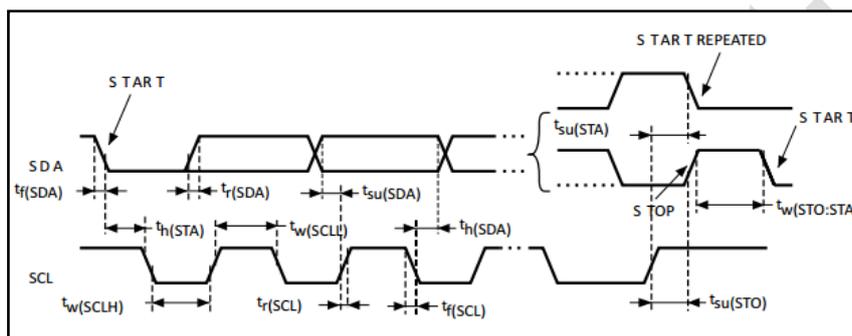


Figure 5-5 I²C Bus Timing Diagram

5.3.22.2. SPI Interface characteristics

Table 5-39 SPI Interface characteristics

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Unit |
|--|---------------------------------------|--------------------------------|--------------------------|--------------------|--------------------------------|------|
| f _{SCK} 1/t _c (SCK) | SPI clock frequency | Master Mode 2.7~3.6 V | - | - | 36 | MHz |
| | | Master Mode 1.8~3.6 V | - | - | 36 | |
| | | Slave mode 2.7~3.6 V | - | - | 36 | |
| | | Slave mode 1.8~3.6 V | - | - | 36 | |
| t _r (SCK) t _f (SCK) | SPI clock rise/fall time | Load capacitance: C= 30 pF | - | - | 5 | ns |
| DuCy(SCK) | SPI Slave Mode Input Clock Duty Cycle | Slave mode | 45 | - | 55 | % |
| t _{su} (NSS) | NSS build time | Slave mode | 4t _{PCLK} | - | - | ns |
| t _h (NSS) | NSS hold time | Slave mode | 2t _{PCLK} | - | - | |
| t _w (SCKH) t _w (SCKL) | SCK high/low time | Master Mode, presc = 4 | 2T _{pclk} -1 | 2T _{pclk} | 2T _{pclk} +1 | |
| t _{su} (MI) | Data entry build time | Master Mode presc = 4 | T _{pclk} +4 (1) | - | - | |
| t _{su} (SI) | | Slave mode presc = 4 | 3 | - | - | |
| t _h (MI) | Data input hold time | Master Mode | 4 | - | - | |
| t _h (SI) | | Slave mode | T _{pclk} +4 | - | - | |
| t _a (SO) | Data output access time | Slave mode presc = 4 | 0 | - | 3T _{pclk} | |
| t _{dis} (SO) | Data output prohibition time | Slave mode | 2T _{pclk} +5 | - | 4T _{pclk} +5 | |
| t _v (SO) | Data output validity time | Slave mode 2.7~3.6 V presc = 4 | 0 | - | 12 or 1.5T _{pclk} (2) | |
| | | Slave mode 1.8~3.6 V presc = 4 | 0 | - | 18 or 1.5T _{pclk} (2) | |

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Unit |
|-------------|-----------------------|--|------------------|---------|---------|------|
| $t_{V(MO)}$ | | Master Mode (after enable edge) | - | 3.5 | 4.5 | |
| $t_{h(SO)}$ | Data output hold time | Slave mode (after enable edge) presc = 4 | 0 ⁽³⁾ | - | - | |
| $t_{h(MO)}$ | | Master Mode (after enable edge) | 2 | - | - | |

1. Master generates 1 PCLK receive control signal before the receive edge.
2. The Slave has a maximum of 1 PCLK delay based on the SCK send edge, and 1.5 PCLK is defined considering the IO delay, etc.
3. The Slave updates the data before the send edge if the SCK duty cycle sent by the Master is wide between the receive edge and the send edge.

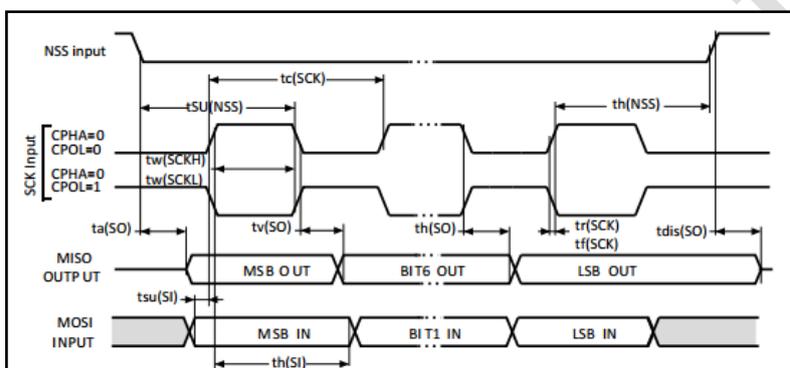


Figure 5-6 SPI Timing Diagram - Slave Mode and CPHA = 0

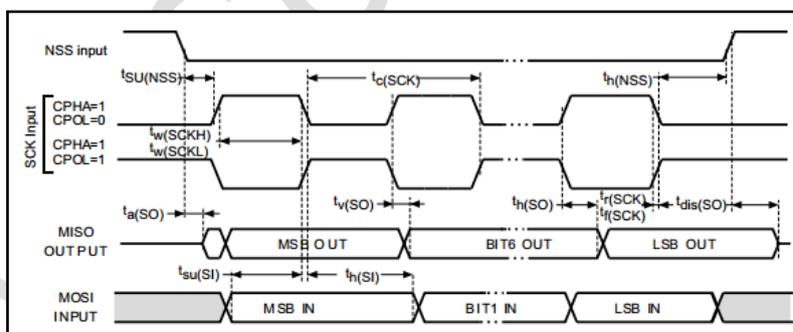


Figure 5-7 SPI Timing Diagram - Slave Mode and CPHA = 1(1)

1. Measurement points set at CMOS levels: $0.3V_{CC}$ and $0.7V_{CC}$

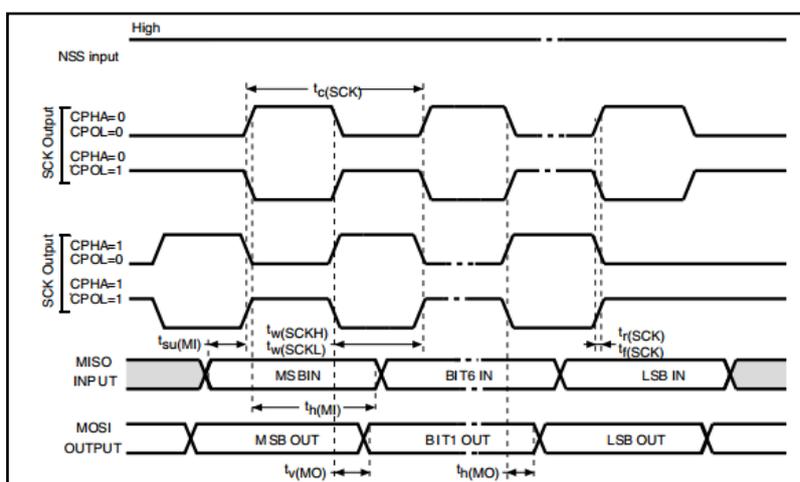


Figure 5-8 SPI Timing Diagram-Master Mode(1)

1. Measurement point set at CMOS level: 0.3V^{CC} and 0.7V^{CC}

5.3.22.3. I2S Interface characteristics

Table 5-40 I2SInterface characteristics

| Symbol | Parameter | Condition | Minimum | Maximum | Unit | |
|--|-----------------------------------|--|-----------|-----------------------------------|------|----|
| f _{MCLK} | I2S Master Clock Output | - | 256x8 K | 256xF _s ⁽¹⁾ | MHz | |
| f _{CK} 1/t _{c(CK)} | I2S Clock Frequency | Master mode data | - | 64xF _s | MHz | |
| | | Slave mode data | - | 64xF _s | | |
| D _{CK} | I2S Clock Duty Cycle | Slave mode reception | 30 | 70 | % | |
| t _{r(CK)} t _{f(CK)} | I2S Clock up/down time | Capacitive load C _L = 50 pF | - | 8 | ns | |
| t _{v(WS)} | W _S Effective time | Master mode | - | 2 | | |
| t _{h(WS)} | W _S Holding time | Master mode | 3 | - | | |
| | | Slave mode | 2 | - | | |
| t _{su(W_S)} | W _S Establishment time | Slave mode | 4 | - | | |
| t _{su(SD_MR)} t _{su(SD_SR)} | Data entry build time | Master receiver | 3 | - | | |
| | | Slave receiver | 4 | - | | |
| t _{h(SD_MR)} t _{h(SD_SR)} | Data input hold time | Master receiver | 5 | - | | |
| | | Slave receiver | 2 | - | | |
| t _{v(SD_ST)} | Data output validity time | Slave receiver (After enable edge) | 2.7-3.6 V | - | | 15 |
| | | | 2.0-3.6 V | - | | 22 |
| t _{v(SD_MT)} | | Master receiver (After enable edge) | - | 2 | | |
| t _{h(SD_ST)} t _{h(SD_MT)} | Data output hold time | Slave receiver (After enable edge) | 7 | - | | |
| | | Master receiver (After enable edge) | 1 | - | | |

1. 256xF_s up to 49.152 MHz

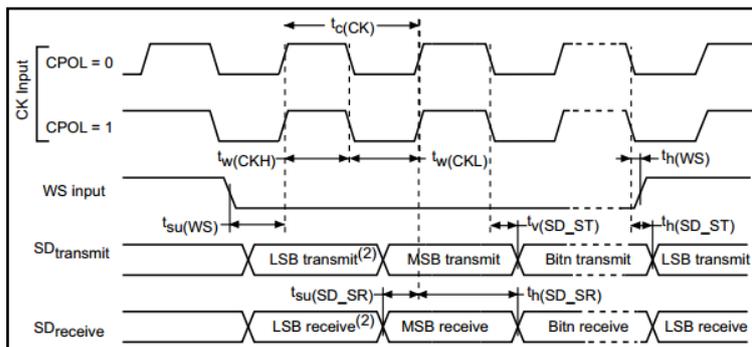


Figure 5-9 I2S Slave mode timing diagram (Philips protocol) ⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3 \times V_{CC}$ and $0.7 \times V_{CC}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

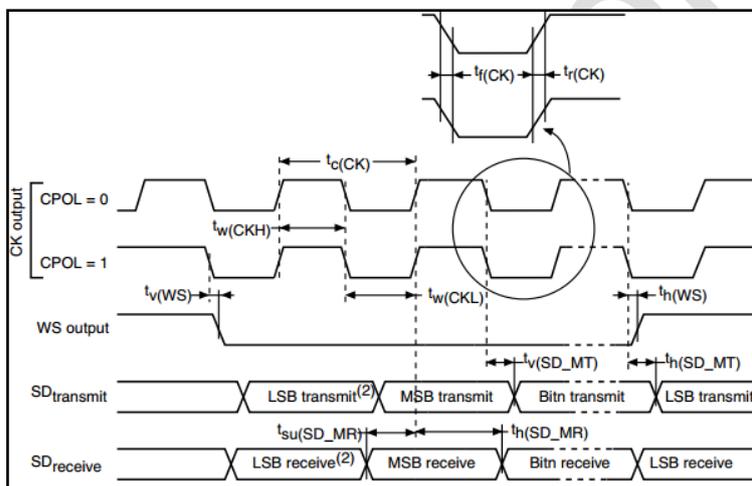


Figure 5-10 I2S Master mode timing diagram (Philips protocol) ⁽¹⁾

1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

5.3.22.4. USB characteristics

Table 5-41 USB Startup time

| Symbol | Parameter | Maximum | Unit |
|-------------------|------------------------------|---------|---------|
| $t_{START}^{(1)}$ | USB transceiver startup time | 1 | μs |

1. Guaranteed by design

Table 5-42 USB DC Characteristics

| Symbol | Parameter | Condition | Minimum ⁽¹⁾ | Maximum ⁽¹⁾ | Unit |
|----------------|--------------------------------------|-------------------|------------------------|------------------------|------|
| V_{CC} | USB operating voltage ⁽²⁾ | - | 3.0 ⁽³⁾ | 3.6 | V |
| $V_{DI}^{(4)}$ | Differential input sensitivity | I(USB_DP, USB_DM) | 0.2 | - | |

| Symbol | Parameter | Condition | Minimum ⁽¹⁾ | Maximum ⁽¹⁾ | Unit |
|----------------|---------------------------------|--|------------------------|------------------------|------|
| $V_{CM}^{(4)}$ | Differential common mode range | Includes VDI range | 0.8 | 2.5 | |
| $V_{SE}^{(4)}$ | Single-ended receiver threshold | - | 1.3 | 2 | |
| Output Level | | | | | |
| V_{OL} | Static output low level | $R_L = 1.5 \text{ k}\Omega$ connected to $3.6 \text{ V}^{(5)}$ | - | 0.3 | V |
| V_{OH} | Static output high level | $R_L = 15 \text{ k}\Omega$ connected to $V_{SS}^{(5)}$ | 2.8 | 3.6 | |

- All voltage measurements are based on the ground at the device end.
- The USB function of this product can be as low as 2.7 V. However, the complete USB electrical characteristics cannot be guaranteed in the range of V_{CC} voltage reduction to 2.7~3.0 V.
- Guaranteed by evaluation, not tested in production.
- R_L is the load connected to the USB driver.

 Table 5-43 USB Full speed electrical characteristics ⁽¹⁾

| Symbol | Parameter | Condition | Minimum | Maximum | Unit |
|-----------|---------------------------------|--------------------------|---------|---------|------|
| t_r | Rise time ⁽²⁾ | $C_L \leq 50 \text{ pF}$ | 4 | 20 | ns |
| t_f | Descent time ⁽²⁾ | $C_L \leq 50 \text{ pF}$ | 4 | 20 | ns |
| t_{rfm} | Rise and fall time match | t_r/t_f | 90 | 110 | % |
| V_{CRS} | Output signal crossover voltage | - | 1.3 | 2.0 | V |

- Guaranteed by design, not tested in production.
- Measurement data signals from 10% to 90%.

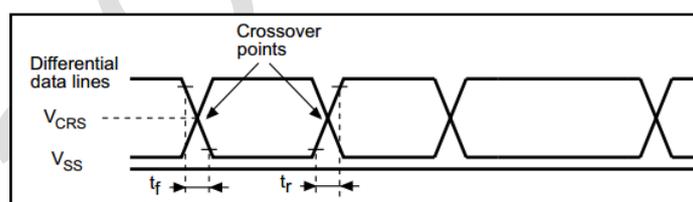


Figure 5-11 USB Timing: Data Signal Rise and Fall Time Definition

5.3.23. SD/SDIO MMCCard host interface characteristics

Table 5-44 SD/MMC characteristics

| Symbol | Parameter | Condition | Minimum | Maximum | Unit |
|--|---------------------------------------|---------------------------|---------|---------|------|
| f_{PP} | Clock frequency in data transfer mode | $C_L \leq 30 \text{ pF}$ | 0 | 48 | MHz |
| $t_{W(CKL)}$ | Clock low time | $f_{PP} = 48 \text{ MHz}$ | 8.5 | - | ns |
| $t_{W(CKH)}$ | Clock High Time | $f_{PP} = 48 \text{ MHz}$ | 8.3 | - | |
| CMD, D input in MMC and SD HS modes (based on CK) | | | | | |
| t_{ISU} | Input build time | $f_{PP} = 48 \text{ MHz}$ | 3.5 | - | ns |
| t_{IH} | Input hold time | $f_{PP} = 48 \text{ MHz}$ | 0 | - | |
| CMD, D output in MMC and SD HS modes (based on CK) | | | | | |

| Symbol | Parameter | Condition | Minimum | Maximum | Unit |
|---|-------------------------------|---------------------------|---------|---------|------|
| t_{OV} | Output effective time | $f_{PP} = 48 \text{ MHz}$ | - | 7 | ns |
| t_{OH} | Output hold time | $f_{PP} = 48 \text{ MHz}$ | 3 | - | |
| CMD, D input in SD default mode (with CK as reference) | | | | | |
| T_{ISUD} | Input build time | $f_{PP} = 24 \text{ MHz}$ | 1.5 | - | ns |
| t_{IH} | Input hold time | $f_{PP} = 24 \text{ MHz}$ | 0.5 | - | |
| CMD, D output in SD default mode (with CK as reference) | | | | | |
| t_{OVD} | Output valid default time | $f_{PP} = 24 \text{ MHz}$ | - | 6.5 | ns |
| t_{OHD} | Output maintains default time | $f_{PP} = 24 \text{ MHz}$ | 3.5 | - | |

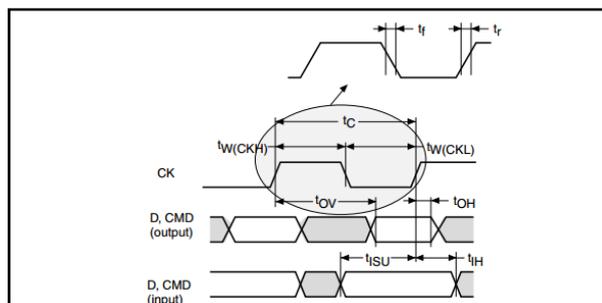


Figure 5-12 SDIO High speed mode

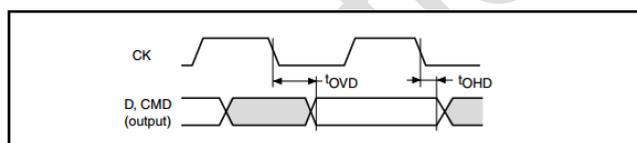


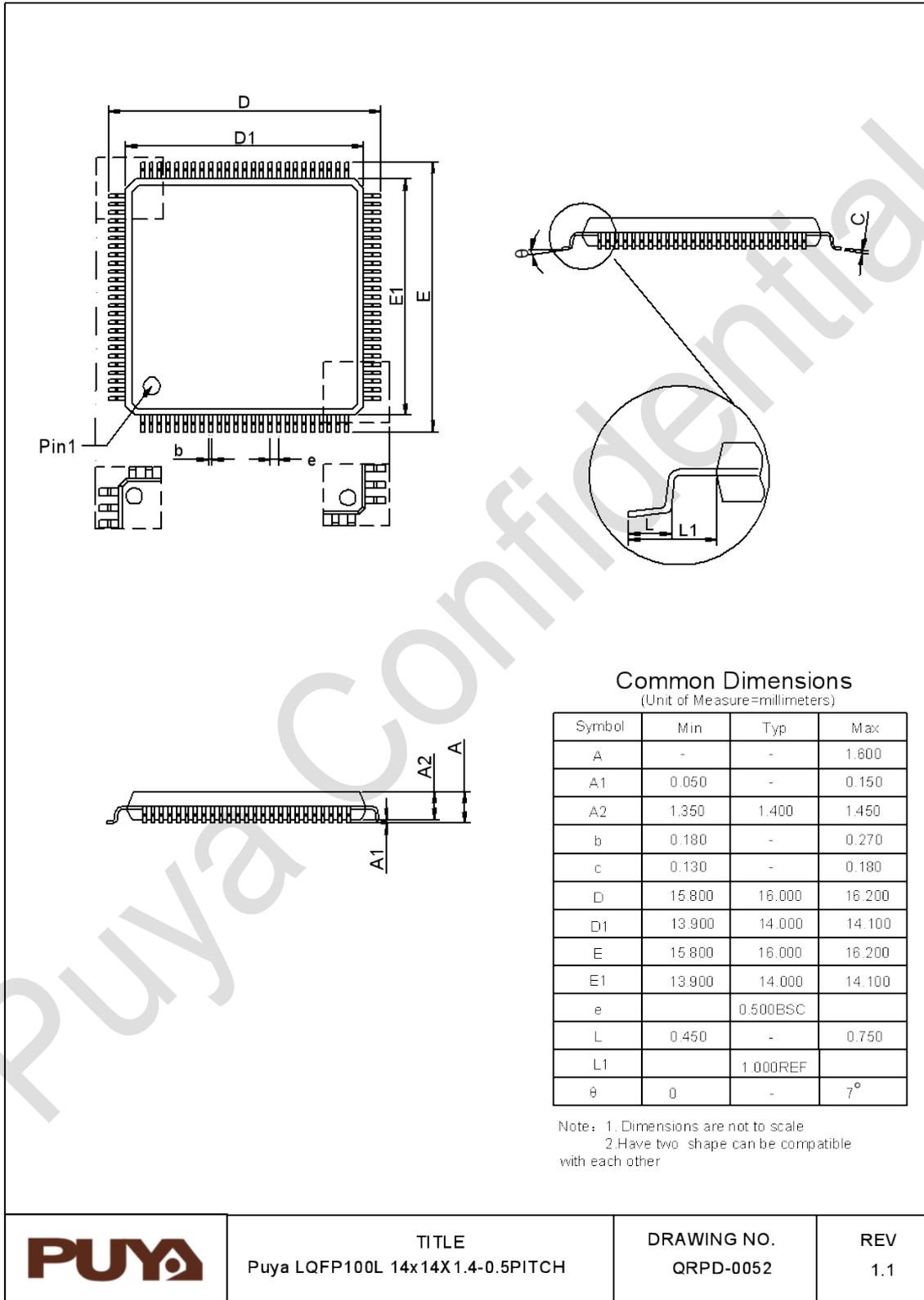
Figure 5-13 SD Default Mode

5.3.24. CANFD Interface characteristics

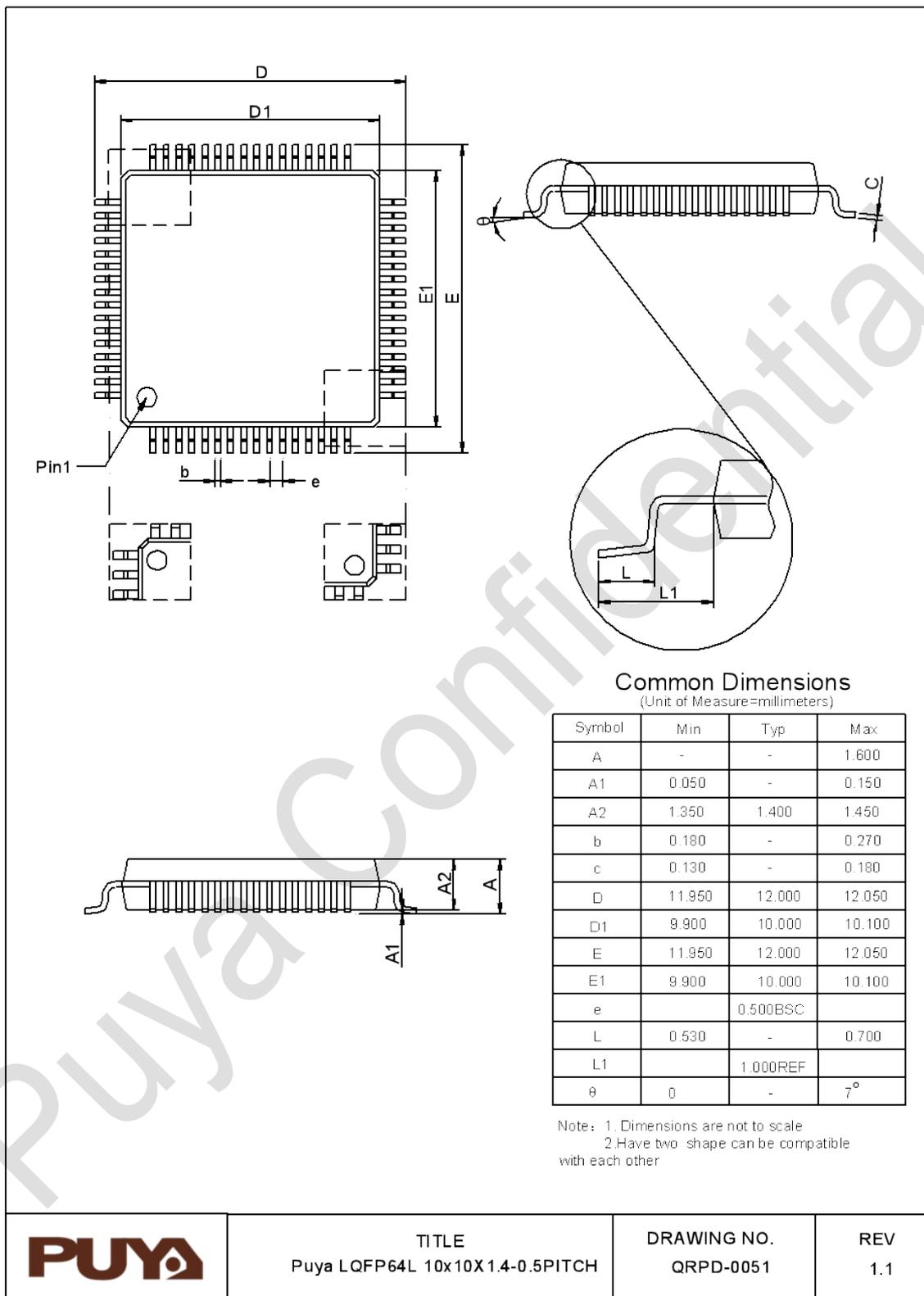
For the characteristics of the input/output multiplexing function pins (CANFD_TX and CANFD_RX), see the IO Port Characteristics chapter.

6. Package information

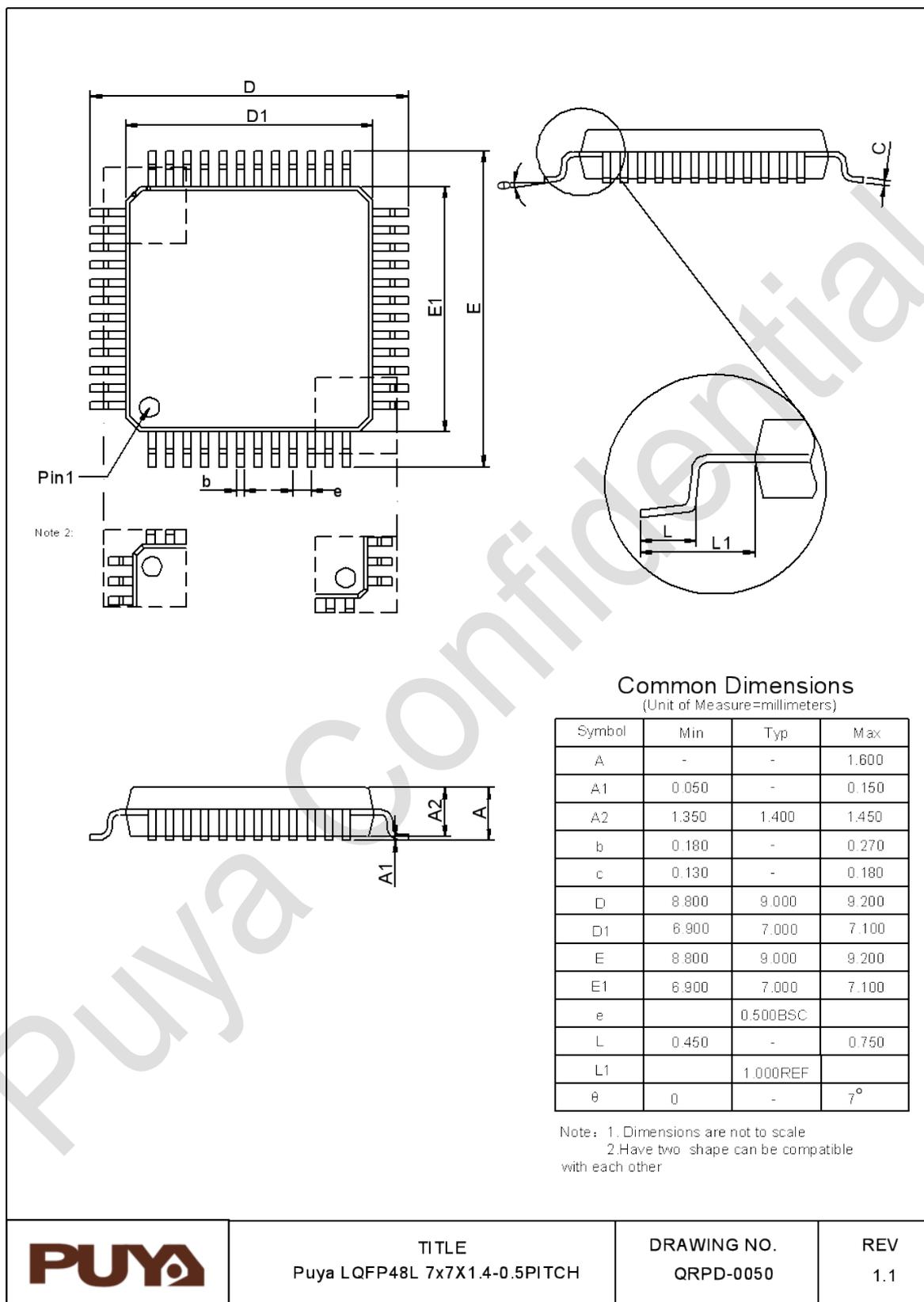
6.1. LQFP100 package size



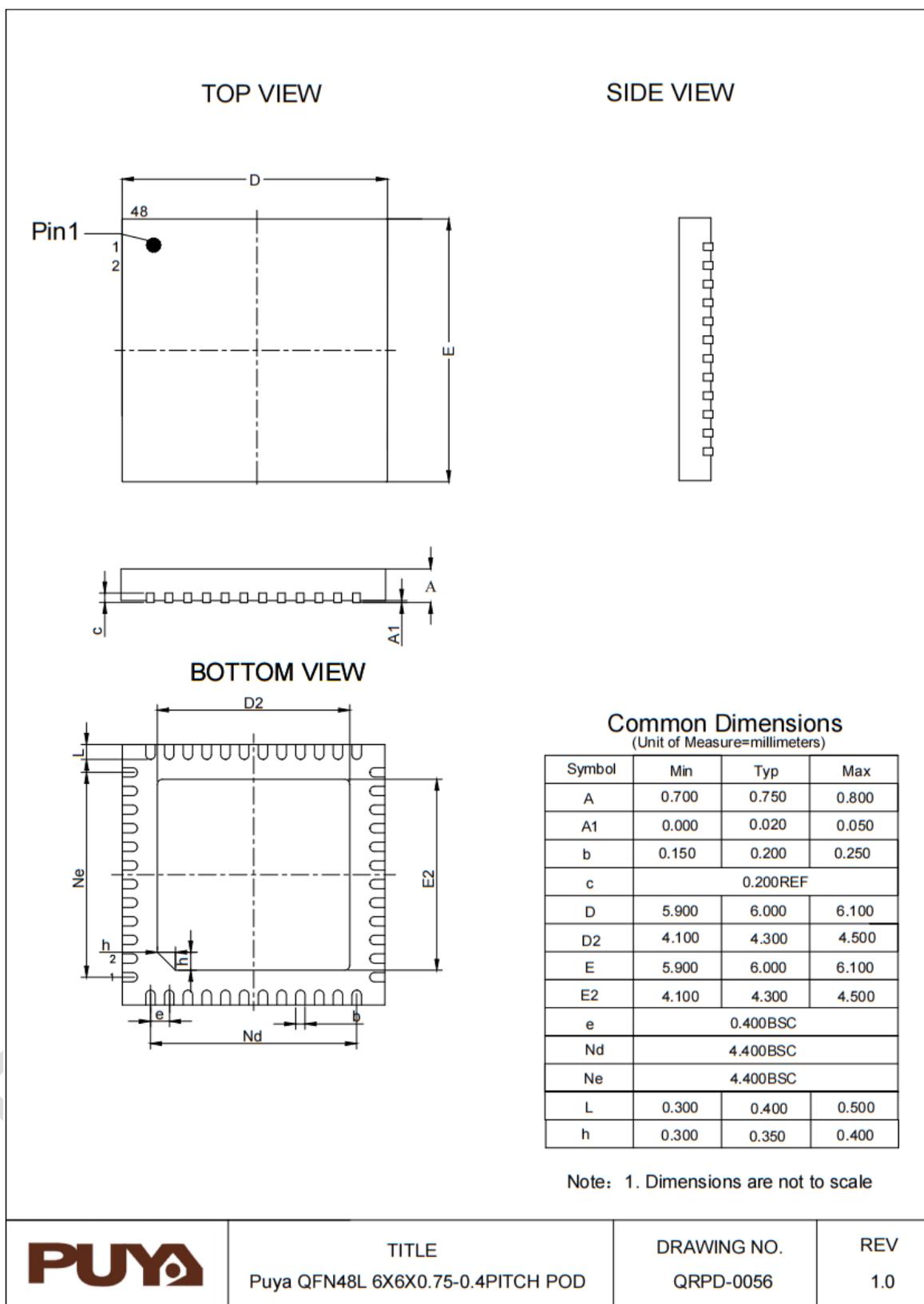
6.2. LQFP64 package size



6.3. LQFP48 package size



6.4. QFN48 package size

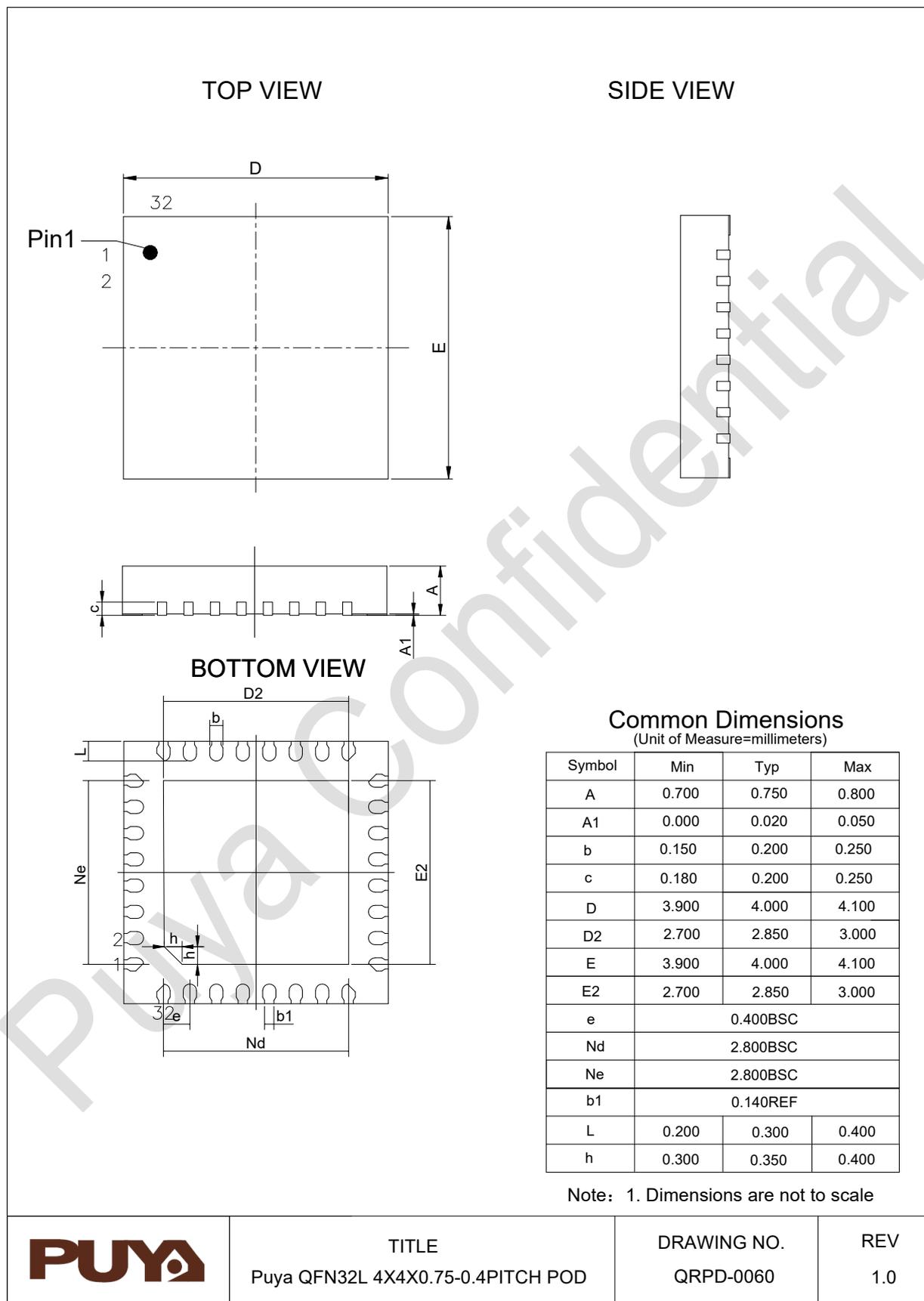


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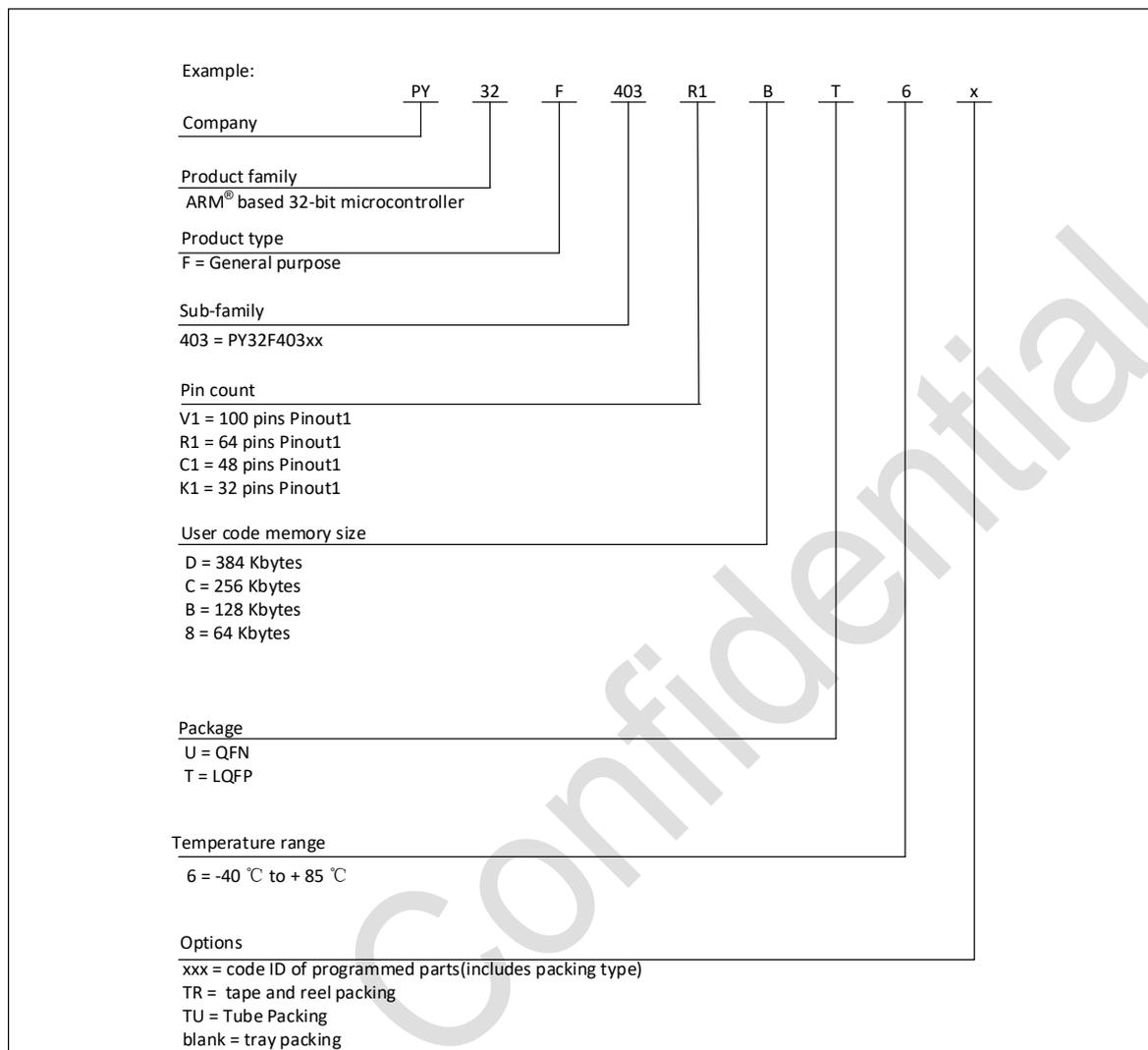
DRAWING NO.
QRPD-0056

REV
1.0

6.5. QFN32 (4*4) package size



7. Ordering information



8. Version history

| Version | Date | Description |
|---------|------------|---|
| V1.0 | 2023.08.30 | 1. Initial version |
| V1.1 | 2024.01.12 | 1. Update Ordering Information |
| V1.2 | 2024.01.29 | 1. Update Figure 3-6 QFN32 PY32F403Kx Pinout1 |
| V1.3 | 2024.05.09 | <ol style="list-style-type: none"> 1. Add QFN48 package 2. Update Table 1-1 3. Update 2.8.1 Power supply block diagram 4. Update Table 5-4 General working conditions 5. Update Table 5-39 SPI Interface characteristics |
| V1.4 | 2024.11.13 | <ol style="list-style-type: none"> 1. Update Table 5-26 EFT 2. Update LQFP100/ LQFP64/ LQFP48 package information |
| V1.8 | 2025.06.11 | <ol style="list-style-type: none"> 1. Consist with the Chinese version No. 2. Update in chapter 3 with PC13 status and use notes when powered by V_{BAT} only |



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