## FEATURES

- **Access Times of 120, 150, 200, and 250ns**

- **Single 5V±10% Power Supply**

- **Simple Byte and Page Write**

- **Low Power CMOS:**
  - 60 mA Active Current
  - 500 µA Standby Current

- **Fast Write Cycle Times**

- **Software Data Protection**

- **Fully TTL Compatible Inputs and Outputs**

- **Endurance:**
  - 10,000 Cycles/byte
  - 100,000 Cycles/page

- **Data Retention: 100 Years**

- **Available in the following package:**
  – 32-Pin 600 mil Ceramic DIP
  – 32-Pin Ceramic LCC (450x550 mils)
  – 32-Pin Solder Seal Flatpack
 **– 44-Pin Ceramic LCC (650x650 mils)**

DESCRIPTION

The PYA28C010 is a 5 Volt 128Kx8 EEPROM using float-ing gate CMOS Technology. The device supports 64-byte page write operation. The PYA28C010 features $\overline{DATA}$ and Toggle Bit Polling as well as a system software scheme used to indicate early completion of a Write Cycle. The device also includes user-optional software data protection. Data Retention is 100 Years. The device is available in a 32-Pin 600 mil wide Ceramic DIP, 32-Pin LCC, 32-Pin Solder Seal Flatpack and 44-Pin Ceramic LCC.

FUNCTIONAL BLOCK DIAGRAM
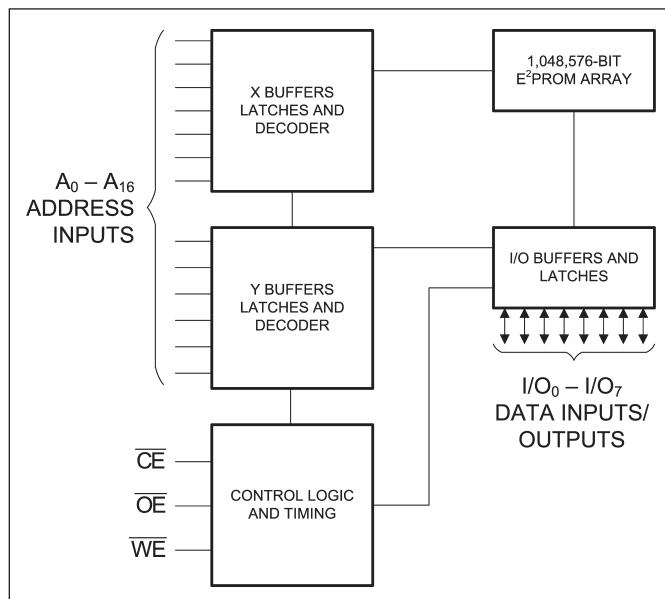
PIN CONFIGURATION

DIP (C10)   LCC (L6)
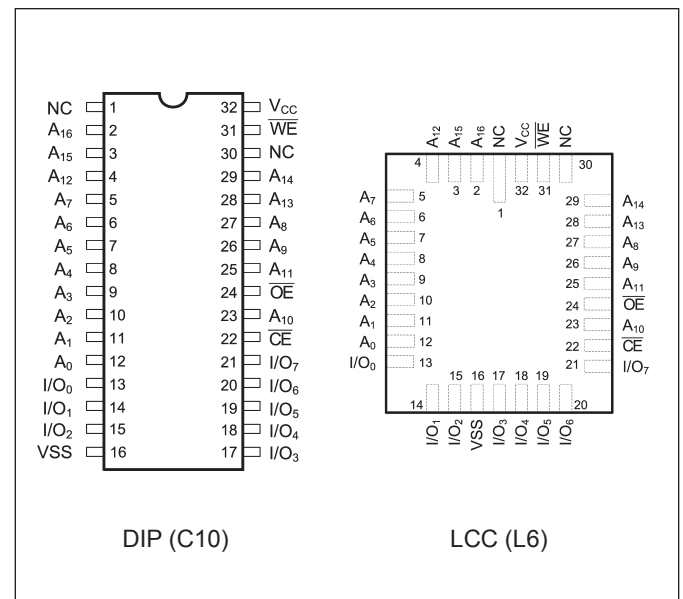
OPERATION

READ

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

WRITE

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The PYA28C010 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.
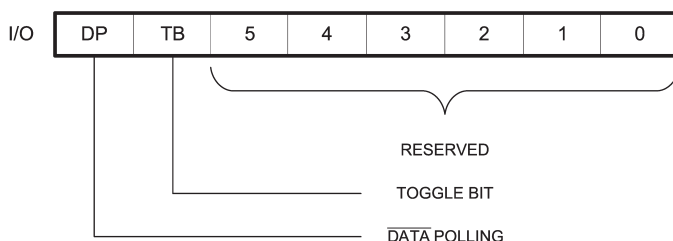
PAGE WRITE

The page write feature of the AS28C010 allows the entire memory to be written in 5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the PYA28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_8 through A_{16}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty-six bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

WRITE

The PYA28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown below.

I/O	DP	TB	5	4	3	2	1	0

RESERVED

TOGGLE BIT

$\overline{DATA}$ POLLING

DATA POLLING

The PYA28C010 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the PYA28C010, eliminating additional interrupts or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data=0xxx xxxx, read data=1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the PYA28C010 is in the protected state and an illegal write operation is attempted, $\overline{DATA}$ Polling will not operate.

TOGGLE BIT

The PYA28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle, I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for addtional read or write operations.

DATA PROTECTION

Pyramid Semiconductor has incorporated both hardware and software features that will protect the memory against inadvertent writes during transitions of the host system power supply.

HARDWARE PROTECTION

Hardware features protect against inadvertent writes to the PYA28C010 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION

A software controlled data protection feature has been implemented on the PYA28C010. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the PYA28C010 is shipped from Pyramid Semiconductor with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} the entire PYA28C010 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the PYA28C010. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the PYA28C010 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the

3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of tWC, read operations will effectively be polling operations.

DEVICE IDENTIFICATION

An extra 128-bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 1FF80H to 1FFFFH the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE

The entire device can be erased using a 6-byte software code. Please see "Software Chip Erase" application note at the end of this datasheet for details.

MAXIMUM RATINGS[1]

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.3 to +6.25	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 6.25V)	-0.5 to +6.25	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES[4]
(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

DC ELECTRICAL CHARACTERISTICS
(Over Recommended Operating Temperature & Supply Voltage)[2]

Sym	Parameter	Test Conditions	PYA28C010 Min	PYA28C010 Max	Unit
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		-0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage		V_{CC} - 0.2	V_{CC} + 0.5	V
V_{LC}	CMOS Input Low Voltage		-0.5[3]	0.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +2.1 mA, V_{CC} = Min		0.45	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = -0.4 mA, V_{CC} = Min	2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max V_{IN} = GND to V_{CC}	-10	+10	µA
I_{LO}	Output Leakage Current	V_{CC} = Max, $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	-10	+10	µA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH}$, $\overline{OE}$ = V_{IL}, V_{CC} = Max, f = Max, Outputs Open	—	3	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{HC}$, V_{CC} = Max, f = Max, Outputs Open, $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	—	300	µA
I_{CC}	Supply Current	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, All I/O's = Open, Inputs = V_{CC} = 5.5V	—	60	µA

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.

2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.

3. Transient inputs with V_{IL} and I_{IL} not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20ns.

4. This parameter is sampled and not 100% tested.

POWER-UP TIMING

Symbol	Parameter	Max	Unit
t_{PUR}	Power-up to Read operation	100	µs
t_{PUW}	Power-up to Write operation	5	ms

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym	Parameter	-120		-150		-200		-250		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	120		150		200		250		ns
t_{AVQV}	Address Access Time		120		150		200		250	ns
t_{ELQV}	Chip Enable Access Time		120		150		200		250	ns
t_{OLQV}	Output Enable Access Time		50		50		50		50	ns
t_{ELQX}	Chip Enable to Output in Low Z	0		0		0		0		ns
t_{EHQZ}	Chip Disable to to Output in High Z		50		50		50		50	ns
t_{OLQX}	Output Enable to Output in Low Z	0		0		0		0		ns
t_{OHQZ}	Output Disable to Output in High Z		50		50		50		50	ns
t_{AVQX}	Output Hold from Address Change	0		0		0		0		ns

TIMING WAVEFORM OF READ CYCLE
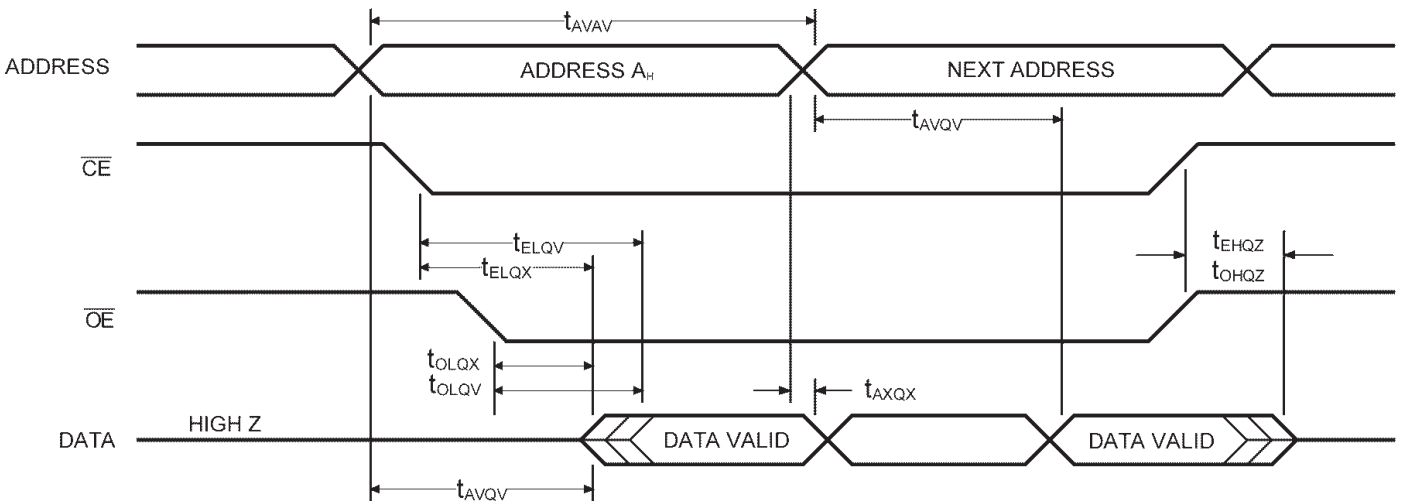
AC CHARACTERISTICS—WRITE CYCLE
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Symbol	Parameter	-120		-150		-200		-250		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WHWL1} t_{EHEL1}	Write Cycle Time		10		10		10		10	ms
t_{AVEL} t_{AVWL}	Address Setup Time	0		0		0		0		ns
t_{ELAX} t_{WLAX}	Address Hold Time	50		50		50		50		ns
t_{WLEL} t_{ELWL}	Write Setup Time	0		0		0		0		ns
t_{WHEH}	Write Hold Time	0		0		0		0		ns
t_{OHEL} t_{OHWL}	$\overline{OE}$ Setup Time	10		10		10		10		ns
t_{WHOL}	$\overline{OE}$ Hold Time	10		10		10		10		ns
t_{ELEH} t_{WLWH}	$\overline{WE}$ Pulse Width	100		100		100		100		ns
t_{DVEH} t_{DVWH}	Data Setup Time	50		50		50		50		ns
t_{EHDX} t_{WHDX}	Data Hold Time	0		0		0		0		ns
t_{EHEL2} t_{WHWL2}	Byte Load Cycle Time	0.2	100	0.2	100	0.2	100	0.2	100	µs
t_{ELWL}	$\overline{CE}$ Setup Time	1		1		1		1		µs
t_{OVHWL}	Output Setup Time	1		1		1		1		µs
t_{EHWH}	$\overline{CE}$ Hold Time	1		1		1		1		µs
t_{WHOH}	$\overline{OE}$ Hold Time	1		1		1		1		µs

TIMING WAVEFORM OF BYTE WRITE CYCLE ($\overline{CE}$ CONTROLLED)
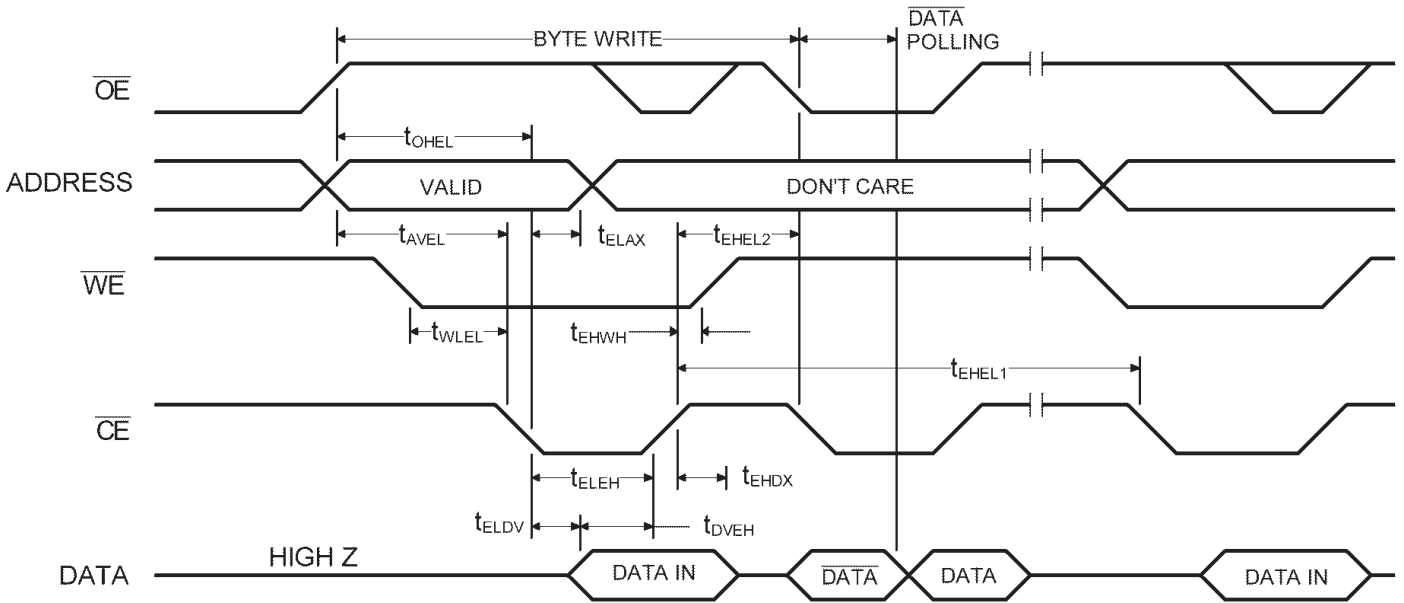
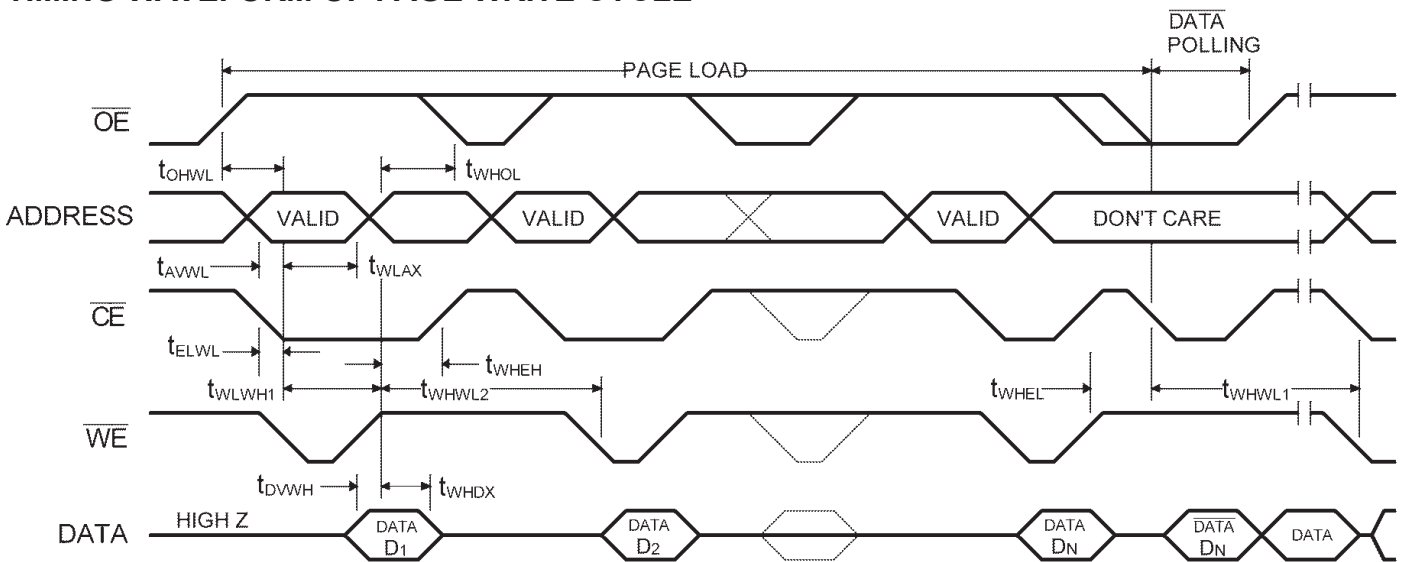## TIMING WAVEFORM OF BYTE WRITE CYCLE ($\overline{WE}$ CONTROLLED)
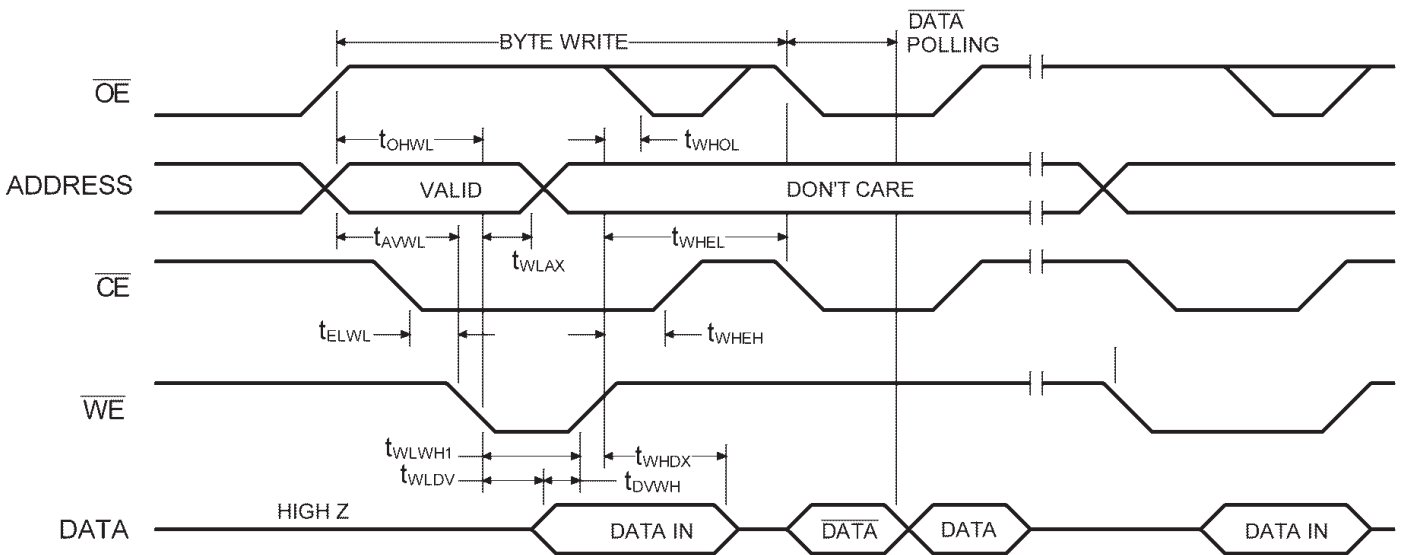
TIMING WAVEFORM OF PAGE WRITE CYCLE
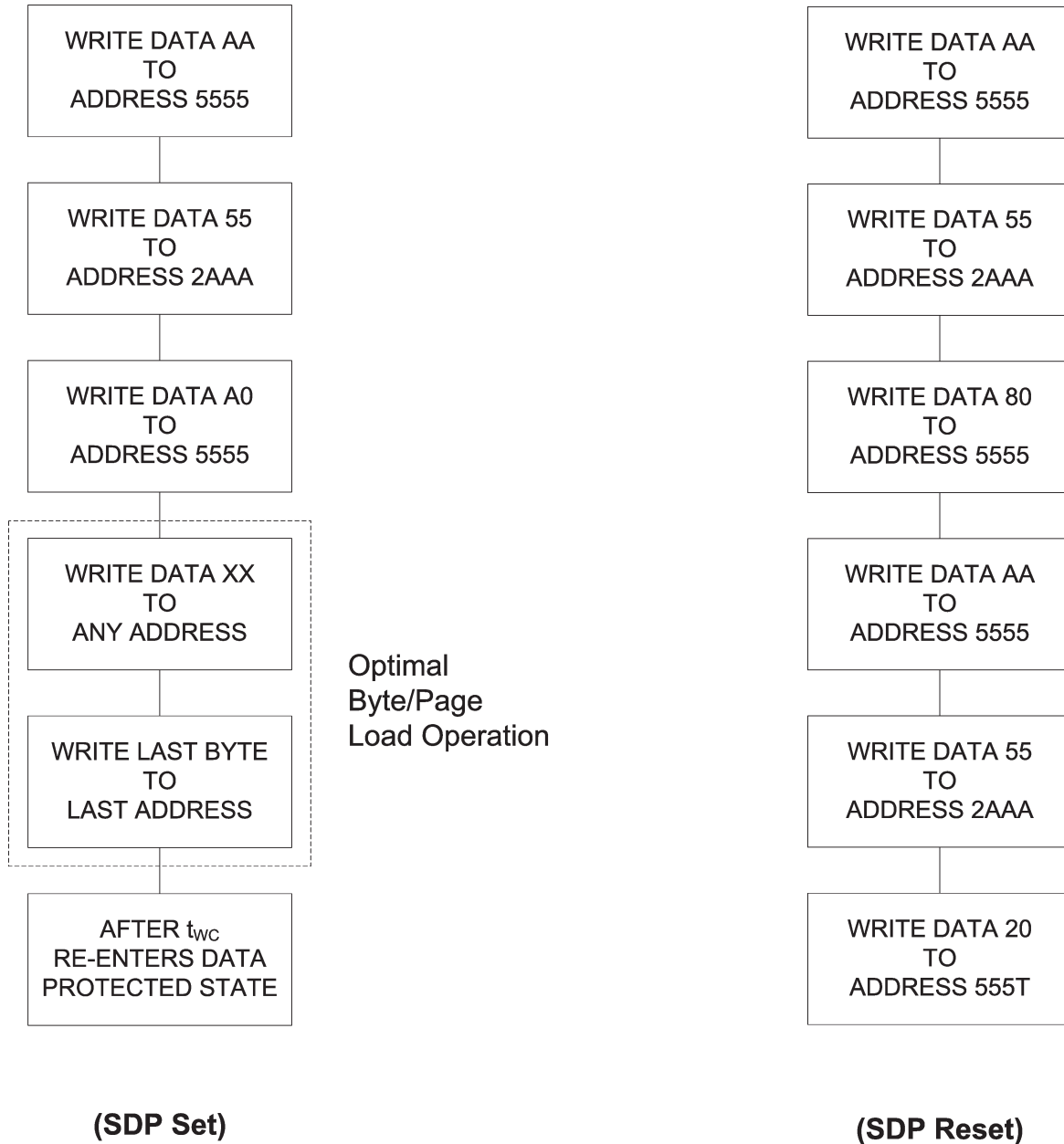

NOTES:

• For each successive write within the page write operation, A_8-A_{16} should be the same. Otherwise, writes to an unknown address could occur.

• Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW. For example, this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write. Alternatively, this can be done with $\overline{WE}$ HIGH and $\overline{CE}$ LOW, effectively performing a polling operation.

• The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

WRITE SEQUENCE FOR SOFTWARE DATA PROTECTION

SOFTWARE SEQUENCE TO DE-ACTIVATE SOFTWARE DATA PROTECTION

WRITE DATA AA TO ADDRESS 5555

WRITE DATA 55 TO ADDRESS 2AAA

WRITE DATA A0 TO ADDRESS 5555

WRITE DATA XX TO ANY ADDRESS

WRITE LAST BYTE TO LAST ADDRESS

Optimal
Byte/Page
Load Operation

AFTER t_{WC} RE-ENTERS DATA PROTECTED STATE

(SDP Set)

WRITE DATA AA TO ADDRESS 5555

WRITE DATA 55 TO ADDRESS 2AAA

WRITE DATA 80 TO ADDRESS 5555

WRITE DATA AA TO ADDRESS 5555

WRITE DATA 55 TO ADDRESS 2AAA

WRITE DATA 20 TO ADDRESS 555T

(SDP Reset)

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figure 1

TRUTH TABLE

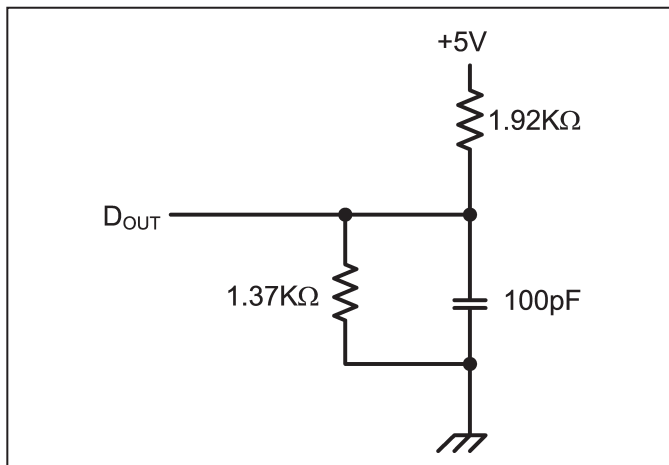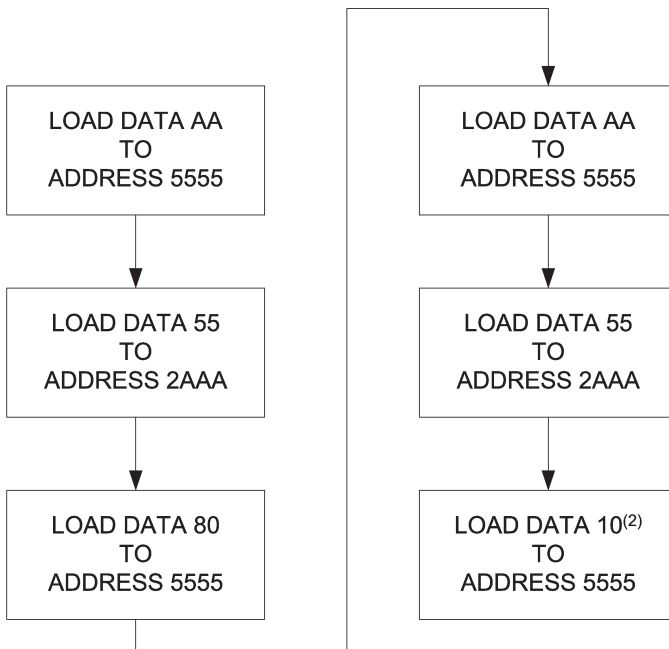| Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	D_{OUT}
Write	L	H	L	D_{IN}
Write Inhibit	X	L	X	—
Write Inhibit	X	X	H	—
Standby	H	X	X	High Z

Figure 1. Output Load

APPLICATION NOTE - SOFTWARE CHIP ERASE

The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with specific data patterns. Once the code has been entered, the device will set each byte to the high state (FFH). After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time required to erase the whole chip is t_{EC} (20 ms). The software data protection is still enabled even after the software chip erase is performed.

CHIP ERASE CYCLE CHARACTERISTICS

Symbol	Parameter	
t_{EC}	Chip Erase Cycle Time	20 ms Max

CHIP ERASE SOFTWARE ALGORITHM[1][3]

LOAD DATA AA
TO
ADDRESS 5555

↓

LOAD DATA 55
TO
ADDRESS 2AAA

↓

LOAD DATA 80
TO
ADDRESS 5555

LOAD DATA AA
TO
ADDRESS 5555

↓

LOAD DATA 55
TO
ADDRESS 2AAA

↓

LOAD DATA 10[2]
TO
ADDRESS 5555

Notes:
1. Data Format: (Hex); Address Format: (Hex).
2. After loading the 6-byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion in 20 ms (max).
3. The flow diagram shown is for a x8 part. For a x16 part, the data should be 16 bits long (e.g., the data to be loaded should be AAAA for step 1 in the algorithm).
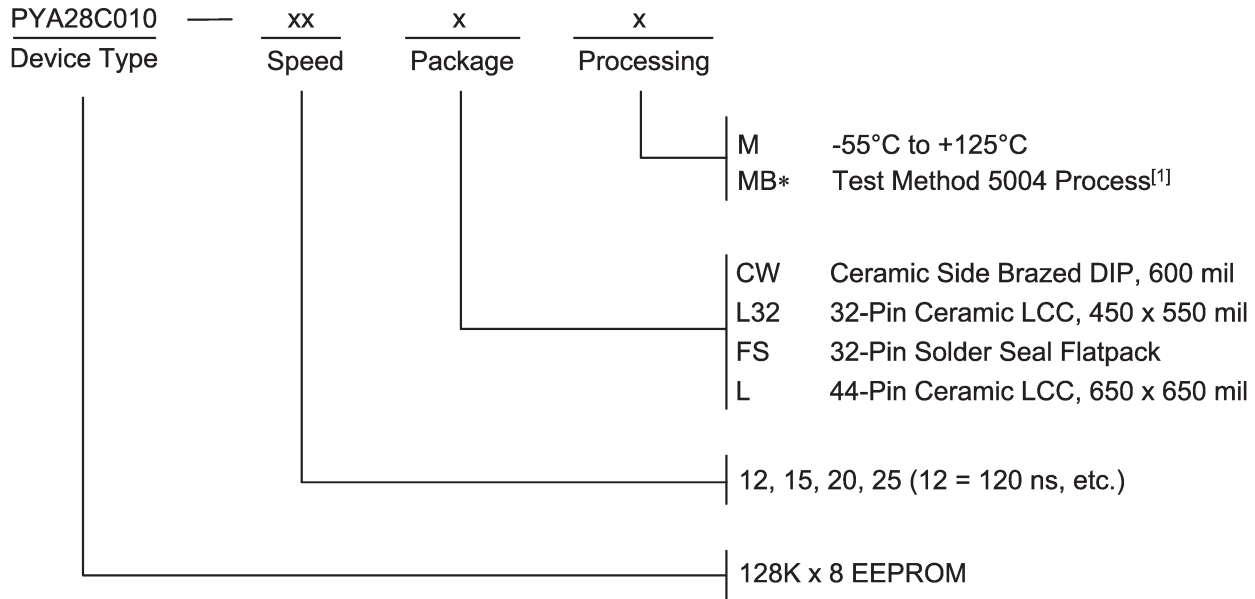
CHIP ERASE CYCLE WAVEFORMS
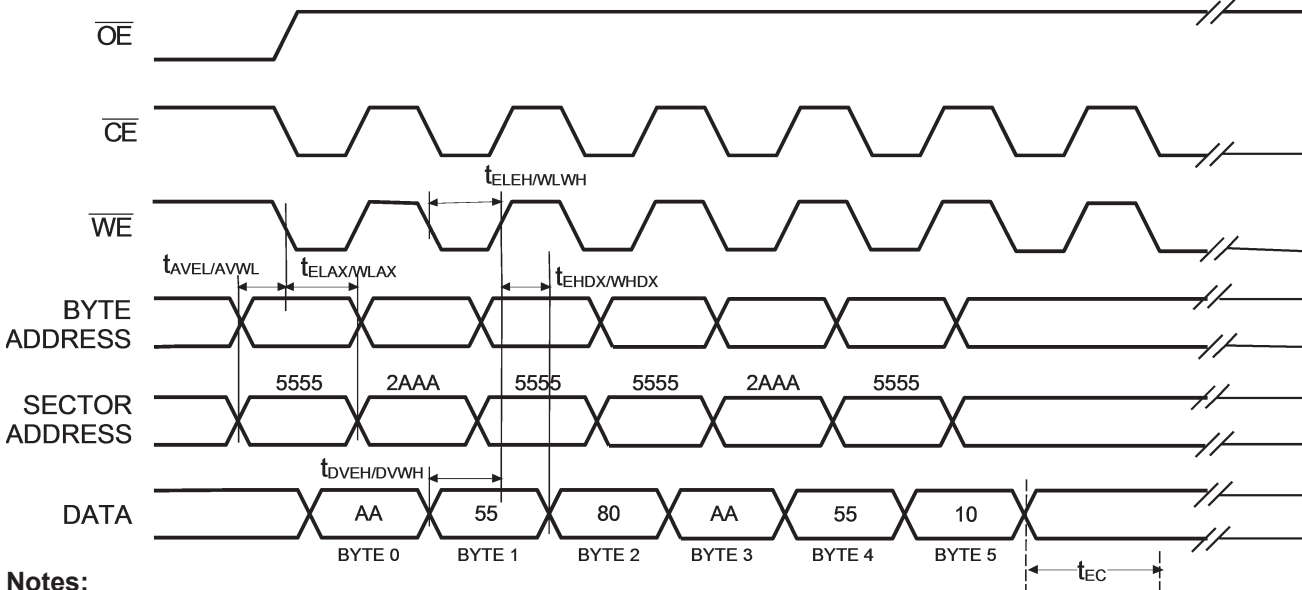
Notes:
1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

ORDERING INFORMATION

PYA28C010 —— xx x x
Device Type | Speed | Package | Processing

M   -55°C to +125°C
MB∗   Test Method 5004 Process[1]

CW   Ceramic Side Brazed DIP, 600 mil
L32   32-Pin Ceramic LCC, 450 x 550 mil
FS   32-Pin Solder Seal Flatpack
L   44-Pin Ceramic LCC, 650 x 650 mil

12, 15, 20, 25 (12 = 120 ns, etc.)

128K x 8 EEPROM

[1] Parts are not MIL-STD-883 compliant. Parts are processed per Test Method 5004.

SIDE BRAZED DUAL IN-LINE PACKAGE (600 mils)

Pkg #	C10	
# Pins	32 (600 mil)	
Symbol	**Min**	**Max**
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.680
E	0.510	0.620
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-

SOLDER SEAL FLAT PACKAGE
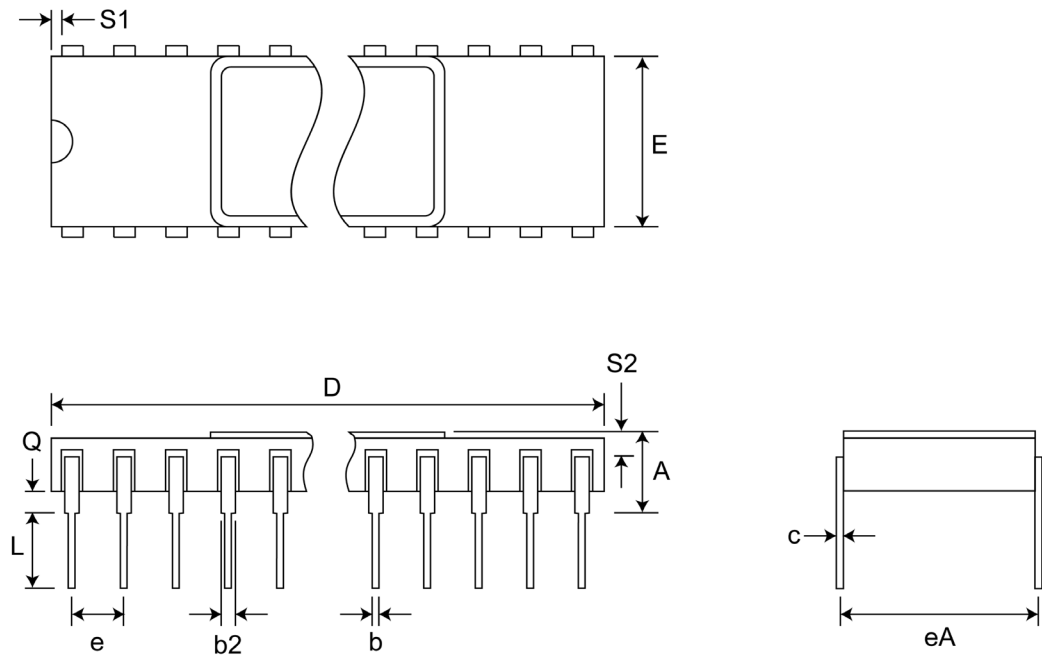
Pkg #	FS-3	
# Pins	32	
Symbol	**Min**	**Max**
A	0.097	0.125
b	0.015	0.019
c	0.003	0.009
D	-	0.830
E	0.400	0.420
E1	-	0.450
E2	0.180	-
E3	0.030	-
e	0.050 BSC	
L	0.250	0.370
Q	0.020	0.045
S	-	0.045
S1	0.000	-
M	-	0.002
N	32	
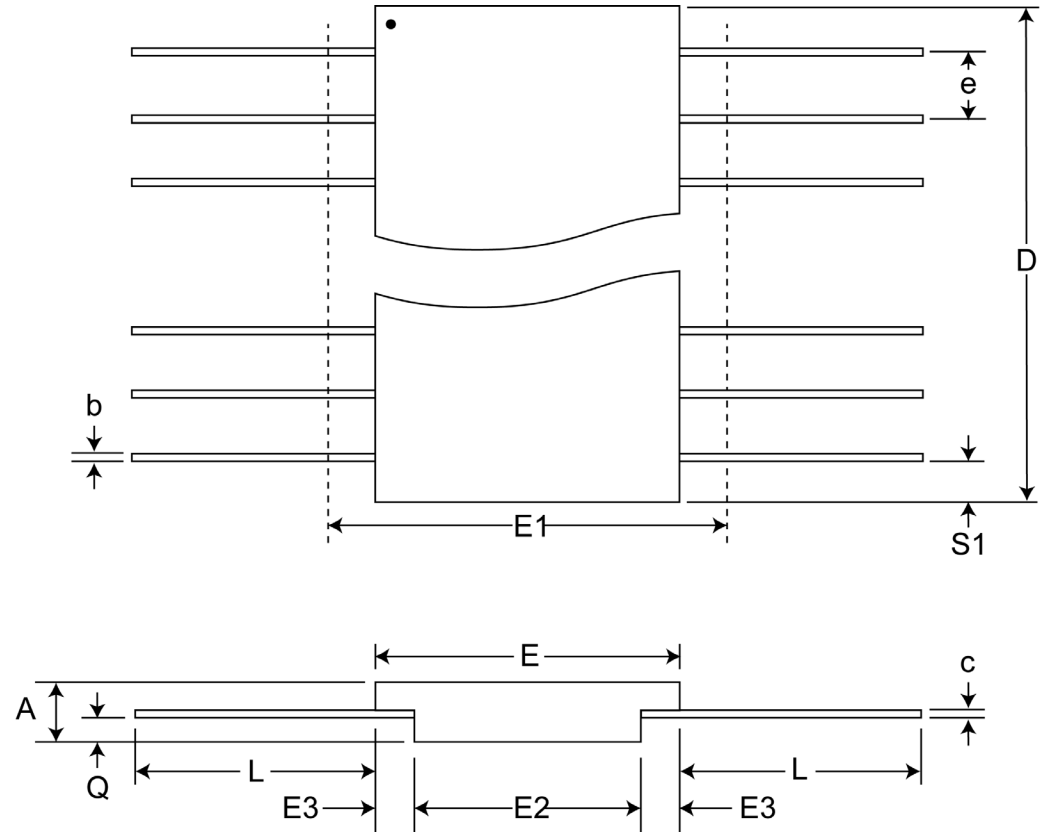
RECTANGULAR LEADLESS CHIP CARRIER

Pkg #	L6	
# Pins	32	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.442	0.458
D1	0.300 BSC	
D2	0.150 BSC	
D3	-	0.458
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	7	
NE	9	
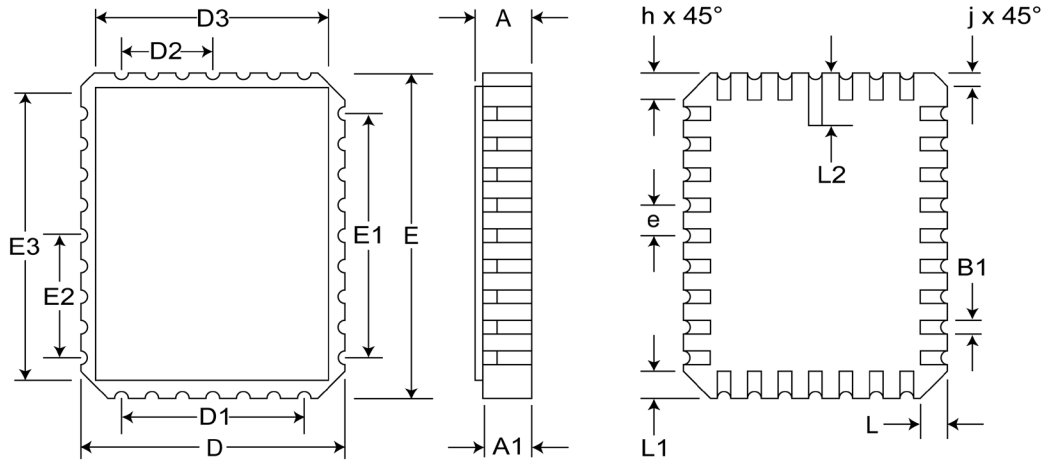
SQUARE LEADLESS CHIP CARRIER

Pkg #	L14	
# Pins	44	
Symbol	**Min**	**Max**
A	0.070	0.088
A1	0.060	0.075
B1	0.022	0.028
D/E	0.640	0.660
D1/E1	0.500 BSC	
D2/E2	0.250 BSC	
D3/E3		0.662
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.080	0.090
ND	11	
NE	11	
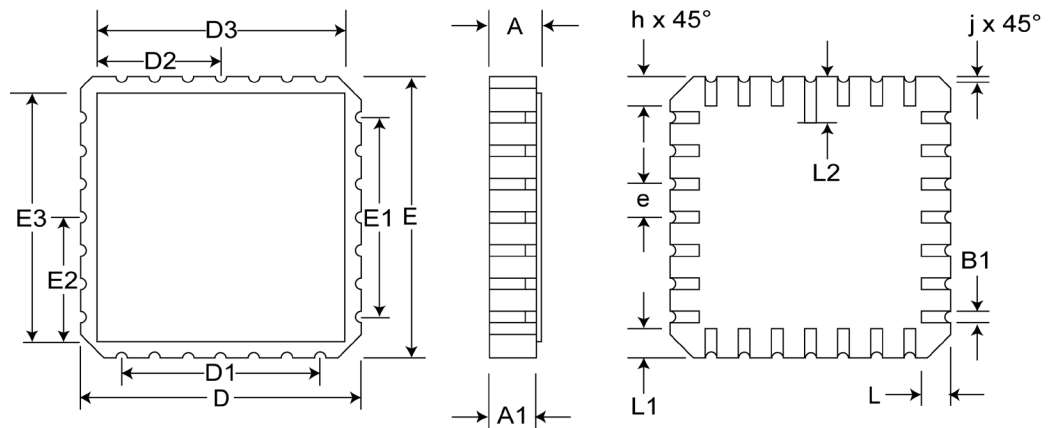
REVISIONS

DOCUMENT NUMBER	EEPROM103
DOCUMENT TITLE	PYA28C010 - 128K x 8 EEPROM

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Oct 2009	JDB	New Data Sheet
01	Jun 2011	JDB	Part number corrected throughout from "PYX28C010" to "PYA28C010"
02	Oct 2011	JDB	Added 32-pin flatpack and 44-pin LCC packages