

NIKO-SEM

P-Channel Enhancement Mode Field Effect Transistor

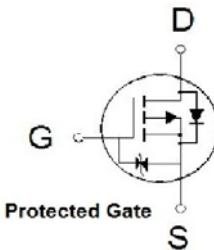
PZ0703ETF

TO-220F

Halogen-Free & Lead-Free

**PRODUCT SUMMARY**

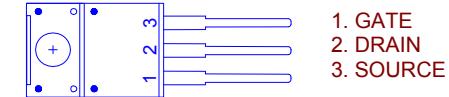
$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
-30V	7.5mΩ	-55A

**Features**

- Pb-Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.
- Products Integrated ESD diode with ESD Protected.

Applications

- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.

**ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 16	V
Continuous Drain Current ^{2,3}	I_D	-55	A
$T_C = 100^\circ\text{C}$	I_D	-35	
Pulsed Drain Current ¹	I_{DM}	-130	
Avalanche Current	I_{AS}	-50	
Avalanche Energy	E_{AS}	125	mJ
Power Dissipation	P_D	41	W
$T_C = 100^\circ\text{C}$	P_D	17	
Junction & Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$	3	62.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$			

¹Pulse width limited by maximum junction temperature.²Limited only by maximum temperature allowed.³Package limitation current is -55A.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1	-1.6	-3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±16V			±30	uA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V			1	
		V _{DS} = -20V, V _{GS} = 0V, T _J = 125 °C			10	μA
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -4.5V, I _D = -20A		7.6	12	
		V _{GS} = -10V, I _D = -20A		5	7.5	mΩ
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -20A		57		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		4987		
Output Capacitance	C _{oss}			1095		pF
Reverse Transfer Capacitance	C _{rss}			1018		
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz		2.4		Ω
Total Gate Charge ²	Q _g			128		
Gate-Source Charge ²	Q _{gs}	V _{DS} = -15V , V _{GS} = -10V , I _D = -20A		15		nC
Gate-Drain Charge ²	Q _{gd}			34		
Turn-On Delay Time ²	t _{d(on)}	V _{DS} = -15V, I _D ≈ -20A, V _{GS} = -10V, R _{GS} = 6Ω		32		
Rise Time ²	t _r			24		
Turn-Off Delay Time ²	t _{d(off)}			90		
Fall Time ²	t _f			44		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I _s				-31	A
Forward Voltage ¹	V _{SD}	I _F = -20A, V _{GS} = 0V			-1.3	V
Reverse Recovery Time	t _{rr}	I _F = -20A, dI _F /dt = 100A / μS		32		nS
Reverse Recovery Charge	Q _{rr}			21		nC

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.²Independent of operating temperature.³Package limitation current is -55A.

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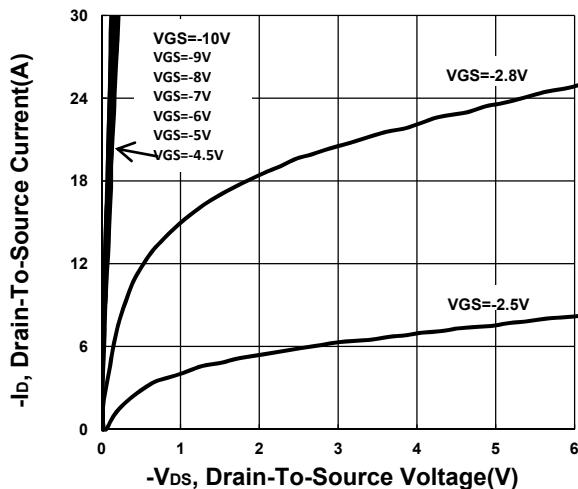
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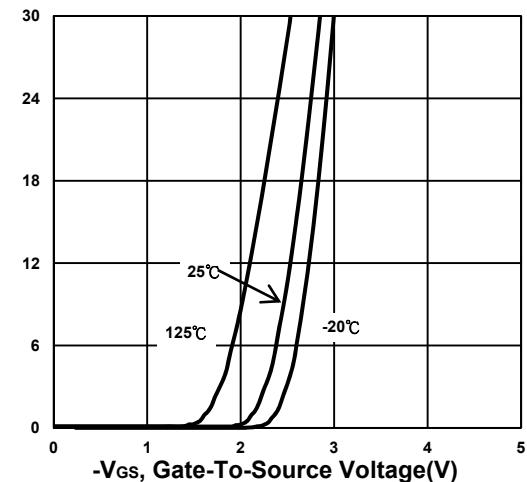
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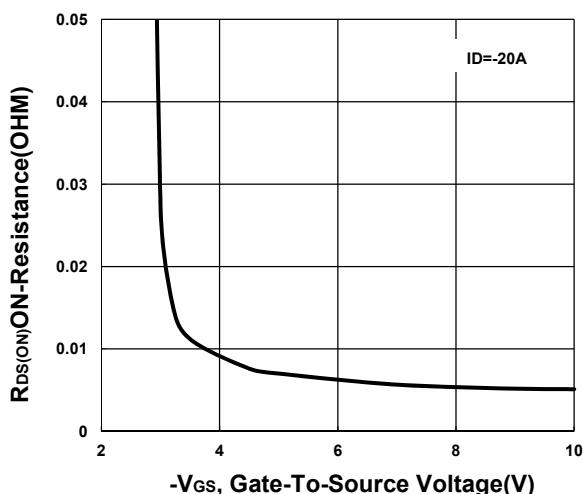
Output Characteristics



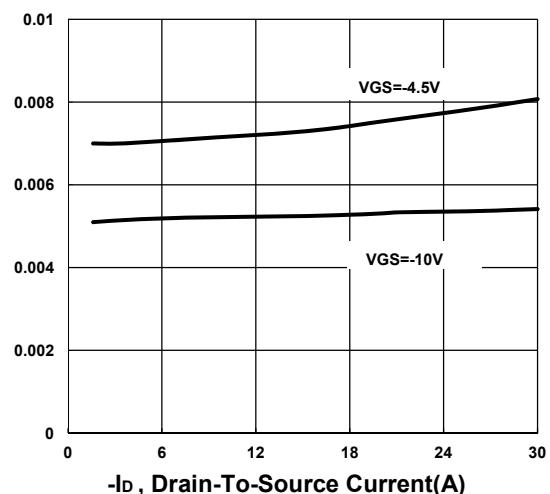
Transfer Characteristics



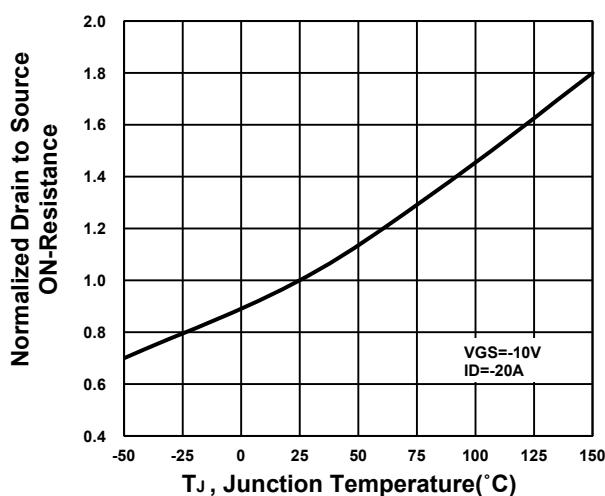
On-Resistance VS Gate-To-Source



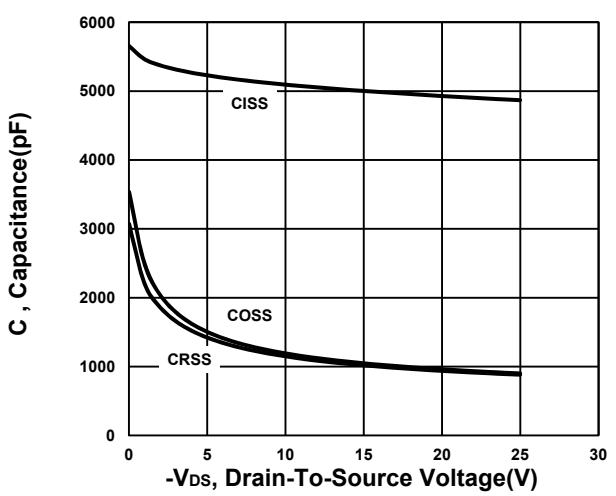
On-Resistance VS Drain Current



On-Resistance VS Temperature



Capacitance Characteristic



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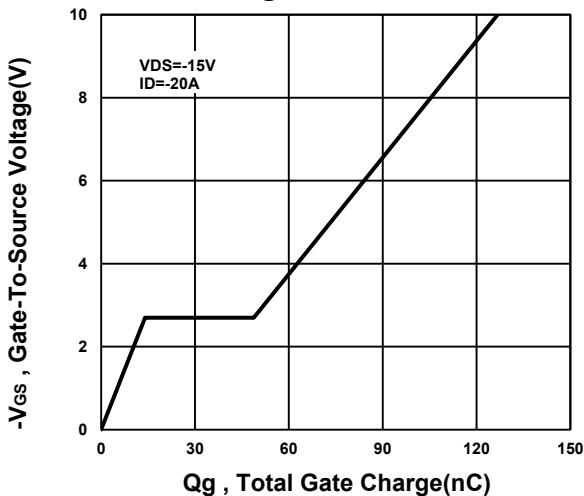
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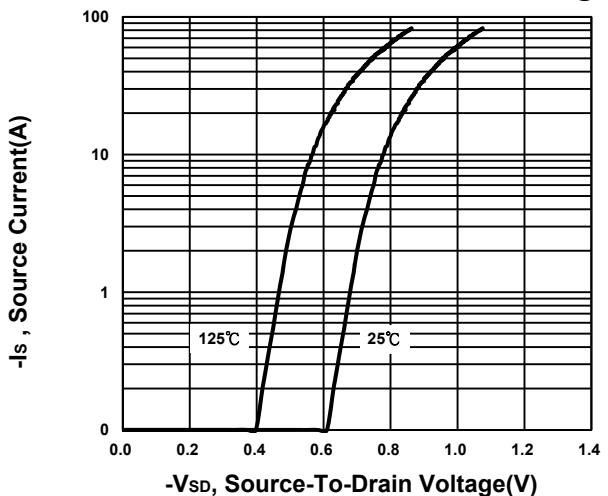
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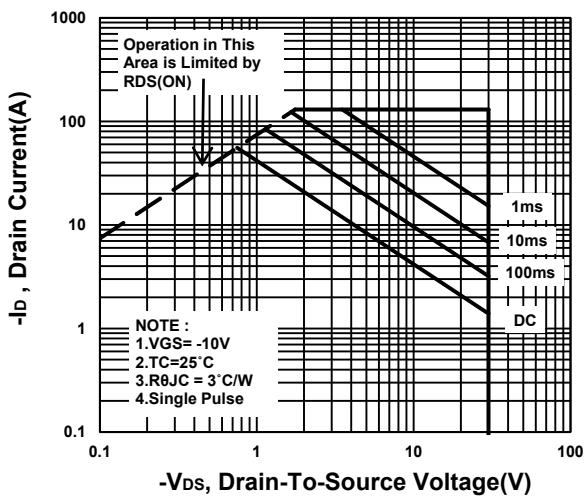
Gate charge Characteristics



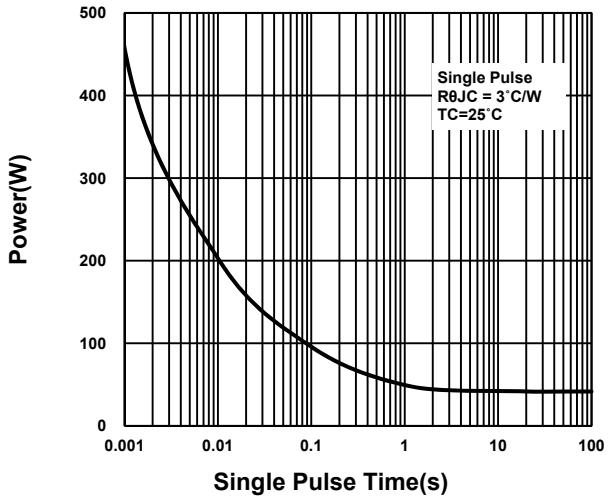
Source-Drain Diode Forward Voltage



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

