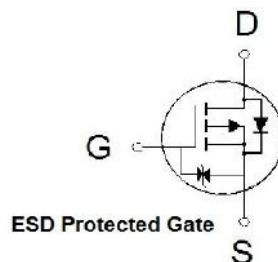


PZ2003EEA

P-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	20mΩ @ $V_{GS} = -10V$	-28A



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 25	
Continuous Drain Current	I_D	-28	A
		-17	
		-8.4	
		-7	
Pulsed Drain Current ¹	I_{DM}	-70	mJ
Avalanche Current	I_{AS}	-30	
Avalanche Energy	E_{AS}	45	mJ
Power Dissipation	P_D	25	W
		10	
		2.2	
		1.4	
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C



PZ2003EEA

P-Channel Logic Level Enhancement Mode MOSFET

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	Steady-State	$R_{\theta JA}$		55	$^{\circ}\text{C} / \text{W}$
Junction-to-Case	Steady-State	$R_{\theta JC}$		5	

¹Pulse width limited by maximum junction temperature.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}\text{C}$.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})DSS}$	$V_{GS} = 0V, I_D = -250\mu\text{A}$	-30			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1	-1.6	-3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 16V$			± 30	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 125^{\circ}\text{C}$			-10	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = -5V, V_{GS} = -10V$	-70			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = -4.5V, I_D = -7A$		28	35	$\text{m}\Omega$
		$V_{GS} = -10V, I_D = -8A$		17.6	20	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -8A$		20		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1\text{MHz}$		1470		pF
Output Capacitance	C_{oss}			238		
Reverse Transfer Capacitance	C_{rss}			215		
Gate Resistance	R_g	$V_{GS} = 0V, V_{DS} = 0V, f = 1\text{MHz}$		3		Ω
Total Gate Charge ²	$Q_g(V_{GS}=-10V)$	$V_{DS} = -15V, I_D = -8A$		34		nC
	$Q_g(V_{GS}=-4.5V)$			18		
Gate-Source Charge ²	Q_{gs}			5.3		
Gate-Drain Charge ²	Q_{gd}			8.4		
Turn-On Delay Time ²	$t_{d(on)}$	$V_{DS} = -15V, I_D \approx -8A, V_{GS} = -10V, R_{GS} = 6\Omega$		10		nS
Rise Time ²	t_r			6		
Turn-Off Delay Time ²	$t_{d(off)}$			34		
Fall Time ²	t_f			20		

PZ2003EEA

P-Channel Logic Level Enhancement Mode MOSFET

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ\text{C}$)

Continuous Current	I_S			-28	A
Forward Voltage ¹	V_{SD}	$I_F = -8\text{A}, V_{GS} = 0\text{V}$		-1.2	V
Reverse Recovery Time	t_{rr}	$I_F = -8\text{A}, dI_F/dt = 100\text{A} / \mu\text{s}$	17		nS
Reverse Recovery Charge	Q_{rr}		7		nC

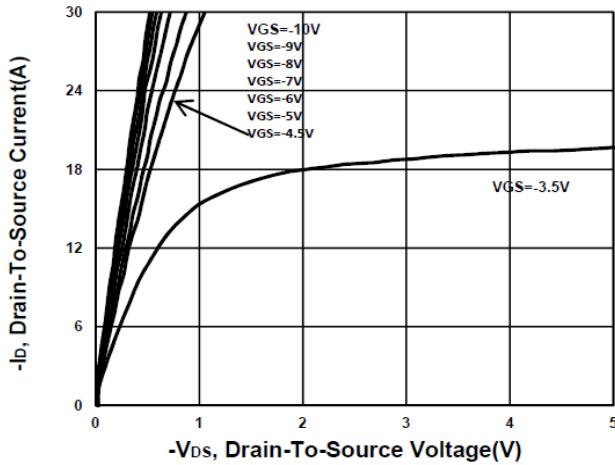
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

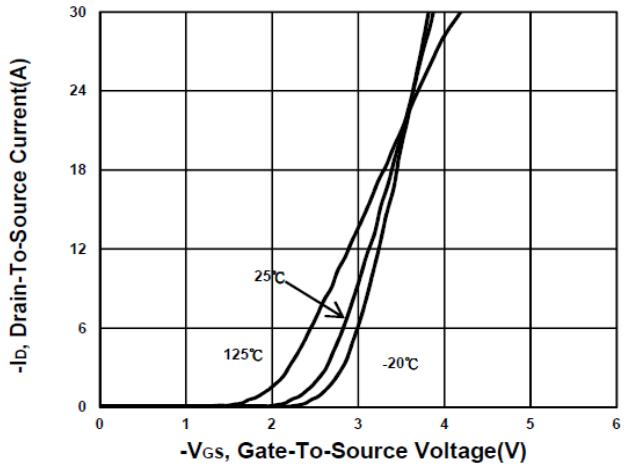
PZ2003EEA

P-Channel Logic Level Enhancement Mode MOSFET

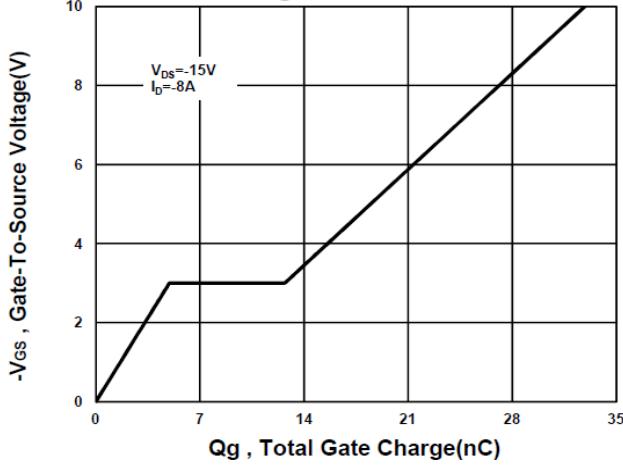
Output Characteristics



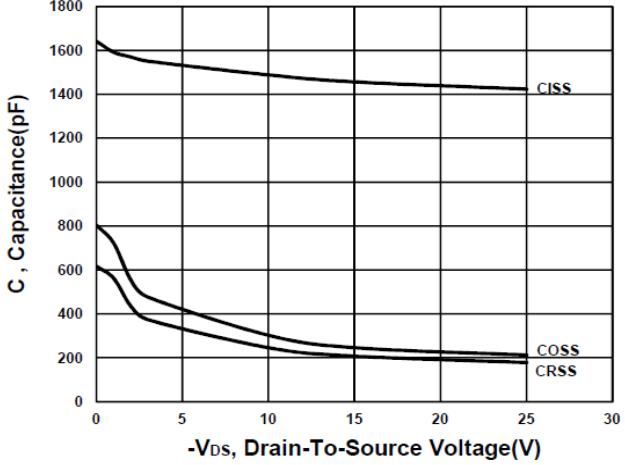
Transfer Characteristics



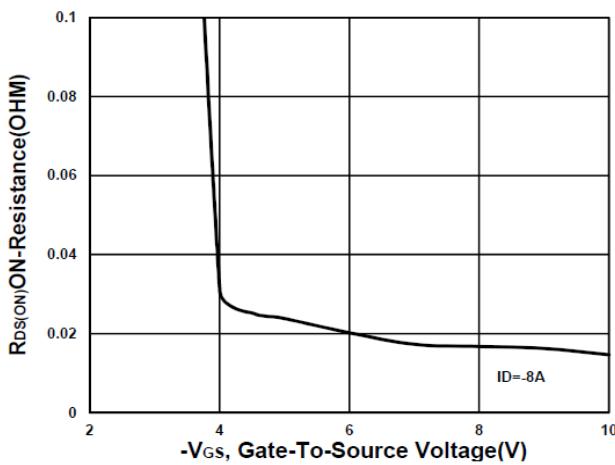
Gate charge Characteristics



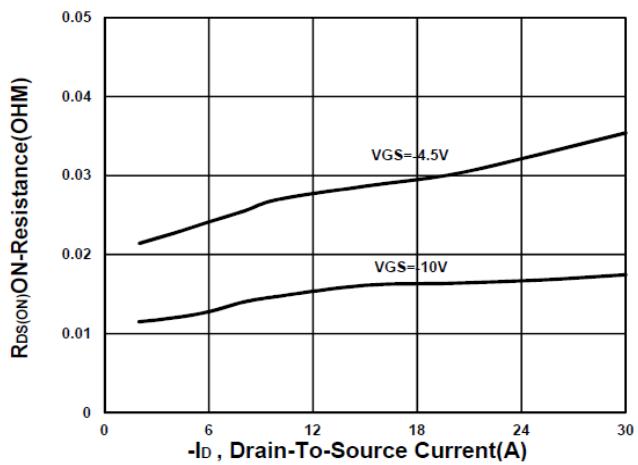
Capacitance Characteristic



On-Resistance VS Gate-To-Source

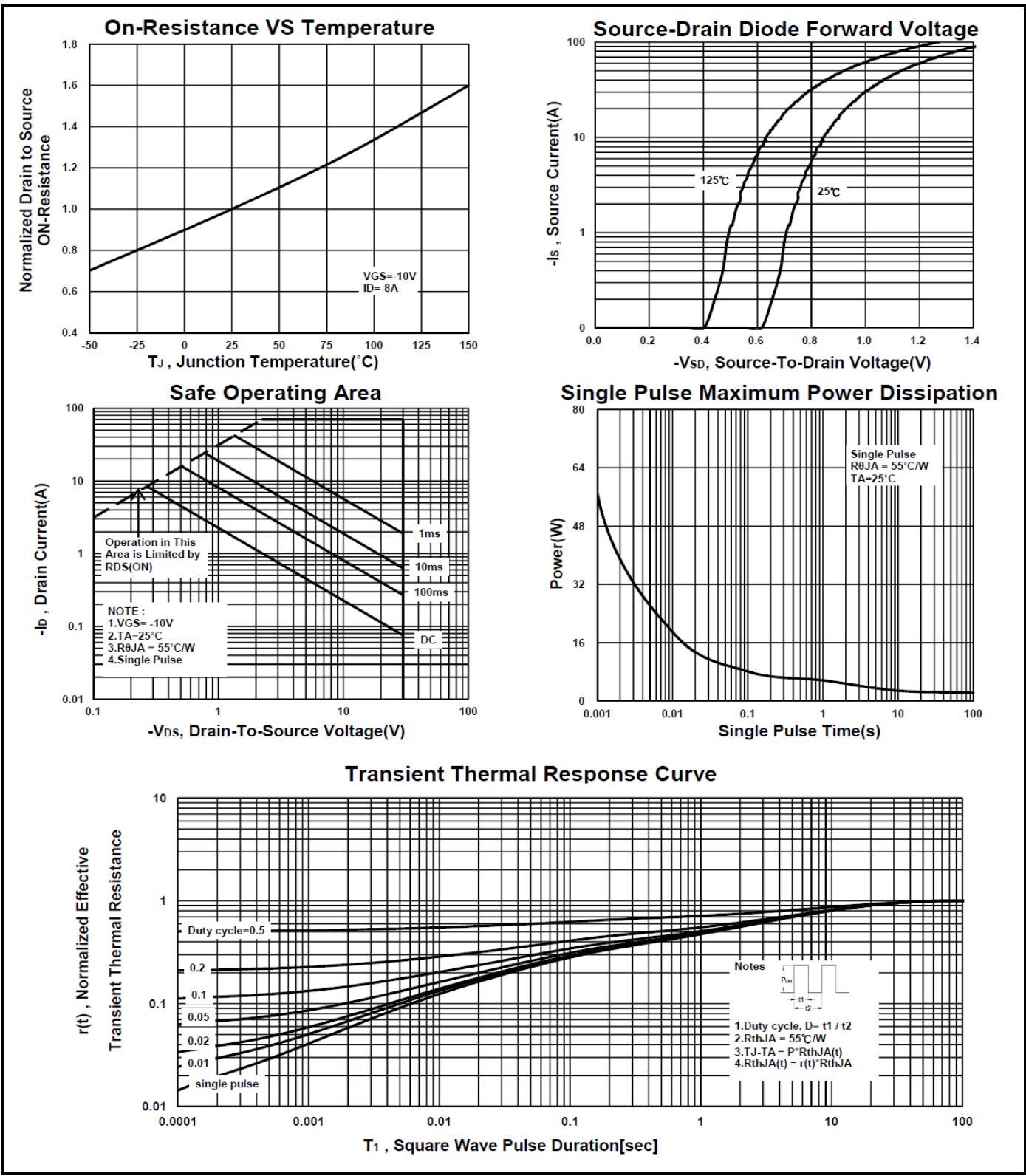


On-Resistance VS Drain Current



PZ2003EEA

P-Channel Logic Level Enhancement Mode MOSFET



PZ2003EEA

P-Channel Logic Level Enhancement Mode MOSFET

Package Dimension

PDFN 3x3P MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	3		3.6	I	0.7		1.12
B	2.88		3.2	J	0.1		0.33
C	2.9		3.2	K	0.6		
D	1.98		2.69	L	0°	10°	12°
E	3		3.6	M	0.14		0.41
F	0		0.455	N	0.6		0.7
G	1.47		2.2	O	0.12		0.36
H	0.15		0.56	P	0		0.2

