

# **High Voltage Transistor Surface Mount**

## **NPN Silicon**

## PZTA42T1G

#### **Features**

- PZTA42T1G is Complement to PZTA92T1G
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Rating	Value	Unit
V <sub>CEO</sub>	Collector-Emitter Voltage (Open Base)	300	Vdc
V <sub>CBO</sub>	Collector-Base Voltage (Open Emitter)	300	Vdc
V <sub>EBO</sub>	Emitter-Base Voltage (Open Collector)	6.0	Vdc
I <sub>C</sub>	Collector Current (DC)	500	mAdc
P <sub>D</sub>	Total Power Dissipation @ T <sub>A</sub> = 25°C (Note 1)	1.5	W
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
TJ	Junction Temperature	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Device mounted on a FR-4 glass epoxy printed circuit board

1.575 in x 1.575 in x 0.0625 in; mounting pad for the collector lead = 0.93 sq in.

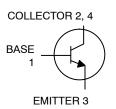
#### THERMAL CHARACTERISTICS

Symbol	Characteristic	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 2)	83.3	°C/W

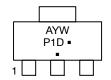
2. Device mounted on a FR-4 glass epoxy printed circuit board 1.575 in x 1.575 in x 0.0625 in; mounting pad for the collector lead = 0.93 sq in.

# **SOT-223 PACKAGE NPN SILICON** HIGH VOLTAGE TRANSISTOR SURFACE MOUNT





#### **MARKING DIAGRAM**



P<sub>1</sub>D = Specific Device Code = Assembly Location Α

= Year W = Work Week = Pb-Free Package

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
PZTA42T1G	SOT-223 (Pb-Free)	1,000 / Tape & Reel
SPZTA42T1G	SOT-223 (Pb-Free)	1,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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### PZTA42T1G

## **ELECTRICAL CHARACTERISTICS** (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Characteristics	Min	Max	Unit
FF CHARAC	CTERISTICS			
V <sub>(BR)CEO</sub>	Collector-Emitter Breakdown Voltage (Note 3) $(I_C = 1.0 \text{ mAdc}, I_B = 0)$	300	_	Vdc
V <sub>(BR)CBO</sub>	Collector-Base Breakdown Voltage $(I_C = 100 \mu Adc, I_E = 0)$	300	_	Vdc
V <sub>(BR)EBO</sub>	Emitter-Base Breakdown Voltage ( $I_E = 100 \mu Adc, I_C = 0$ )	6.0	_	Vdc
I <sub>CBO</sub>	Collector-Base Cutoff Current $(V_{CB} = 200 \text{ Vdc}, I_E = 0)$	-	0.1	μAdc
I <sub>EBO</sub>	Emitter-Base Cutoff Current $(V_{BE} = 6.0 \text{ Vdc}, I_C = 0)$	-	0.1	μAdc
N CHARAC	TERISTICS		•	
h <sub>FE</sub>	DC Current Gain	25 40 40	- - -	-
YNAMIC CH	ARACTERISTICS			
f <sub>T</sub>	Current-Gain – Bandwidth Product (I <sub>C</sub> = 10 mAdc, V <sub>CE</sub> = 20 Vdc, f = 100 MHz)	50	_	MHz
C <sub>re</sub>	Feedback Capacitance (V <sub>CB</sub> = 20 Vdc, I <sub>E</sub> = 0, f = 1.0 MHz)	-	3.0	pF
V <sub>CE(sat)</sub>	Collector-Emitter Saturation Voltage (I <sub>C</sub> = 20 mAdc, I <sub>B</sub> = 2.0 mAdc)	-	0.5	Vdc
V <sub>BE(sat)</sub>	Base-Emitter Saturation Voltage (I <sub>C</sub> = 20 mAdc, I <sub>B</sub> = 2.0 mAdc)	_	0.9	Vdc

<sup>3.</sup> Pulse Test Conditions,  $t_p$  = 300  $\mu$ s,  $\delta$  0.02.

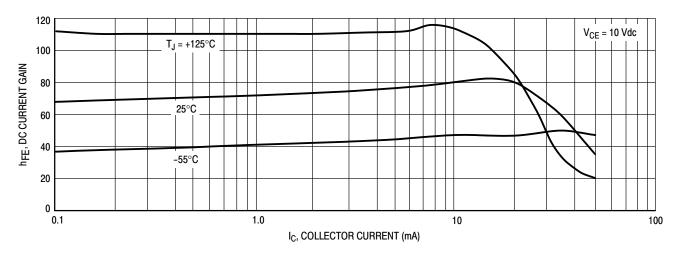


Figure 1. DC Current Gain

#### PZTA42T1G

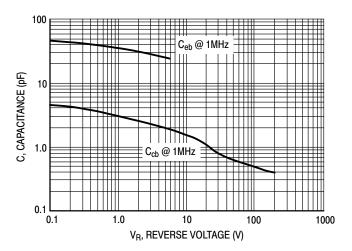
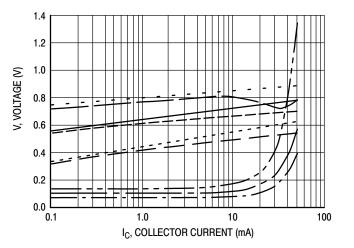


Figure 2. Capacitance



 V<sub>CE</sub>(sat)
 @ 25°C, I<sub>C</sub>/I<sub>B</sub> = 10

 V<sub>CE</sub>(sat)
 @ 125°C, I<sub>C</sub>/I<sub>B</sub> = 10

 V<sub>CE</sub>(sat)
 @ -55°C, I<sub>C</sub>/I<sub>B</sub> = 10

 V<sub>BE</sub>(sat)
 @ 25°C, I<sub>C</sub>/I<sub>B</sub> = 10

 V<sub>BE</sub>(sat)
 @ 125°C, I<sub>C</sub>/I<sub>B</sub> = 10

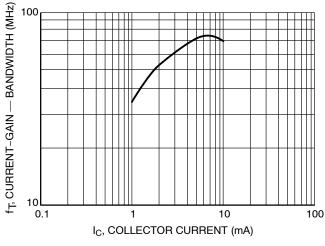
 V<sub>BE</sub>(sat)
 @ -55°C, I<sub>C</sub>/I<sub>B</sub> = 10

 V<sub>BE</sub>(on)
 @ 25°C, V<sub>CE</sub> = 10 V

 V<sub>BE</sub>(on)
 @ 125°C, V<sub>CE</sub> = 10 V

 V<sub>BE</sub>(on)
 @ -55°C, V<sub>CE</sub> = 10 V

Figure 3. "ON" Voltages



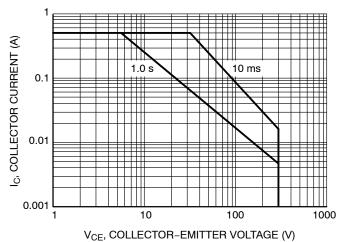


Figure 4. Current Gain Bandwidth Product

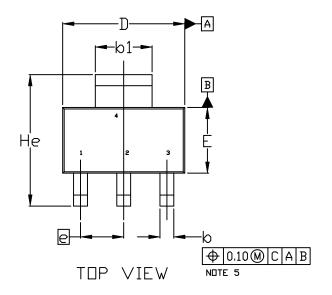
Figure 5. Safe Operating Area

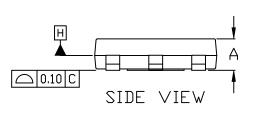


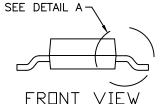


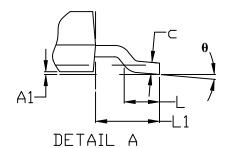
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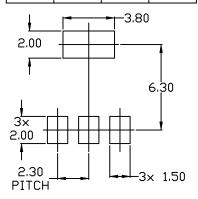




#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
- 4. DATUMS A AND B ARE DETERMINED AT DATUM H.
- 5. AI IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
- 6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS 6 AND 61.

	MILLIMETERS		
DIM	MIN.	N□M.	MAX.
Α	1.50	1.63	1.75
A1	0.02	0.06	0.10
Ø	0.60	0.75	0.89
b1	2.90	3.06	3.20
U	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
е	2.30 BSC		
L	0.20		
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°		10°



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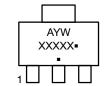
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STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

# GENERIC MARKING DIAGRAM\*



A = Assembly Location

Y = Year W = Work Week

XXXXX = Specific Device Code

= Pb-Free Package

(Note: Microdot may be in either location)
\*This information is generic. Please refer to
device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "•", may
or may not be present. Some products may

not follow the Generic Marking.

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