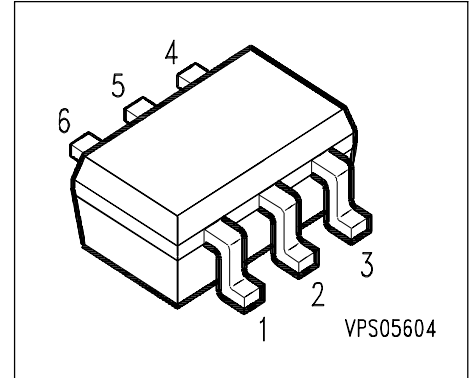
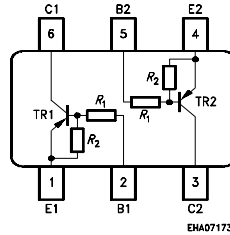


## PNP Silicon Digital Transistor Array

- Switching circuit, inverter, interface circuit, driver circuit
- Two (galvanic) internal isolated Transistors in one package
- Built in bias resistor ( $R_1=22k\Omega$ ,  $R_2=22k\Omega$ )



Type	Marking	Ordering Code	Pin Configuration			Package	
BCR 191S	WOs	Q62702-C2418	1=E1	2=B1	3=C2	4=E2 5=B2 6=C1	SOT-363

### Maximum Ratings

Parameter	Symbol	Values	Unit
Collector-emitter voltage	$V_{CEO}$	50	V
Collector-base voltage	$V_{CBO}$	50	
Emitter-base voltage	$V_{EBO}$	10	
Input on Voltage	$V_{i(on)}$	30	
DC collector current	$I_C$	100	mA
Total power dissipation, $T_S = 115^\circ\text{C}$	$P_{tot}$	250	mW
Junction temperature	$T_j$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	- 65 ... + 150	

### Thermal Resistance

Junction ambient <sup>1)</sup>	$R_{thJA}$	$\leq 275$	K/W
Junction - soldering point	$R_{thJS}$	$\leq 140$	

1) Package mounted on pcb 40mm x 40mm x 1.5mm / 0.5cm<sup>2</sup> Cu

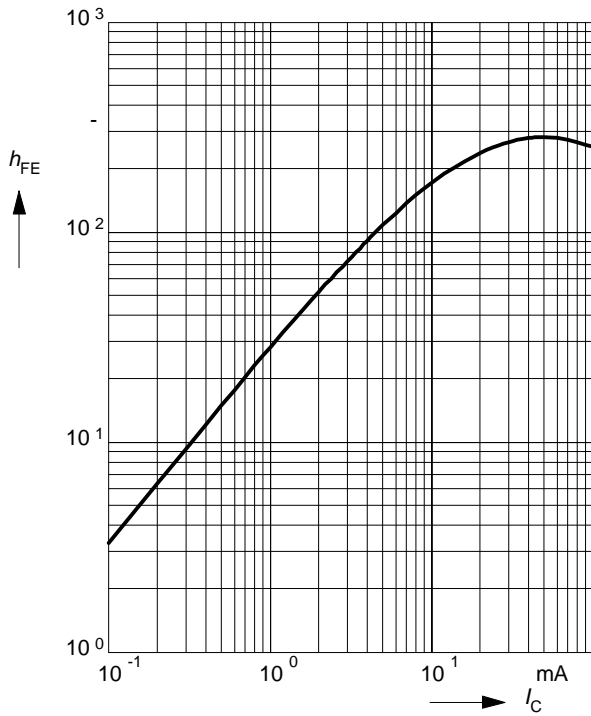
## Electrical Characteristics at $T_A=25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>DC Characteristics</b>					
Collector-emitter breakdown voltage $I_C = 100 \mu\text{A}, I_B = 0$	$V_{(BR)CEO}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10 \mu\text{A}, I_B = 0$	$V_{(BR)CBO}$	50	-	-	
Collector cutoff current $V_{CB} = 40 \text{ V}, I_E = 0$	$I_{CBO}$	-	-	100	nA
Emitter cutoff current $V_{EB} = 10 \text{ V}, I_C = 0$	$I_{EBO}$	-	-	350	$\mu\text{A}$
DC current gain $I_C = 5 \text{ mA}, V_{CE} = 5 \text{ V}$	$h_{FE}$	50	-	-	-
Collector-emitter saturation voltage 1) $I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$	$V_{CEsat}$	-	-	0.3	V
Input off voltage $I_C = 100 \mu\text{A}, V_{CE} = 5 \text{ V}$	$V_{i(off)}$	0.8	-	1.5	
Input on Voltage $I_C = 2 \text{ mA}, V_{CE} = 0.3 \text{ V}$	$V_{i(on)}$	1	-	2.5	
Input resistor	$R_1$	15	22	29	$\text{k}\Omega$
Resistor ratio	$R_1/R_2$	0.9	1	1.1	-
<b>AC Characteristics</b>					
Transition frequency $I_C = 10 \text{ mA}, V_{CE} = 5 \text{ V}, f = 100 \text{ MHz}$	$f_T$	-	200	-	MHz
Collector-base capacitance $V_{CB} = 10 \text{ V}, f = 1 \text{ MHz}$	$C_{cb}$	-	3	-	pF

1) Pulse test:  $t < 300 \mu\text{s}$ ;  $D < 2\%$

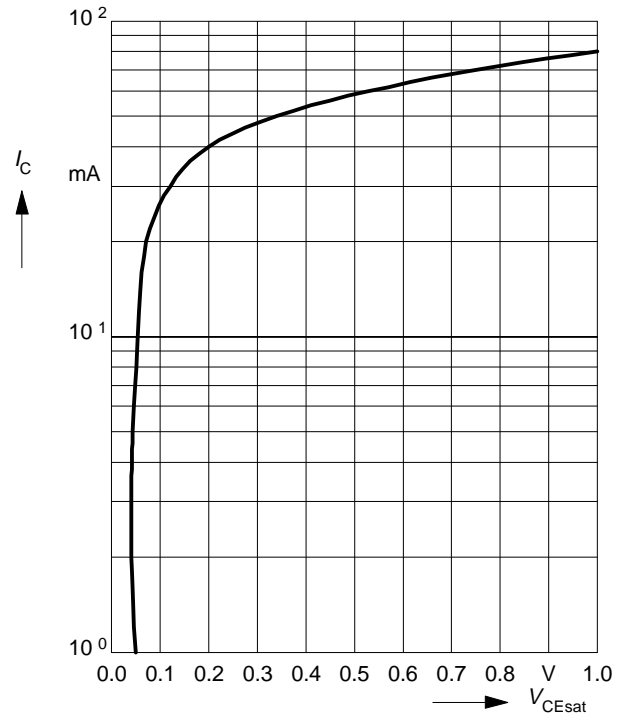
### DC Current Gain $h_{FE} = f(I_C)$

$V_{CE} = 5V$  (common emitter configuration)



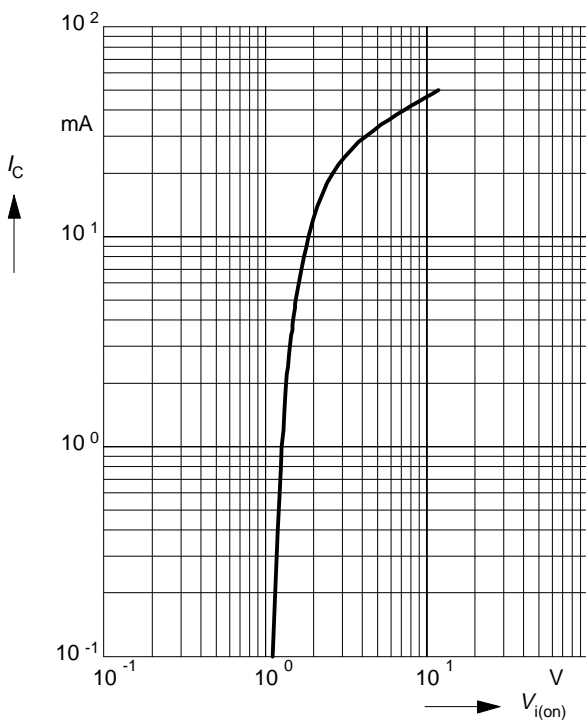
### Collector-Emitter Saturation Voltage

$V_{CEsat} = f(I_C), h_{FE} = 20$



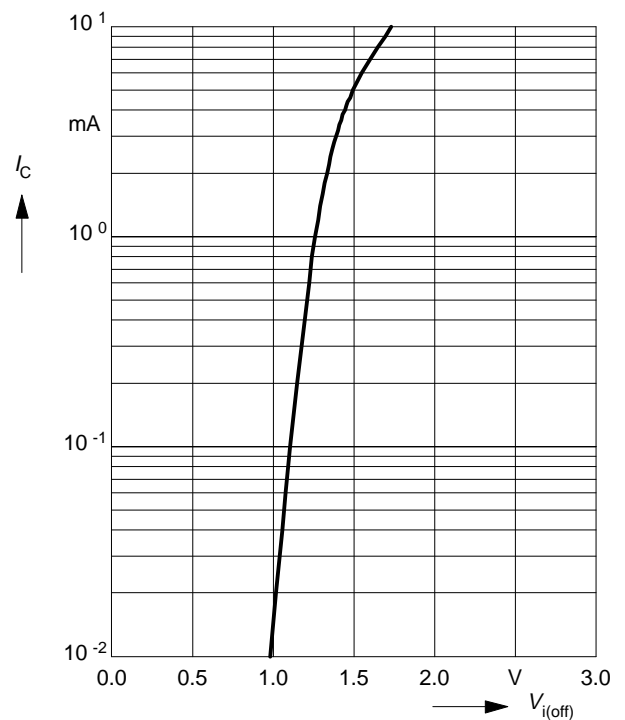
### Input on Voltage $V_{i(on)} = f(I_C)$

$V_{CE} = 0.3V$  (common emitter configuration)



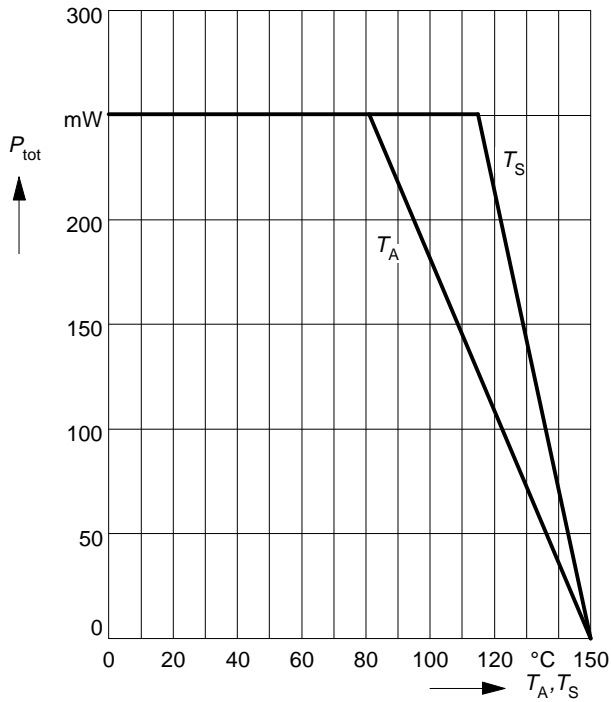
### Input off voltage $V_{i(off)} = f(I_C)$

$V_{CE} = 5V$  (common emitter configuration)

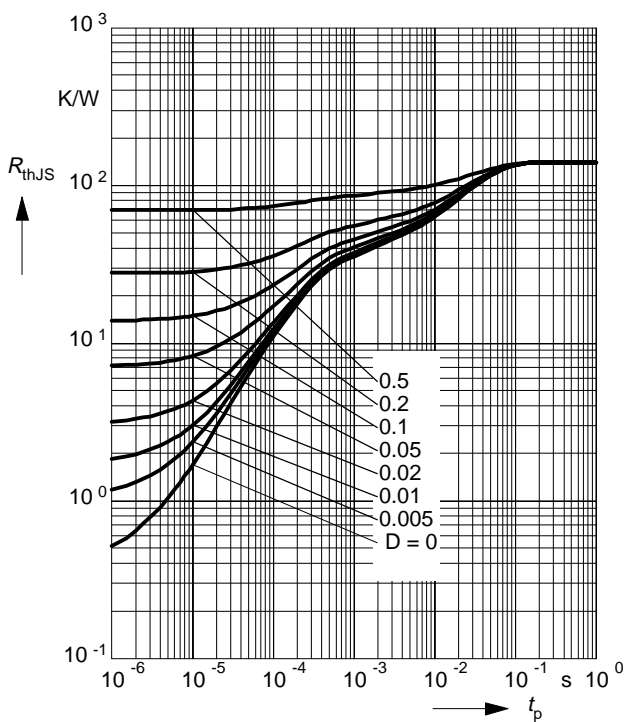


**Total power dissipation  $P_{tot} = f(T_A^*; T_S)$**

\* Package mounted on epoxy



**Permissible Pulse Load  $R_{thJS} = f(t_p)$**



**Permissible Pulse Load  $P_{totmax} / P_{totDC} = f(t_p)$**

