QA3111N6N

30V Asymmetric Dual N-Channel Power MOSFET

General Description

The QA3111N6N is a high performance trench Dual N-channel asymmetric MOSFET which utilizes extremely high cell density to provide low Rdson and gate charge characteristics. It is ideally suited to support synchronous buck converter applications.

The QA3111N6N meets RoHS and Green Product requirements while supporting full function reliability.

Features

- ✓ Advanced high cell density Trench technology
- ✓ Super Low Gate Charge
- ✓ Excellent CdV/dt effect decline
- ✓ Green Device Available

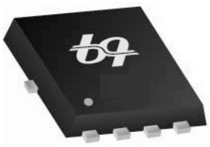
Product Summary

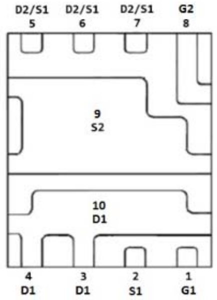
	V_{DS}	$R_{DS(ON)}$ max (V_{GS}=10V)	I_D (T_C=25 °C)
Die1	30V	5.6mΩ	59A
Die2	30V	1.3mΩ	135A

Applications

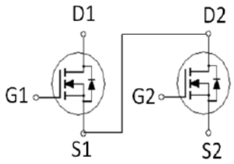
- ✓ High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- ✓ Networking DC-DC Power System
- ✓ CCFL Back-light Inverter

Pin Configuration

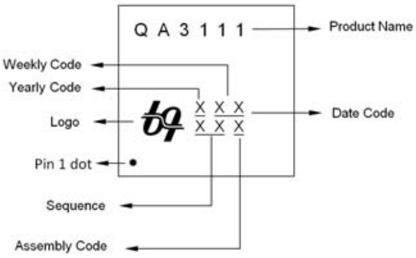




BOTTOM VIEW



Ordering Information

Order Number	Package Type	Top Marking
QA3111N6N	DFN5X6	

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		Die1	Die2	
V_{DS}	Drain-Source Voltage	30	30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_C=25°C	Continuous Drain Current, V_{GS} @ 10V[1]	59	135	A
I_D@T_C=100°C	Continuous Drain Current, V_{GS} @ 10V[1]	37	85	A
I_D@T_A=25°C	Continuous Drain Current, V_{GS} @ 10V[1]	15	31	A
I_D@T_A=70°C	Continuous Drain Current, V_{GS} @ 10V[1]	12	25	A
I_{DM}	Pulsed Drain Current[2]	118	270	A
EAS	Single Pulse Avalanche Energy[3]	58.5	391.6	mJ
I_{AS}	Avalanche Current	34.2	88.5	A
P_D@T_C=25°C	Total Power Dissipation[4]	31	40	W
P_{DSM}@T_A=25°C	Total Power Dissipation[4]	2	2	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C

Thermal Data

Symbol	Parameter	Die1	Die2	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient[1]	62	56	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	4	3.1	°C/W

Die1 N-Channel Electrical Characteristics

Die1 N-Channel Electrical Characteristics: (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	--	--	V
△BV_{DSS} /△T_J	BVDSS Temperature Coefficient	Reference to 25°C, I_D=1mA	--	0.016	--	V/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=30A	--	4.3	5.6	mΩ
		V_{GS}=4.5V, I_D=15A	--	6.0	8.4	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS}, I_D =250uA	1.2	--	2.5	V
△$V_{GS(th)}$ /△T_J	$V_{GS(th)}$ Temperature Coefficient		--	-3.7	--	mV/°C
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	--	--	1	uA
		V_{DS}=24V, V_{GS}=0V,T_J=55°C	--	--	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=± 20V, V_{DS}=0V	--	--	±100	nA
gfs	Forward Transconductance	V_{DS}=5V, I_D=30A	--	33	--	S
R_g	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz	--	1.6	--	Ω
Q_g	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=15A	--	14.5	--	nC
Q_g	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=15A	--	6.7	--	nC
Q_{gs}	Gate-Source Charge		--	2.5	--	
Q_{gd}	Gate-Drain Charge		--	2.2	--	
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=15V, V_{GS}=10V, R_G=3.3Ω, I_D=15A	--	6.5	--	ns
t_r	Rise Time		--	52.1	--	
$t_{d(off)}$	Turn-Off Delay Time		--	16.0	--	
t_f	Fall Time		--	2.7	--	
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz	--	850	--	pF
C_{oss}	Output Capacitance		--	280	--	
C_{rss}	Reverse Transfer Capacitance		--	18	--	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy[5]	V_{DD}=25V, L=0.1mH , I_{AS}=24A	28.8	--	--	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current [1,6]	V_G=V_D=0V, Force Current	--	--	59	A
I_{SM}	Pulsed Source Current[2,6]		--	--	118	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V, I_S=1A	--	--	1.2	V
t_{rr}	Reverse Recovery Time	I_F=15A, di/dt=100A/μs, T_J=25ºC	--	20.7	--	nS
Q_{rr}	Reverse Recovery Charge		--	11.1	--	nC

Note:

1. Test data conducted with surface mount attachment to 1 inch^2, FR-4 board utilizing 2oz copper
2. Pulse Test. Pulse width ≦ 300uS, duty cycle ≦ 2%
3. EAS data is a maximum rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH
4. The power dissipation is limited by a 150°C maximum junction temperature
5. The Min. value is 100% EAS tested guarantee
6. The data is theoretically the same as I_D and I_{DM}. In real applications, it will be limited by total power

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Die2 N-Channel Electrical Characteristics

Die2 N-Channel Electrical Characteristics: (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	--	--	V
$\triangle BV_{DSS}$ /$\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25°C, I_D=1mA	--	0.016	--	V/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=30A	--	1.0	1.3	mΩ
		V_{GS}=4.5V, I_D=15A	--	1.3	1.8	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS}, I_D =250uA	1.2	--	2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		--	-4.9	--	mV/°C
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	--	--	1	uA
		V_{DS}=24V, V_{GS}=0V,T_J=55°C	--	--	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=± 20V, V_{DS}=0V	--	--	±100	nA
gfs	Forward Transconductance	V_{DS}=5V, I_D=30A	--	83	--	S
R_g	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz	--	0.6	--	Ω
Q_g	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=15A	--	52.2	--	nC
Q_g	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=15A	--	23.5	--	nC
Q_{gs}	Gate-Source Charge		--	10.8	--	
Q_{gd}	Gate-Drain Charge		--	4.7	--	
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=15V, V_{GS}=10V, R_G=3.3Ω, I_D=15A	--	11.4	--	ns
t_r	Rise Time		--	46.9	--	
$t_{d(off)}$	Turn-Off Delay Time		--	35.9	--	
t_f	Fall Time		--	5.9	--	
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz	--	4040	--	pF
C_{oss}	Output Capacitance		--	1310	--	
C_{rss}	Reverse Transfer Capacitance		--	65	--	

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Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy[5]	V_{DD}=25V, L=0.1mH, I_{AS}=63A	198.45	--	--	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current [1,6]	V_G=V_D=0V, Force Current	--	--	135	A
I_{SM}	Pulsed Source Current[2,6]		--	--	270	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V, I_S=1A	--	--	1.2	V
t_{rr}	Reverse Recovery Time	I_F=15A, di/dt=100A/μs, T_J=25ºC	--	109	--	nS
Q_{rr}	Reverse Recovery Charge		--	126	--	nC

Note:

1. Test data conducted with surface mount attachment to 1 inch^2, FR-4 board utilizing 2oz copper
2. Pulse Test. Pulse width ≦ 300uS, duty cycle ≦ 2%
3. EAS data is a maximum rating. The test condition is V_{DD}=50V, V_{GS}=10V, L=0.1mH
4. The power dissipation is limited by a 150°C maximum junction temperature
5. The Min. value is 100% EAS tested guarantee
6. The data is theoretically the same as I_D and I_{DM}. In real applications, it will be limited by total power

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Die1 Typical Characteristics

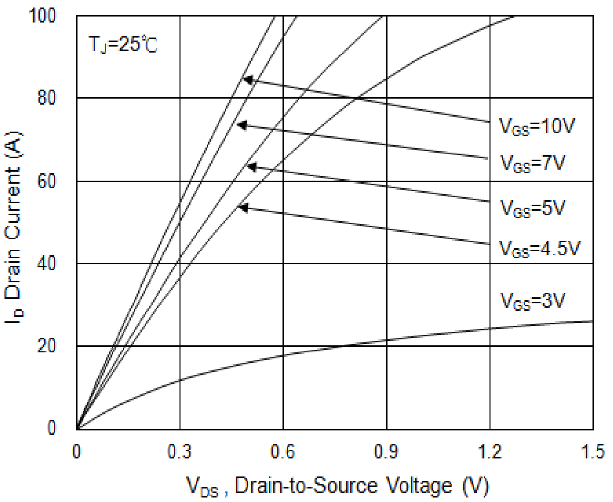

Fig.1: Typical Output Characteristics

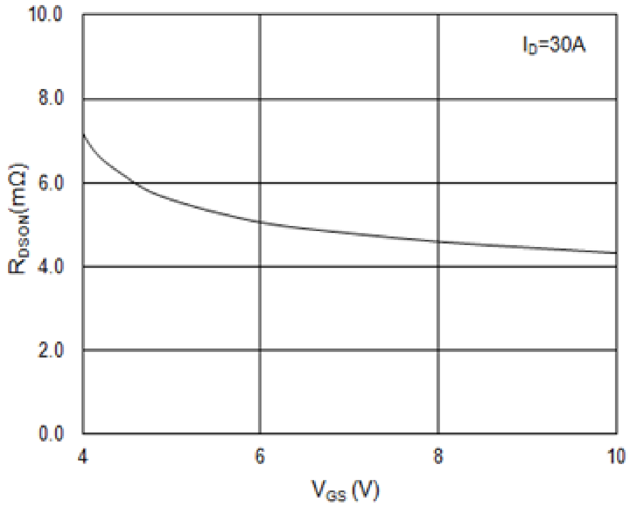

Fig.2: On-Resistance vs. Gate-Source

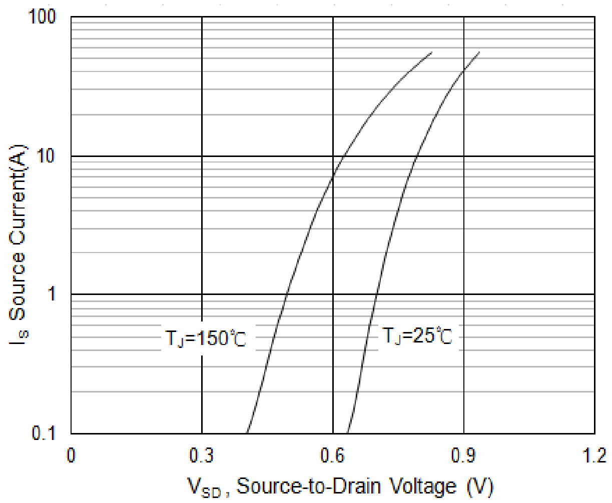

Fig.3: Forward Characteristics of Reverse

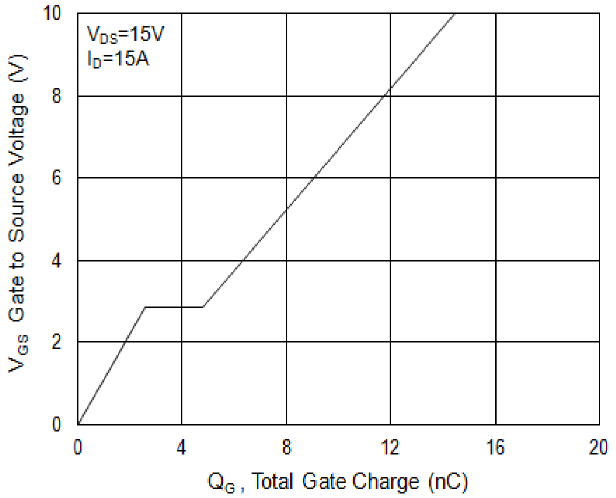

Fig.4: Gate-Charge Characteristics

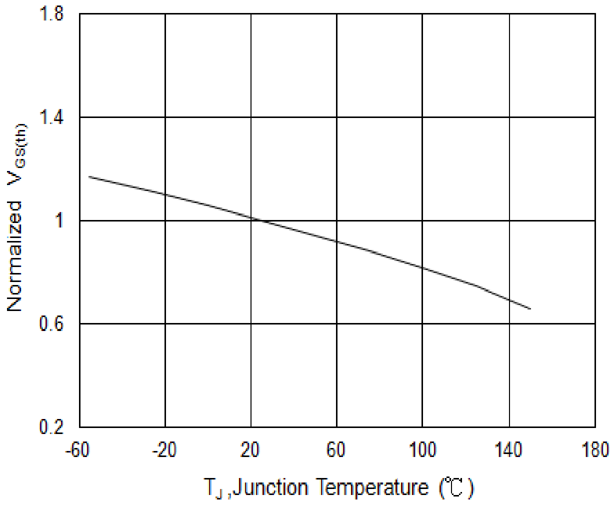

Fig.5: Normalized $V_{GS(th)}$ vs. T_J

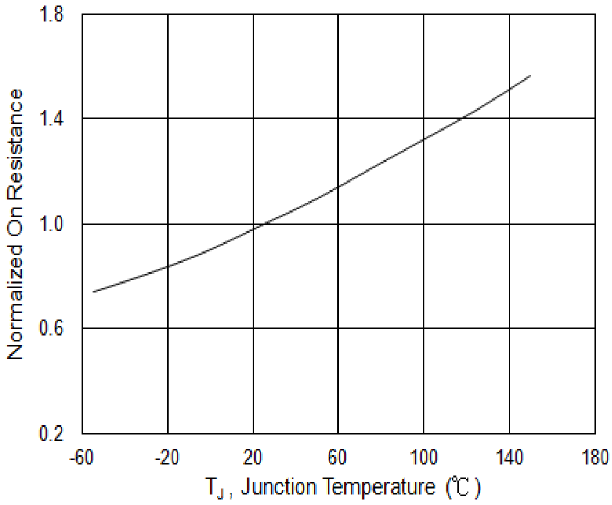

Fig.6: Normalized R_{DSON} vs. T_J

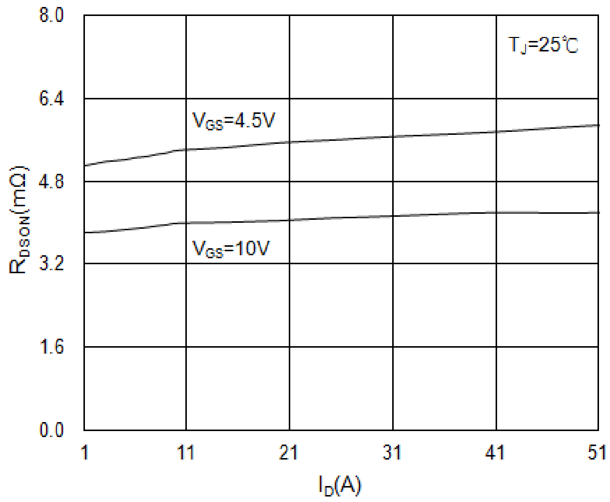

Fig.7: Drain-Source On-State Resistance

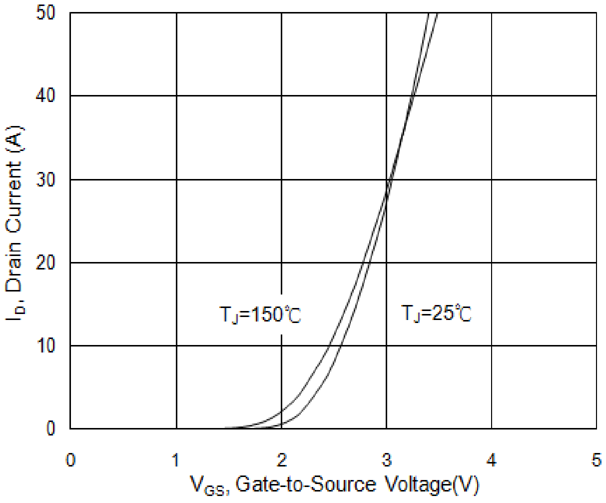

Fig.8: Transfer Characteristics

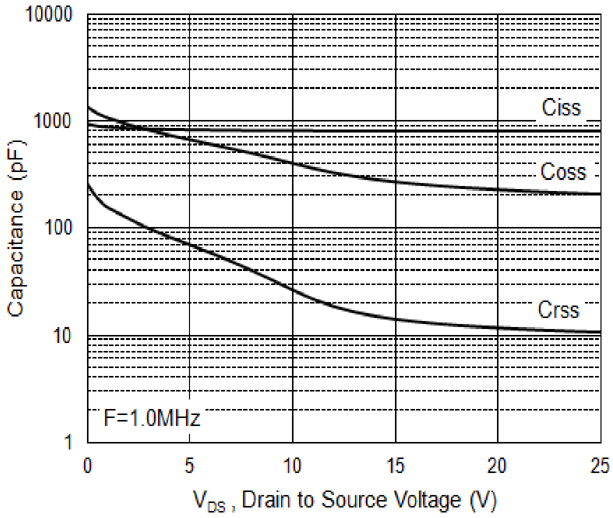

Fig.9: Capacitance

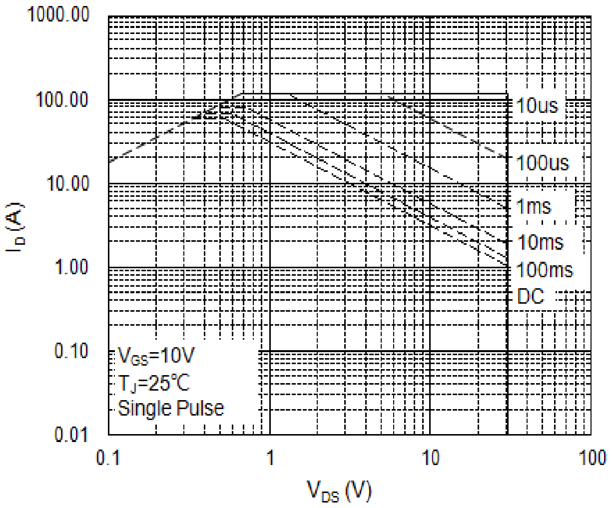

Fig.10: Safe Operating Area

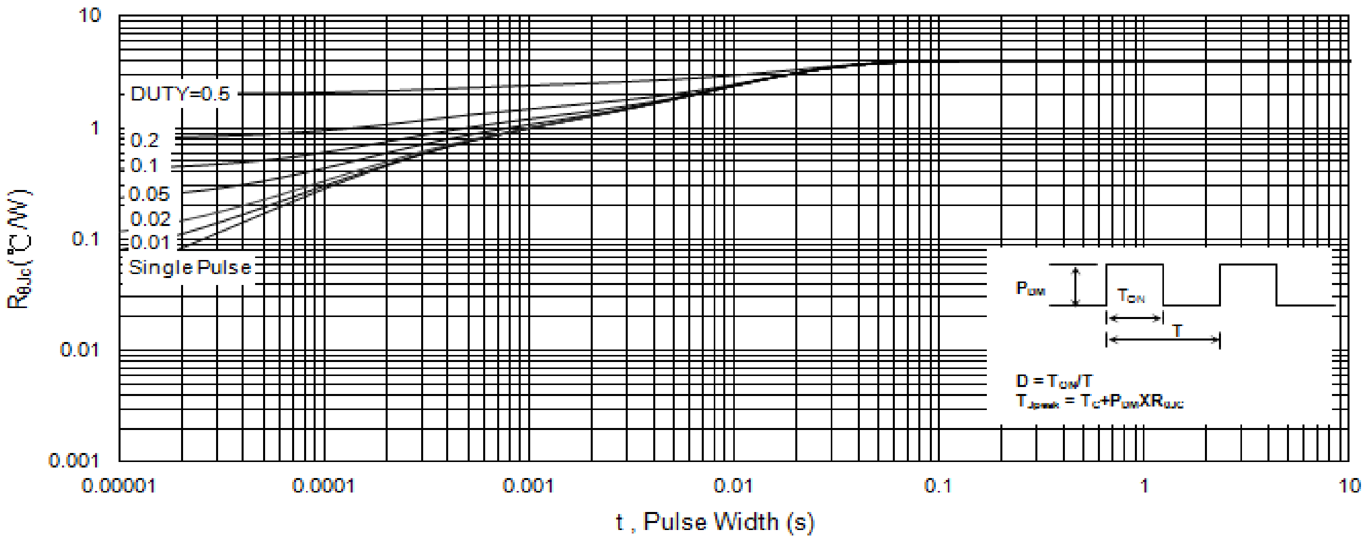

Fig.11: Transient Thermal Impedance

Die2 Typical Characteristics

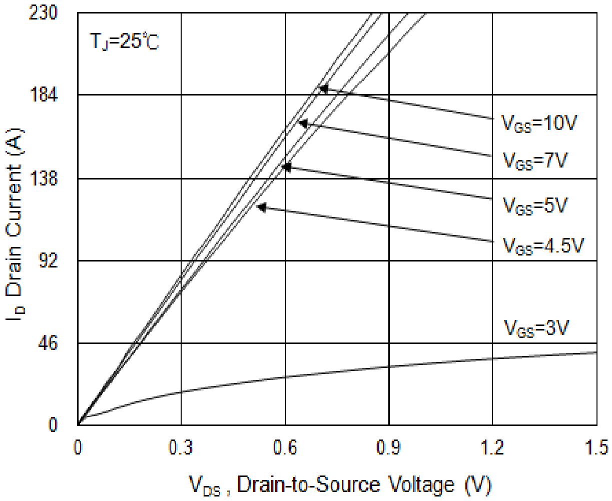

Fig.1: Typical Output Characteristics

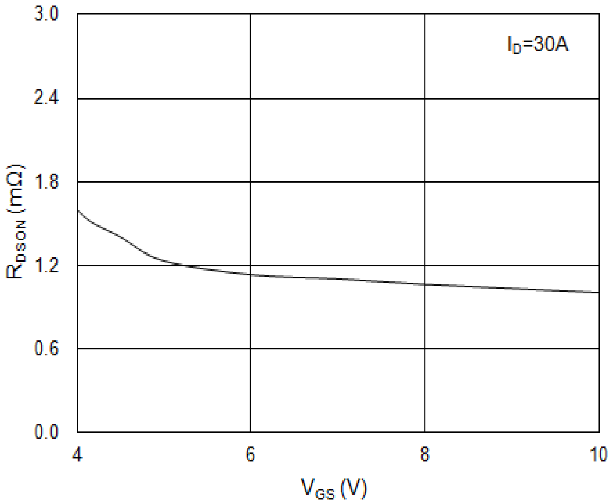

Fig.2: On-Resistance vs. Gate-Source

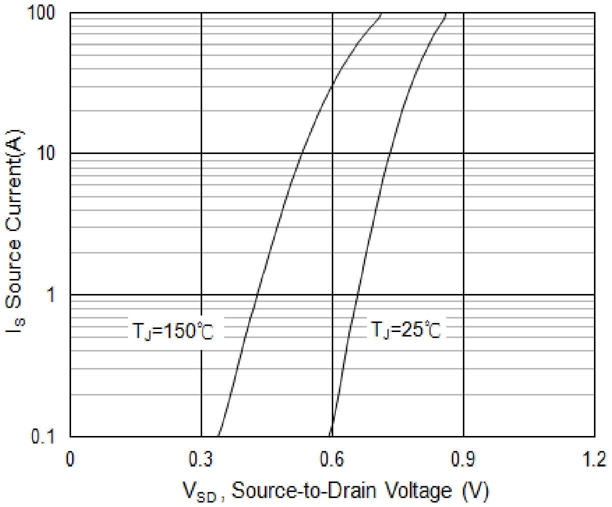

Fig.3: Forward Characteristics of Reverse

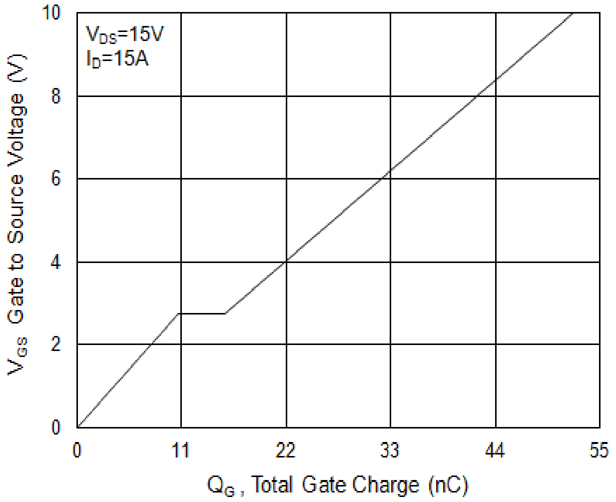

Fig.4: Gate-Charge Characteristics

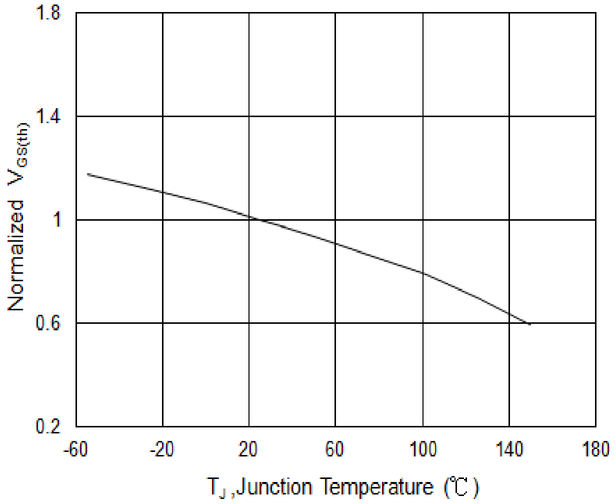

Fig.5: Normalized $V_{GS(th)}$ vs. T_J

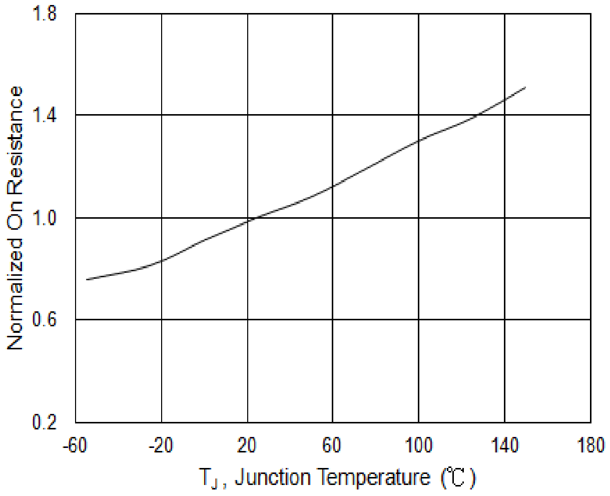

Fig.6: Normalized R_{DSON} vs. T_J

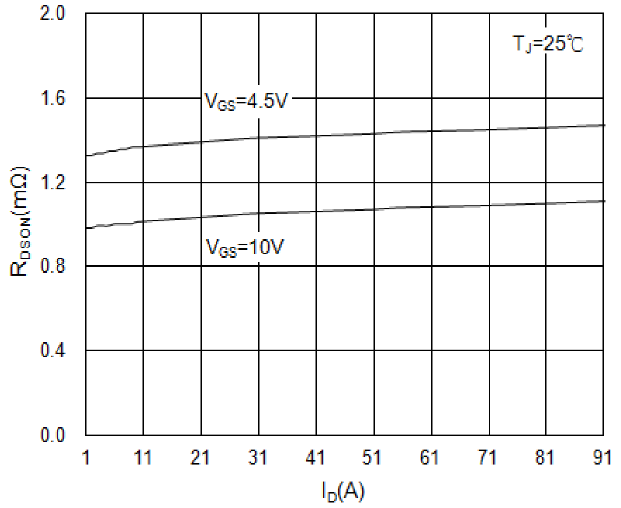

Fig.7: Drain-Source On-State Resistance

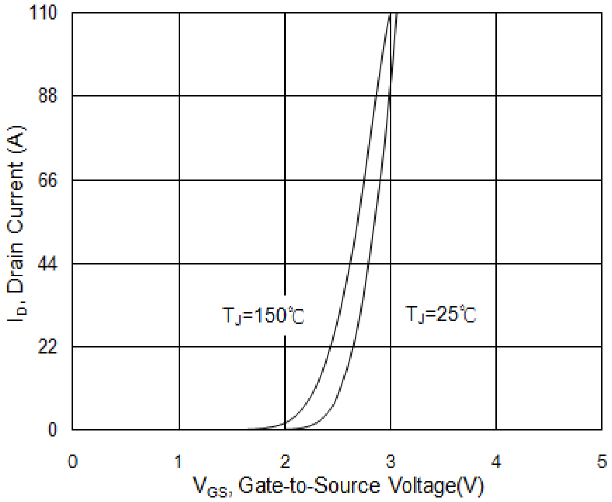

Fig.8: Transfer Characteristics

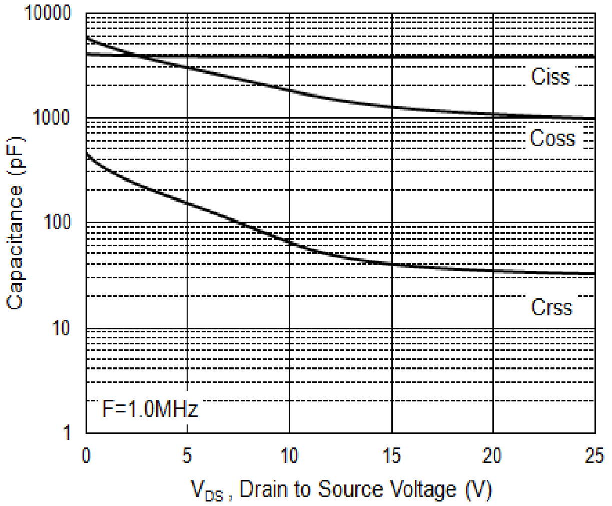

Fig.9: Capacitance

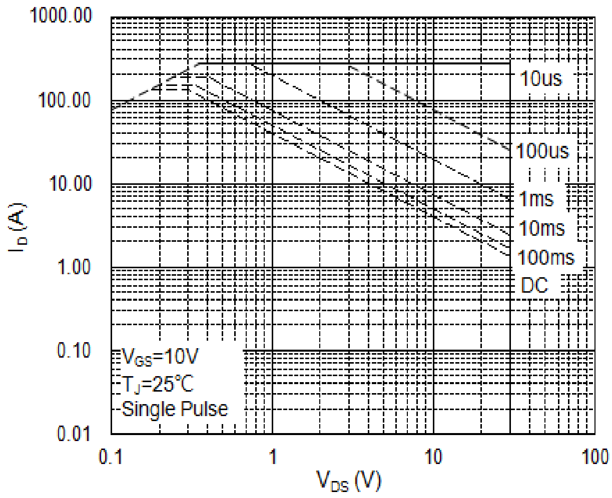

Fig.10: Safe Operating Area

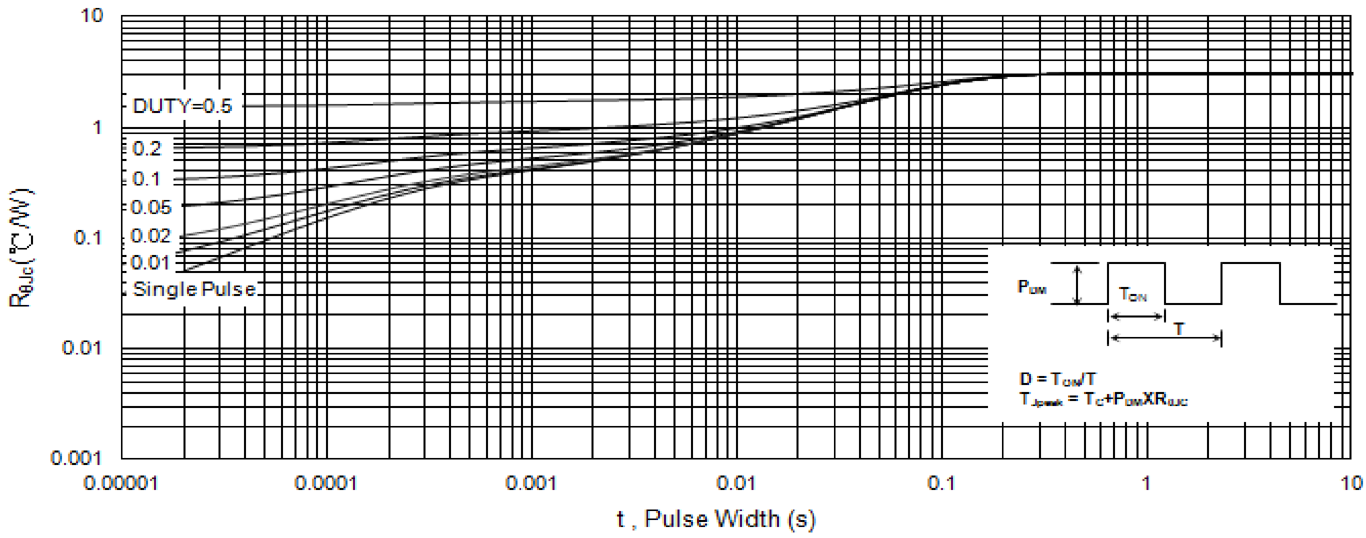

Fig.11: Transient Thermal Impedance

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uPI Semiconductor Corp.
9F.,No.5, Taiyuan 1st St. Zhubei City, Hsinchu, Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

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