Prepared by: **Date** **HC Liu** **5/19/2003**		**Doc No. QD14XL07-13** **REV.: 13** **Issue Date: 6/23/2004** **Page: 29 pages** **(Cover Page Included)**
Formal	**Quanta Display Inc.** **SPECIFICATION**	

Specification for TFT LCD Module

Model No. QD14XL07 Rev.02

Customer's Approval

Date _____

by _____

Approved By _____

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Revision History			
REV.	Date	ECN NO.	Change Content
0	7/17/2001	N/A	Preliminary specification Initiate
1	8/24/2001	N/A	Rise/Fall time update, 5 points average 150 nits
2	9/11/2001	N/A	Doc. No. change from QD141X1LH07A to QD141X1LH07A0; Modify interface cable pin assignments
3	10/23/2001	N/A	Page 3 299.5(W)x228.6(H)x5.5typ(D) change to 299.5(W) x228.6(H)x 5.5 (D) 5.5 max Page 6 WR-L16S-VF-1 (JAE) change to LVC-D20SFYG (HONDA) Pin 17~20 definition
4	1/23/2002	N/A	Update outline drawing
5	10/04/2002	N/A	Product ID Change QD141X1LH07 to QD14XL0701 Page 9 VIN=9V,VBB=5V:min 485 VIN=9V,VBB=5V:min 200 Max 300 Page 11 Brightness Control: eliminated block diagram and AC Electrical characteristic Page15 Modified EDID data structure Page 19 Optical Data:Wx=0.315±0.02 Wy=0.330±0.02 Rx=0.595±0.02 Ry=0.327±0.02 Bx=0.148±0.02 By=0.128±0.02 Luminance of white:min 150 Typ:200 Color Gamut:50% 5d $_{W}$:1.25 13d $_{W}$:1.53 Page23 Temperature cycle—Non Operating: -25? to +65? , Ramp ≦24? /min, Duration at Temp.=60min, Test cycles=50 Vibration test:1.5G 30min/each axis 1.6G random
6	01/09/2003	N/A	Update EDID data for customer request.
7	01/20/2003	N/A	Update Data – Mass: 440g.
8	5/13/2003	N/A	Update EDID Code according to customer new spec.
9	5/23/2003	N/A	Add PPID “C1787” into EDID data and errors correction.
10	7/2/2003	N/A	Update the LCD curent consumption spec.
11	11/21/2003	N/A	Update PPID from C1787 to C4011 (EDID changed).
12	1/13/2004	N/A	EDID Data Correction (Byte 17, “13” Replaced by “D”), Checksum Unchanged.
13	6/23/2004	N/A	EDID Update for Adding Ambit Inverter

1. Application

This specification applies to a color TFT-LCD module, QD14XL07.

2. Overview

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, control circuit and power supply circuit and a backlight unit. Graphics and texts can be displayed on a 1024× 3× 768 dots panel with 262,144 colors by using LVDS (Low Voltage Differential Signaling) to interface and supplying +3.3V DC supply voltage for TFT-LCD panel driving and supply voltage for backlight.

The TFT-LCD panel used for this module has very high aperture ratio. A low-reflection and higher-color-saturation type color filter is also used for this panel. Therefore, high-brightness and high-contrast image, which is suitable for the multimedia use, can be obtained by using this module.

Optimum viewing direction is 6 o'clock.

[Features]

1) High aperture panel; high-brightness or low power consumption.
2) Brilliant and high contrast image.
3) Small footprint and thin shape.
4) Light weight.
5) 100% SPWG, style B

3. Mechanical Specifications

Parameter	Specifications	Unit
Display size	36 (14.1") Diagonal	cm
Active area	285.7 (H)× 214.3 (V)	mm
Pixel format	1024 (H)× 768 (V)	Pixel
	(1 pixel = R+G+B dots)	
Pixel pitch	0.279 (H) × 0.279 (V)	mm
Pixel configuration	R,G,B vertical stripe	
Display mode	Normally white	
Unit outline dimensions (typ.)*1	299(W)× 228 (H)× 5.2(D) 5.5 Max	mm
Mass (without inverter)	Max: 440	g
Surface treatment	Anti-glare and hard-coating 3H Low reflection (~ 5%)	

*1.Note: excluding backlight cables. Outline dimensions are shown in this specification.

4. Input Terminals

4-1. TFT-LCD panel driving

CN1 (1 channel, LVDS signals – NSC/Ti standard and +3.3V DC power supply)

Using connector: FI-XB30Sx-HFxx/FI-X30Sx-HFxx/equivalent (JAE)

Corresponding connector: TBD

Interface Cable Pin Assignments

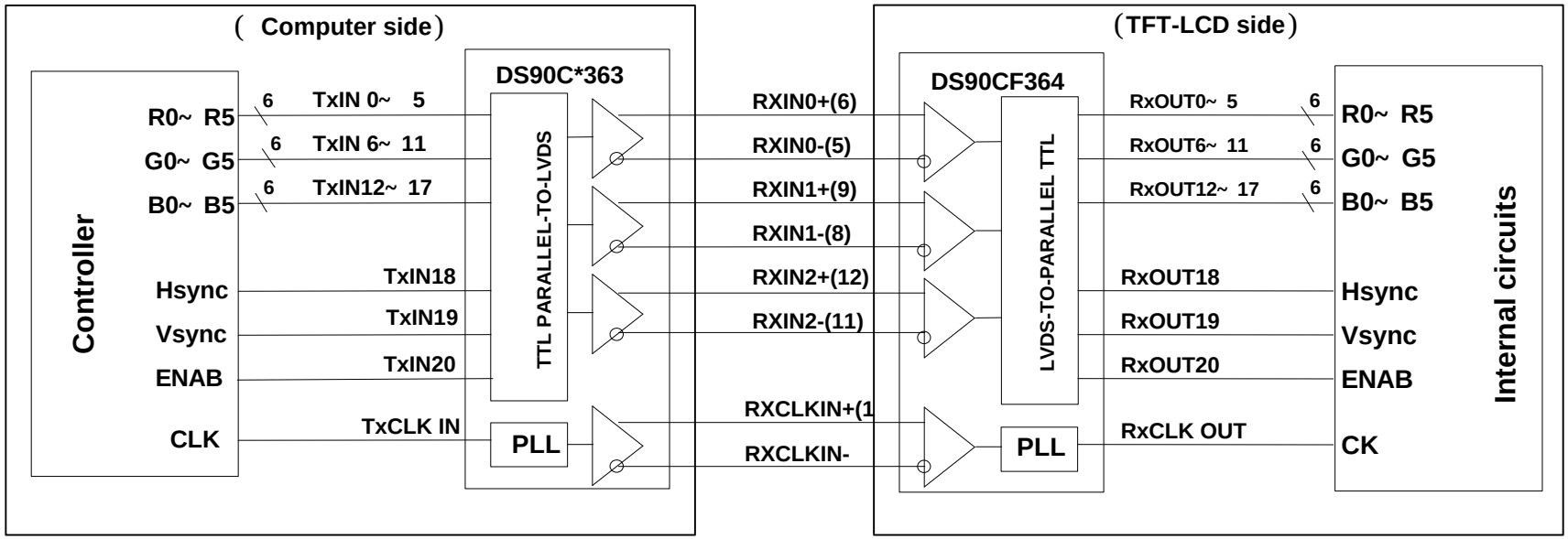
PIN NO	. SYMBOL	FUNCTION
1	VSS	Ground
2	VDD	Power Supply, 3.3 V (typical)
3	VDD	Power Supply, 3.3 V (typical)
4	V EEDID	DDC 3.3V power
5	NC	Reserved for supplier test point
6	Clk EEDID	DDC Clock
7	DATA EEDID	DDC Data
8	Rin0-	- LVDS differential data input (R0-R5, G0) (odd pixels)
9	Rin0+	+ LVDS differential data input (R0-R5, G0) (odd pixels)
10	VSS	Ground
11	Odd_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (odd pixels)
12	Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (odd pixels)
13	VSS	Ground
14	Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
15	Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
16	VSS	Ground
17	ClkIN-	- LVDS differential clock input (odd pixels)
18	ClkIN+	+ LVDS differential clock input (odd pixels)
19	VSS	Ground
20	NC	No connect
21	NC	No connect
22	NC	No connect
23	NC	No connect
24	NC	No connect
25	NC	No connect
26	NC	No connect
27	NC	No connect
28	NC	No connect
29	NC	No connect
30	NC	No connect

? Note 1? Relation between LVDS signals and actual data shows below section (4-2).

? Note 2? The shielding case is connected with signal GND.

4-2 Interface block diagram

Using receiver：DS90CF364(National semiconductor) Corresponding Transmitter：DS90C363,DS90C383(National semiconductor)



4-3. Backlight driving

CN2: BHSR-02VS-1(JST)

Mating connector: SM02B-BHSS-1-TB (JST) or 87210-0200

Pin No.	Symbol	Function
1	V_{HIGH}	Power supply for lamp (High voltage side)
2	V_{LOW}	Power supply for lamp (Low voltage side)

4-4. Inverter driving

Connector pin assignment:

CN3:(Inverter signals and Inverter Power Supply)

Using connector:LVC-D20SYFG(HONDA)

Corresponding connector: LVC-D20LVM-SG (HONDA)

Pin no.	Symbol	Function
1,2,3	INV SRC	Input voltage
4	N.C	No connect
5,8,11,13	GND	Ground
6	5VSUS	System +5V voltage(Inverter no use)
7	5VALW	Dallas IC VCC Voltage
9	SDA	Brightness control data signal(SMBUS DATA)
10	SCL	Brightness control clock signal(SMBUS CLOCK)
12	FPVEE	MPS IC Enable voltage
14	N.C.	No connect
15	N.C.	No connect
16	N.C.	No connect
17	N.C.	No connect
18	N.C.	No connect
19	N.C.	No connect
20	N.C.	No connect

5. Absolute Maximum Ratings

5-1 LCD module

Parameter	Symbol	Condition	Ratings	Unit	Remark
Input voltage	V_I	Ta=25?	- 0.3 ~ Vcc+0.3	V	[Note1]
+3.3V supply voltage	Vcc	Ta=25?	0 ~ + 4	V	
Storage temperature	Tstg	-	- 25 ~ + 60	?	[Note2]
Operating temperature (Ambient)	Topa	-	0 ~ + 50	?	

[Note1] LVDS signals

[Note2] Humidity：95%RH Max. at Ta? 40? .

Maximum wet-bulb temperature at 39? or less at Ta>40? .

No condensation.

5-2. Inverter driving

5-2.1. Backlight lifetime

The backlight system is an edge-lighting type with single CCFT (Cold Cathode Fluorescent Tube).

The lifetime of the lamp are shown in the following table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp life time	LL	10000	-	-	Hour	[Note]

[Note] Lamp life time is defined as the time when m occurs in the continuous operation under the condition of Ta = 25℃ and SDA data=00HEX

m Brightness becomes 50% of the original value under standard condition.

5.2.2 Recommended Operation Condition

Parameter	Symbol	Min.	Typ	Max	Unit
Inverter power supply voltage	Vin	9	-	21	V
Base of Brightness control voltage	VBB	4.85	5.0	5.2	V
Brightness control IC supply voltage	VBC	4.5	5.0	5.5	V
Logic signals	SDA, SCL FPVEE	0		5	V

5.2.3 DC Electrical Conditions

Ta=25℃

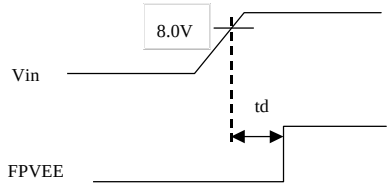
Parameter		Symbol	Condition	Min.	Typ	Max	Unit	Remark
VIN supply current		IVin	VIN=9V,VBB=5V	485	-	585	mA	Note
			VIN=21V,VBB=5V	200	-	300		
Brightness control IC supply current		IVbc	VBC=4.5~5.5V	-	-	200	uA	
SDA SCL	Input voltage low	Vil	VBC=4.5~5.5V	-	-	0.3× VBC	V	
	Input voltage High	Vih	VBC=4.5~5.5V	0.7× VBC	-	-	V	
FPVEE	Input voltage low	Vil	VIN=9~21V	0	-	0.6	V	
	Input voltage High	Vih	VIN=9~21V	3.0	-	5.0	V	

Note: Brightness control from minmum to maximum

5.2.4. Power ON/OFF sequence

9V≦Vin<21V

10ms≦td



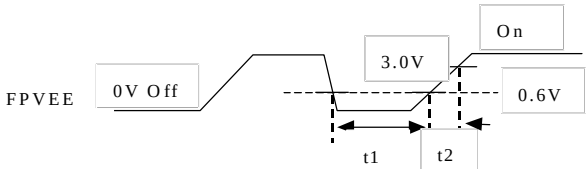
5.2.5 FPVEE ON sequence

Backlight power on/off is possible with FPVEE.

Make sure to have more than 50-millisecond interval between each power-on.

50ms≦t1

t2≦20ms



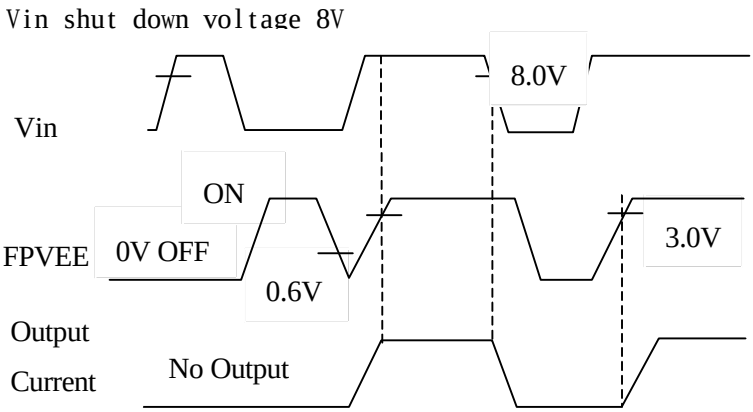
5.2.6 The Condition of Shut Down

Please refer to the figure below for the conditions that will cause the inverter shut down.

If the Vin voltage is higher than 8.0V but there is no enable signal, then the inverter will shut down.

If the Vin voltage is down less than 8.0V, it will cause the inverter shut down.

The enable signal has to be reset to get the inverter started again.



5.2.7. Brightness Control

SDA data	Brightness	Notes
00HEX	Maximum Brightness	Set on power-up
01~FEHEX	?	
FFHEX	Minimum Brightness	

6. Electrical Characteristics

6-1.TFT-LCD panel driving

Ta= 25?

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remark
Vcc	Supply voltage		Vcc	+3.0	+3.3	+3.6	V	[Note2]
	Current dissipation		Icc	-	*360*	*560*	m A	[Note3]
Permissive input ripple voltage			V_{RP}	-	-	100	mV p-p	Vcc=+3.3V
Differential input Threshold voltage		High	V_{TH}	-	-	+100	mV	V_{CM}=+1.2V [Note1]
		Low	V_{TL}	–100	-	-	mV	
Input current (High)			I_{OH}	-	-	± 10	µ A	V_I=2.4V Vcc=3.6V
Input current (Low)			I_{OL}	-	-	± 10	µ A	V_I=0V Vcc=3.6V
Terminal resistor			R_T	-	100	-	0	Differential input
Rush current			I_{RUSH}			1.5	A	Rise time 470uS

[Note1] V_{CM} : Common mode voltage of LVDS driver.

[Note2]

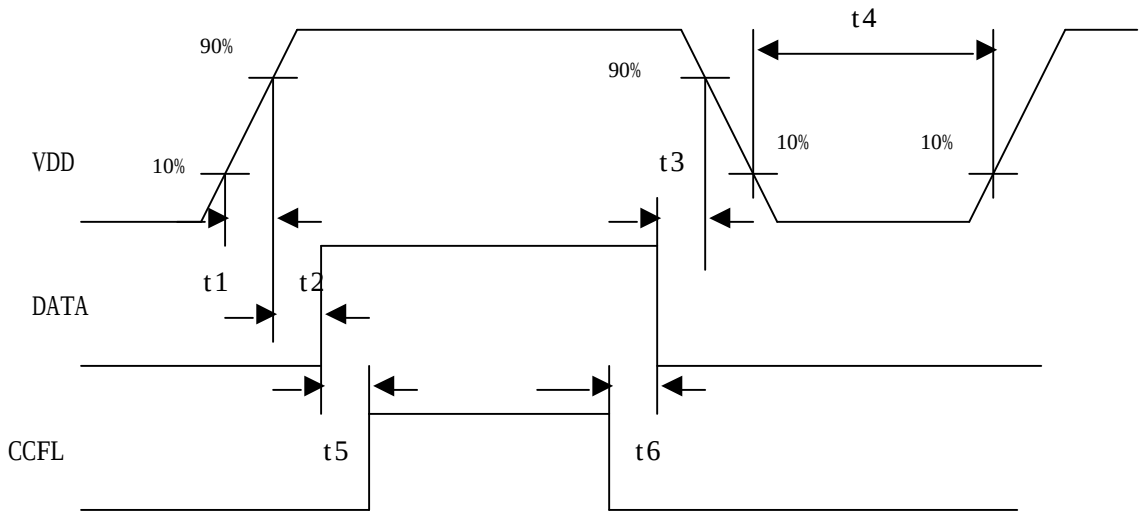
On-off conditions for supply voltage

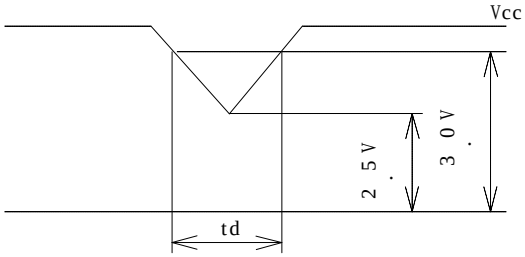
0< t1? 10 ms

0< t2? 50 ms

0< t3? 50 ms

400 ms? t4 ; 200 ms? t5 ; 200 ms? t6





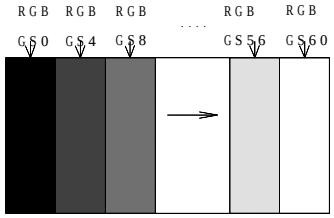
Vcc-dip conditions

1) **2.5 V? Vcc< 3.0 V**
   td? 10 ms
2) **Vcc< 2.5 V**

Vcc-dip conditions should also follow the On-off conditions for supply voltage

[Note3]

1. **The maximum current pattern: one pixel line at gray-level 8 and fully black pixel line aside (one line on-off)**
2. **Typical current pattern: 16-gray-bar pattern, Vcc=+3.3V**

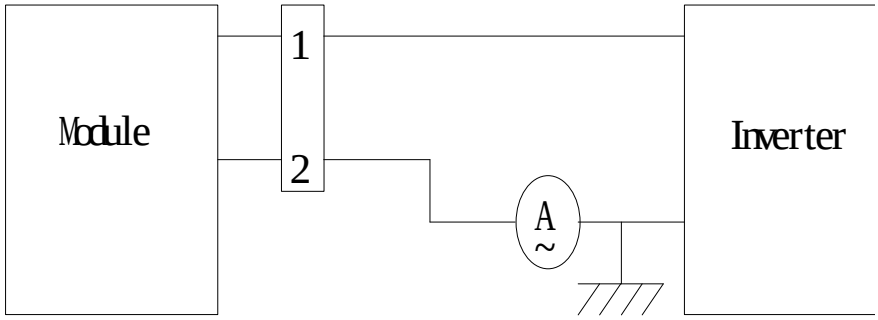


6-2. Backlight driving

The backlight system is an edge-lighting type with single CCFT (Cold Cathode Fluorescent Tube).

The characteristics of the lamp are shown in the following table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp current range	I_L	5.8	6.1	6.4	mArms	[Note1]
Lamp voltage	V_L		675		Vrms	
Lamp power consumption	P_L	-	2.7	-	W	[Note2]
Lamp frequency	F_L	*30*	60	*70*	kHz	[Note3]
Kick-off voltage	Vs	-	-	*1670*	Vrms	Ta=25?
		-	-	*1355*	Vrms	Ta=0? [Note4]
Lamp life time	L_L	*10000*	-	-	hour	[Note5]



* 2 pin is V_{LOW}

[Note1] Lamp current is measured with current meter for high frequency as shown below.

[Note2] Calculated Value for reference (I_L × V_L)

[Note3] Lamp frequency may produce interference with horizontal synchronous frequency, and this may cause beat on the display. Therefore lamp frequency shall be detached as much as possible from the horizontal synchronous frequency and from the harmonics of horizontal synchronous to avoid interference.

[Note4] The voltage above this value should be applied to the lamp for more than 1 second to start-up. Otherwise the lamp may not be turned on.

[Note5] Lamp life time is defined as the time when either ? or ? occurs in the continuous operation under the condition of Ta = 25? and I_L = 6.0 mArms.

? Brightness becomes 50 % of the original value under standard condition.

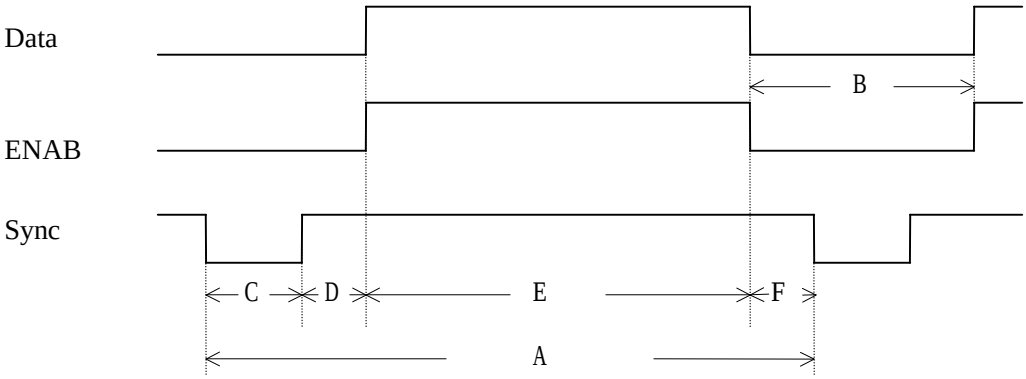
? Kick-off voltage at Ta = 0? exceeds maximum value.

Note) The performance of the backlight, for example life time or brightness, is much influenced by the characteristics of the DC-AC inverter for the lamp. When you design or order the inverter, please make sure that a poor lighting caused by the mismatch of the backlight and the inverter (miss-lighting, flicker, etc.) never occur. When you confirm it, the module should be operated in the same condition as it is installed in your instrument.

7. Timing characteristics of LCD module input signals

7-1. Timing characteristics

(This is specified at digital outputs of LVDS driver.)



(Vertical)

Item(symbol)	Min.	Typ.	Max.	Unit	Remark
Vsync cycle (T_{VA})	-	16.667	-	ms	Negative
	803	806		line	
Blanking period(T_{VB})	35	38	-	line	
Sync pulse width (T_{VC})	4	6	-	line	
Back porch (T_{VD})	0	29		line	
Sync pulse width + Back porch (T_{VC}+T_{VD})	35	35	35	line	
Active display area (T_{VE})	768	768	768	line	
Front porch (T_{VF})	0	3	-	line	

(Horizontal)

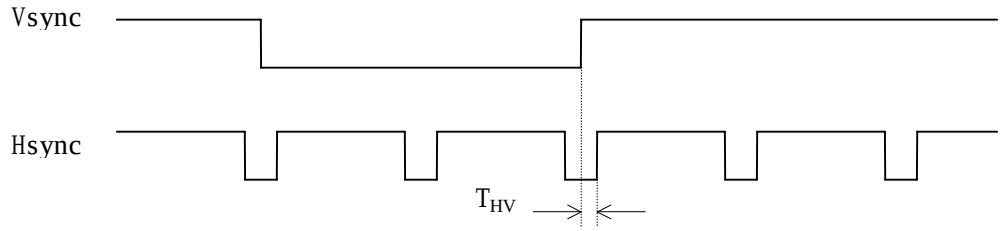
Item(symbol)	Min.	Typ.	Max.	Unit	Remark
Hsync cycle (T_{HA})	19.2	20.677	-	μ s	Negative
	1260	1344	1408	clock	
Blanking period (T_{HB})	236	320	-	clock	
Sync pulse width (T_{HC})	8	136	-	clock	
Back porch (T_{HD})	0	160	312	clock	
Sync pulse width + Back porch (T_{HC} +T_{HD})	1500 - T_{HA}	296	T_{HA} - 1024	clock	
Active display area (T_{HE})	1024	1024	1024	clock	
Front porch (T_{HF})	8	24	-	clock	

(Clock)

Item	Min.	Typ.	Max.	Unit	Remark
Frequency	-	65.0	65.0	MHz	[Note]

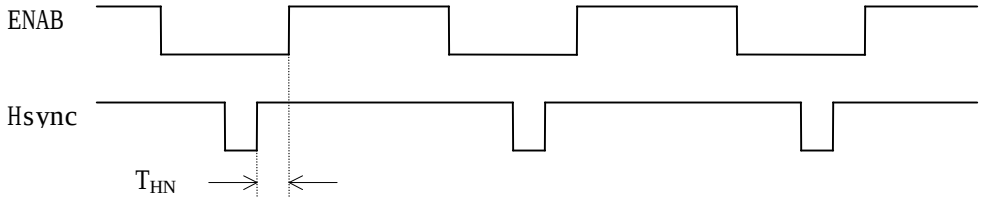
Note) In case of lower frequency, the deterioration of display quality, flicker etc., may be occurred.

(Hsync-Vsync Phase difference)



Item(symbol)	Min.	Typ.	Max.	Unit	Remark
Hsync-Vsync Phase difference (T_{HV})	1	-	T_{HA}- T_{HC}	clock	

(Hsync-ENAB Phase difference)



Item	Min.	Typ.	Max.	Unit	Remark
(T_{HN})	0	-	312	clock	

7-2 Display position

Item	Standards	Beginning	Ending	Unit	Remark
Horizontal	rising edge of ENAB	0	1024	clock	
	rising edge of Hsync	296	1320	clock	[Note1]
Vertical	rising edge of Vsync	35	803	clock	

[Note1] ENAB signal must be fixed to low.

[Note]

(Horizontal display direction)

When ENAB is fixed low, 296 clock are counted from Hsync negative edge and data from after are available. If you need other timing, please use ENAB signal.

(Vertical display direction)

35 lines are counted from Vsync negative edge and data from next line are available.

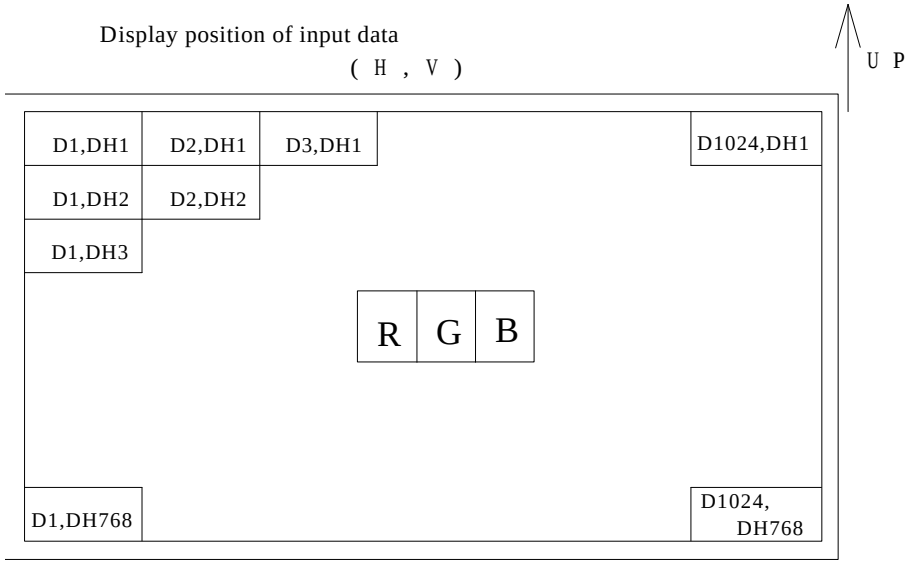
(Note of ENAB signal)

ENAB could not be used for the purpose of the vertical display start timing.

<u>Caution</u>

Image will not be displayed on the right position otherwise.

7-3. Input Data Signals and Display Position on the screen



8. Input Signals, Basic Display Colors and Gray Scale of Each Color

	Colors & Gray scale	Gray Scale	Data signal																	
			R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
Basic Color	Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	-	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	-	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	-	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	-	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	-	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	-	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	✍	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	✍	✍			✍						✍						✍			
	✍	✍			✍						✍						✍			
	Brighter	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	✍	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	✍	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	✍	✍			✍						✍						✍			
	✍	✍			✍						✍						✍			
	Brighter	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	✍	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	✍	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	✍	✍			✍						✍						✍			
	✍	✍			✍						✍						✍			
	Brighter	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	✍	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

0 : Low level voltage, 1 : High level voltage

Each basic color can be displayed in 64 gray scales from 6 bit data signals. According to the combination of total 18 bit data signals, the 262,144-color display can be achieved on the screen.

9.EDID data structure

This is the EDID (Extended Display Identification Data) data format to support displays as defined in the VESA Plug & Display.

Byte (decimal)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	EISA manufacture code=QDS	44	01000100
9	09	EISA manufacture code (Compressed ASCII)	93	10010011
10	0A	Product code: 0005 (P08A)	05	00000101
11	0B	Product code (hex, LSB first)	00	00000000
12	0C	LCD module Serial No (fixed ”0”)	00	00000000
13	0D	LCD module Serial No (fixed ”0”)	00	00000000
14	0E	LCD module Serial No (fixed ”0”)	00	00000000
15	0F	LCD module Serial No (fixed ”0”)	00	00000000
16	10	Week of manufacture	00	00000000
17	11	Year of manufacture – 1990 (ex2000-1990=10), ex: 2003-1990=13=D (hex)	0D	00001101
18	12	EDID structure version # = 1	01	00000001
19	13	EDID revision # = 3	03	00000011
20	14	Video I/P definition = Digital I/P	80	10000000
21	15	Max H image size (cm) = 29cm	1D	00011101
22	16	Max V image size (cm) = 21cm	15	00010101
23	17	Display gamma (2.2× 100) –100= 120	78	01111000
24	18	Feature support (no DMPS, Active off, RGB, timing BLK1)	0A	00001010
25	19	Red/Green Low bit	8C	10001100
26	1A	Blue/White Low bit	E9	11101001
27	1B	Red X (Rx)(written value “0.588”)	96	10010110
28	1C	Red Y (Ry)(written value “0.325”)	53	01010011
29	1D	Green X (Gx)(written value “0.308”)	4E	01001110
30	1E	Green Y (Gy)(written value “0.563”)	90	10010000
31	1F	Blue X (Bx)(written value “0.148”)	25	00100101
32	20	Blue Y (By)(written value “0.116”)	1D	00011101
33	21	White X (Wx)(written value “0.315”)	50	01010000
34	22	White Y (Wy)(written value “0.330”)	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Established timings 3 (Manufacture’s reserved timing)	00	00000000
38	26	Standard timing ID1	01	00000001
39	27	Standard timing ID1	01	00000001
40	28	Standard timing ID2	01	00000001
41	29	Standard timing ID2	01	00000001
42	2A	Standard timing ID3	01	00000001
43	2B	Standard timing ID3	01	00000001
44	2C	Standard timing ID4	01	00000001
45	2D	Standard timing ID4	01	00000001
46	2E	Standard timing ID5	01	00000001

47	2F	Standard timing ID5	01	00000001
48	30	Standard timing ID6	01	00000001
49	31	Standard timing ID6	01	00000001
50	32	Standard timing ID7	01	00000001
51	33	Standard timing ID7	01	00000001
52	34	Standard timing ID8	01	00000001
53	35	Standard timing ID8	01	00000001
54	36	Detailed timing descriptor#1	64	01100100
55	37	#1 fck	19	00011001
56	38	#1 Horizontal active 1024=400h “00”	00	00000000
57	39	#1 Horizontal blanking 320=140h “40”	40	01000000
58	3A	#1 Horizontal active/Horizontal blanking “41h”	41	01000001
59	3B	#1 Vertical active 768=300h “00”	00	00000000
60	3C	#1 Vertical blanking 38=026h “26”	26	00100110
61	3D	#1 Vertical active/Vertical blanking “30h”	30	00110000
62	3E	#1 Horizontal sync, offset 24=018h “18”	18	00011000
63	3F	#1 Horizontal sync, width 136=088h “88”	88	10001000
64	40	#1 Vertical sync, offset/Vertical sync, width	36	00110110
65	41	#1 Horizontal sync offset/width/Vertical sync offset/width	00	00000000
66	42	#1 Horizontal image size 290mm=122h “22”	1D	00011101
67	43	#1 Vertical image size 220mm=0DCh “DC”	D6	11010110
68	44	#1 Horizontal image size / Vertical image size	10	00010000
69	45	Horizontal border	00	00000000
70	46	Vertical border	00	00000000
71	47	Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Flag	00	00000000
73	49	Flag	00	00000000
74	4A	Reserved	00	00000000
75	4B	Dummy Descriptor	0F	00001111
76	4C	Flag	00	00000000
77	4D	Value = $HSPW_{min}$ /2 (pixel clks) =8/2 =4	04	00000100
78	4E	Value = $HSPW_{max}$ /2 (pixel clks) =384/2 = 192	C0	11000000
79	4F	Value = $Thbp_{min}$ /2 (pixel clks) =92/2 =46	2E	00101110
80	50	Value = $Thbp_{max}$ /2 (pixel clks) =384/2 =192	C0	11000000
81	51	Value = $VSPW_{min}$ /2 (line pulses)= 4/2 =2	02	00000010
82	52	Value = $VSPW_{max}$ /2 (line pulses)= 35/2 =17	11	00010001
83	53	Value = $Tvbp_{min}$ /2 (line pulses)= 35/2 =17	11	00010001
84	54	Value = $Tvbp_{max}$ /2 (line pulses)= 35/2 =17	11	00010001
85	55	Thp_{min} = value*2 + $HA_{pixel\ clks}$ (pixel clks),value= 118	76	01110110
86	56	Thp_{max}= value*2 + $HA_{pixel\ clk}$ (pixelclks),value =192	C0	11000000
87	57	Tvp_{min} = value*2 + VA_{lines} (line pulses),value =18	12	00010010
88	58	Tvp_{max} = value*2 + VA_{lines} (line pulses),value =99	63	01100011
89	59	Module “A” Revision = Example: 00, 01, 02, 03, etc.	00	00000000
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Reserved	00	00000000
93	5D	Dummy Descriptor	FE	11111110
94	5E	Flag	00	00000000
95	5F	Dell PN Character C	43	01000011
96	60	Dell PN Character 4	34	00110100
97	61	Dell PN Character 0	30	00110000
98	62	Dell PN Character 1	31	00110001
99	63	Dell PN Character 1	31	00110001
100	64	LCD Supplier EEDID Reversion # 02	02	00000010

101	65	Manufacturer PN	00	00000000
102	66	Manufacturer PN	00	00000000
103	67	Manufacturer PN	00	00000000
104	68	Manufacturer PN	00	00000000
105	69	Manufacturer PN	00	00000000
106	6A	Manufacturer PN	00	00000000
107	6B	Manufacturer PN	00	00000000
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag	FE	11111110
112	70	Flag	00	00000000
113	71	SMBUS Value = 20 nts	D8	11011000
114	72	SMBUS Value = 30 nts	C8	11001000
115	73	SMBUS Value = 40 nts	B8	10111000
116	74	SMBUS Value = 50 nts	A8	10101000
117	75	SMBUS Value = 70 nts	90	10010000
118	76	SMBUS Value = 100 nts	70	01110000
119	77	SMBUS Value = 135 nts	50	01010000
120	78	SMBUS Value = Max nts	00	00000000
121	79	Number of LVDS receiver chips	01	00000001
122	7A	Panel type-Standard	00	00000000
123	7B	(If<13 char, then terminate with ASCII code 0Ah, set remaining char=20h)	0A	00001010
124	7C	(If<13 char, then terminate with ASCII code 0Ah, set remaining char=20h)	20	00100000
125	7D	(If<13 char, then terminate with ASCII code 0Ah, set remaining char=20h)	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	2B	00101011

10. Optical Characteristics

Ta=25? , Vcc=+3.3V

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	? 21,? 22	CR>10	40	-	-	Deg.	[Note1,4]
	Vertical	? 11		10	-	-	Deg.	
		? 12		30	-	-	Deg.	
Contrast ratio		C R n	? =0°	300	-	-		[Note2,4]
Response Time	Rise	t r	? =0°	-	12.5	-	ms	[Note3,4]
	Decay	t d		-	22.5	-	ms	
Chromaticity of White		Wx		0.295	0.315	0.335		[Note4]
		Wy		0.310	0.330	0.350		
Chromaticity of Red		Rx		0.558	0.588	0.618		
		Ry		0.295	0.325	0.355		
Chromaticity of Green		Gx		0.278	0.308	0.338		
		Gy		0.533	0.563	0.593		
Chromaticity of Blue		Bx		0.118	0.148	0.178		
		By		0.086	0.116	0.146		
Luminance of white ? Note4?		Y L 2	Center	150	200	-	Cd/m^2	I_L = 6.0mArms F_L=60kHz
Color Gamut		?			50%			NTSC
White Uniformity		d W	13 Points	-	-	1.53		[Note5]
White Uniformity		d W	5 Points	-	-	1.25		[Note5]

? The measurement shall be executed 30 minutes after lighting at rating. (typical condition : IL = 6.0 mArms)

The optical characteristics shall be measured in a dark room or equivalent state with the method shown in Fig.3.

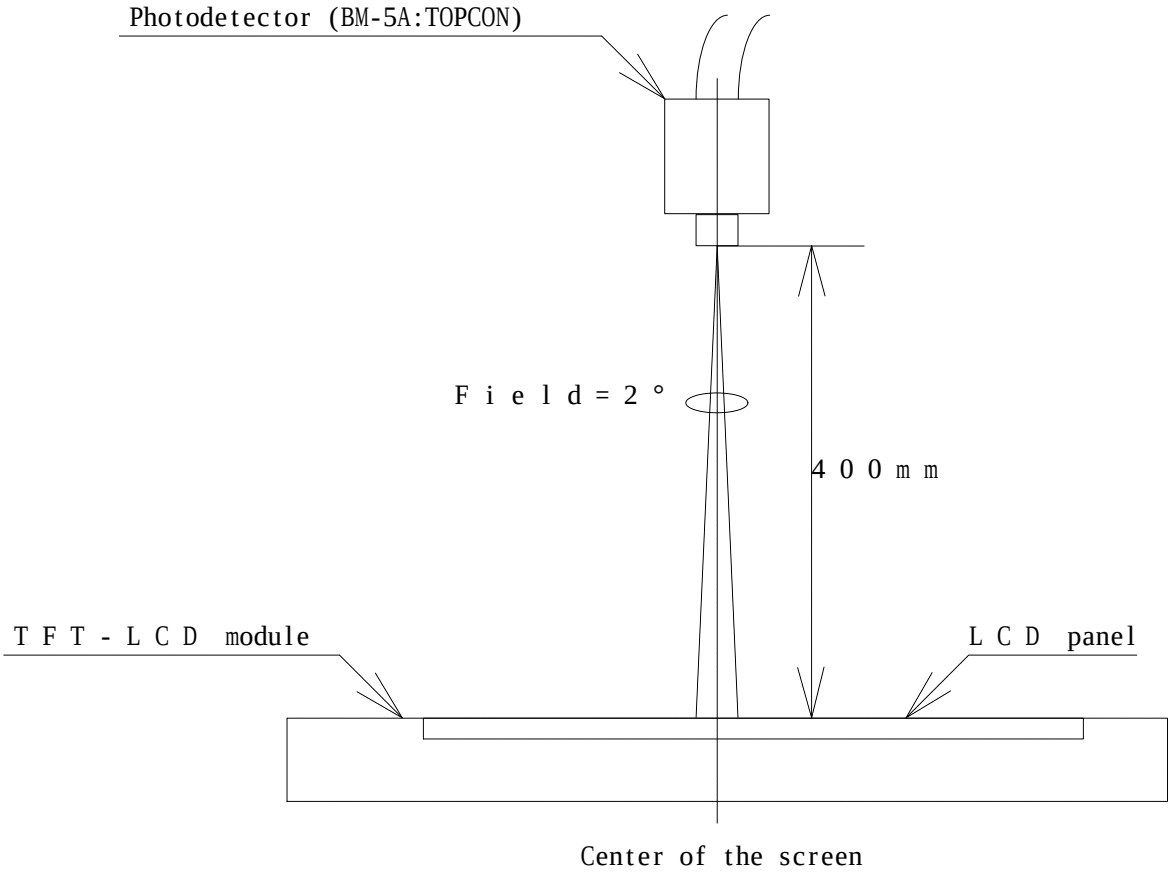
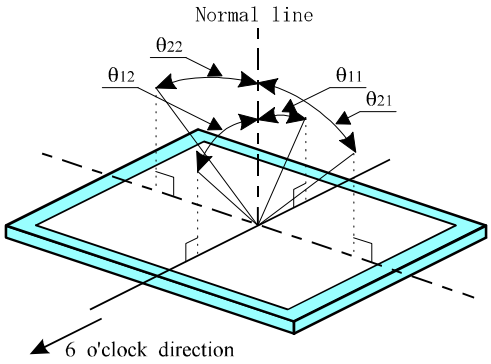


Fig.3 Optical characteristics measurement method

[Note1] Definitions of viewing angle range:



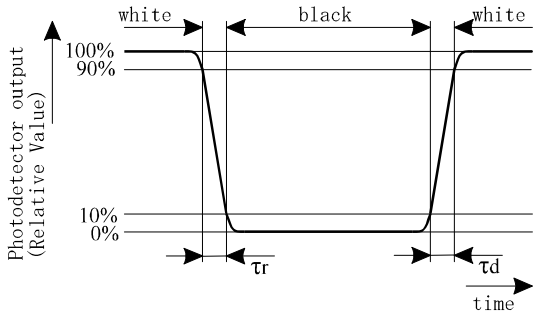
[Note2] Definition of contrast ratio:

The contrast ratio is defined as the following.

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

[Note3] Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".

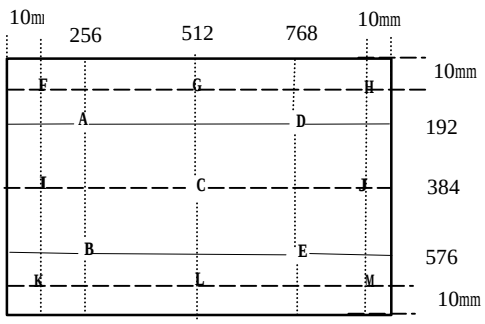


[Note4] This shall be measured at center of the screen.

[Note5] Definition of white uniformity:

$$dw = \frac{\text{Maximun Luminance of 5/13 points}}{\text{Minimum Luminance of 5/13 points}}$$

(5 Points A,B,C,D,E 13 Points A,B,C,D,E,F,G,H,I,J,K,L,M)



11. Display Quality

The display quality of the color TFT-LCD module shall be in compliance with the Incoming Inspection Standard.

12. Handling Precautions

a) Be sure to turn off the power supply when inserting or disconnecting the cable.

b) Be sure to design the cabinet so that the module can be installed without any extra stress such as warp or twist.

c) Since the front polarizer is easily damaged, pay attention not to scratch it.

d) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

e) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

f) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.

g) Since CMOS LSI is used in this module, take care of static electricity and injure the human earth when handling.

h) Observe all other precautionary requirements in handling components.

i) This module has its circuitry PCBs on the rear side and should be handled carefully in order not to be stressed.

j) Laminated film is attached to the module surface to prevent it from being scratched. Peel the film off slowly just before the use with strict attention to electrostatic charges. Ionized air shall be blown over during the action. Blow off the 'dust' on the polarizer by using an ionized nitrogen gun, etc…

k) Black PET sheet covers some electric components and handle with special care to avoid mechanical stress and shock on this PET surface.

l) Mounting screw hole can stand torque 1.3~1.5 Kgf-cm.

13. Reliability test items

No.	Test item	Conditions
1	High temperature storage test	Ta = 60? 240h
2	Low temperature storage test	Ta = -25? 240h
3	High temperature & high humidity operation test	Ta = 40? ; 90 %RH 240h ; (As remark 3) (No condensation)
4	High temperature operation test	Ta = 50? 240h (The panel temp. must be less than 60?)
5	Low temperature operation test	Ta = 0? 240h
6	Temperature cycle—Non Operating	-25 ? to +65 ? , Ramp ≦ 24 ? /min, Duration at Temp.=60min, Test cycles=50
7	Vibration test (non- operating)	1.5G 30min/each axis 1.6G random Sweep time : 11 minutes Test period : 3 hours (1 hour for each direction of X,Y,Z)
8	Shock test (non- operating)	Max. gravity : 220G Pulse width : 11 ms, sine wave Direction : ± X,± Y,± Z once for each direction.

Remark:

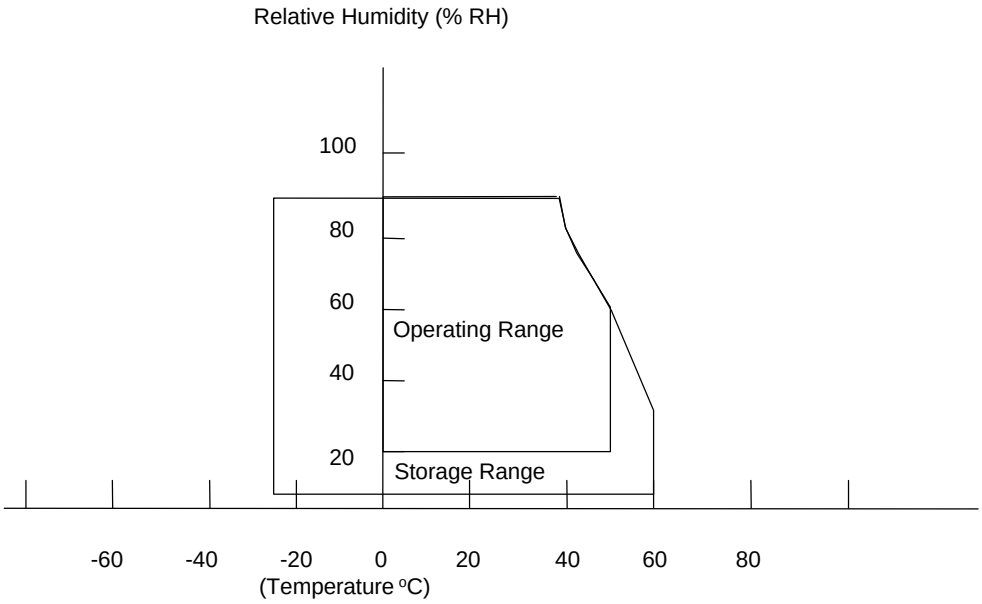
(1) A failure is defined as the appearance of pixel failured on any color layer or the appearance of horizontal or vertical lines, bars etc.

(2) Low temperature storage " Panel must return to operating temperature range prior to activation."

(3) Hi temperature / Humidity test

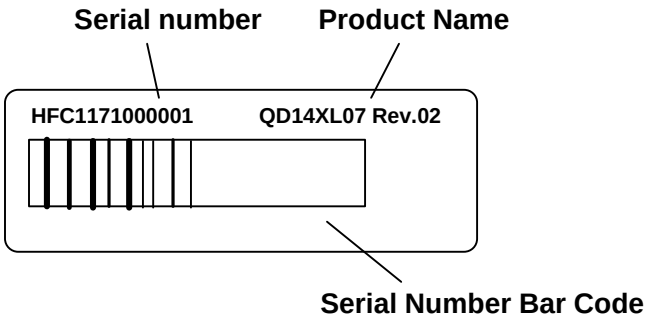
Max. wet-bulb temperature is less than 39°C ; At glass temperature high than 40 °C.

Temperature and relative humidity range is shown in the figure below.

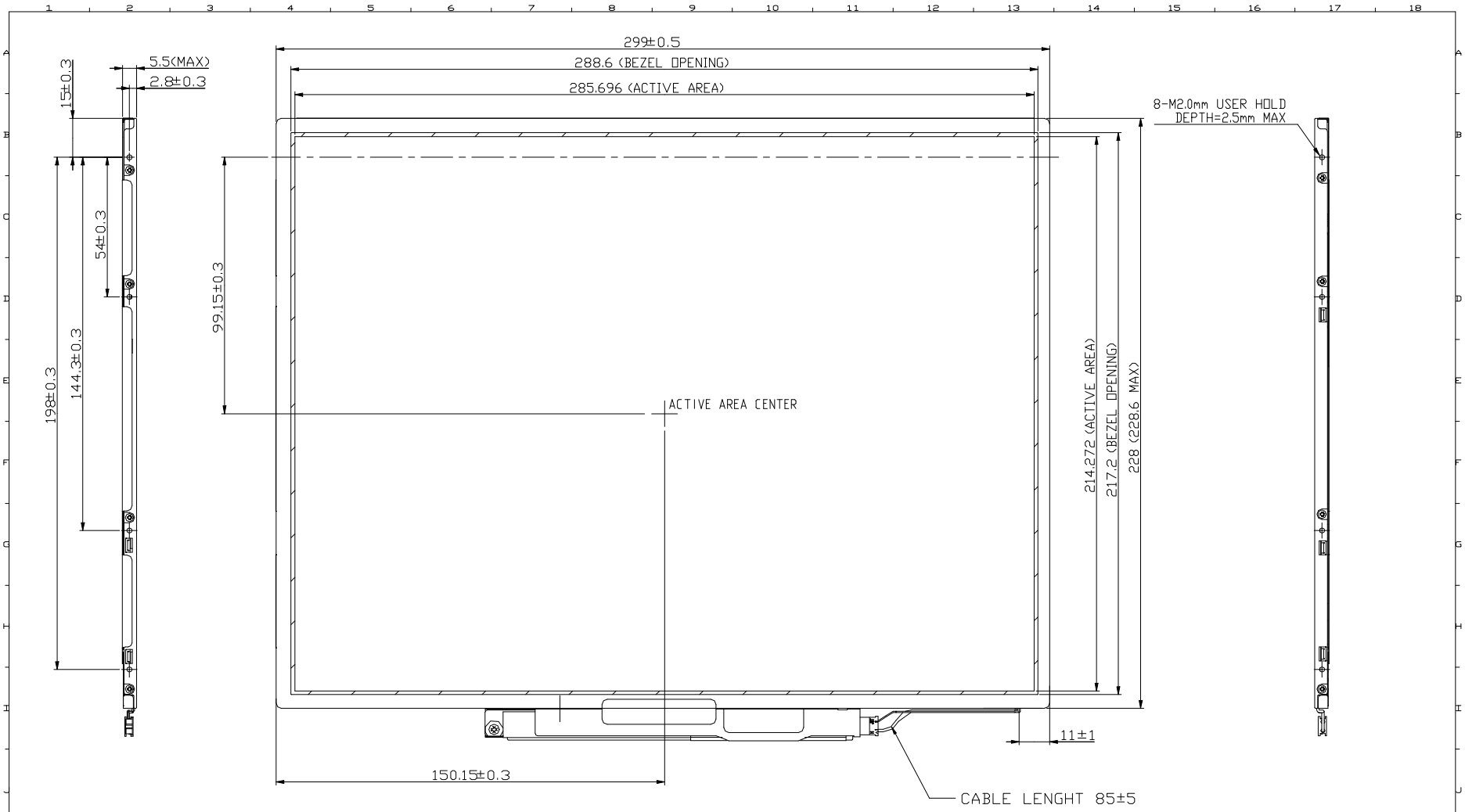


14. Others

1) **Lot No. Label:**



2) **Adjusting volume has been set optimally before shipment, so do not change any adjusted value. If adjusted value is changed, the specification may not be satisfied.**
3) **Disassembling the module can cause permanent damage and should be strictly avoided.**
4) **Please be careful since image retention may occur when a fixed pattern is displayed for a long time.**
5) **If any problem occurs in relation to the description of this specification, it shall be resolved through discussion with spirit of cooperation.**



NOTES:
1. UNSPECIFIED TOLERANCE TO BE ±0.5
2. WARP AND FLATING FOR PCB AND CHASSIS ARE EXCLUDED FROM THICKNESS AND DIMENSION OF THE UNIT.

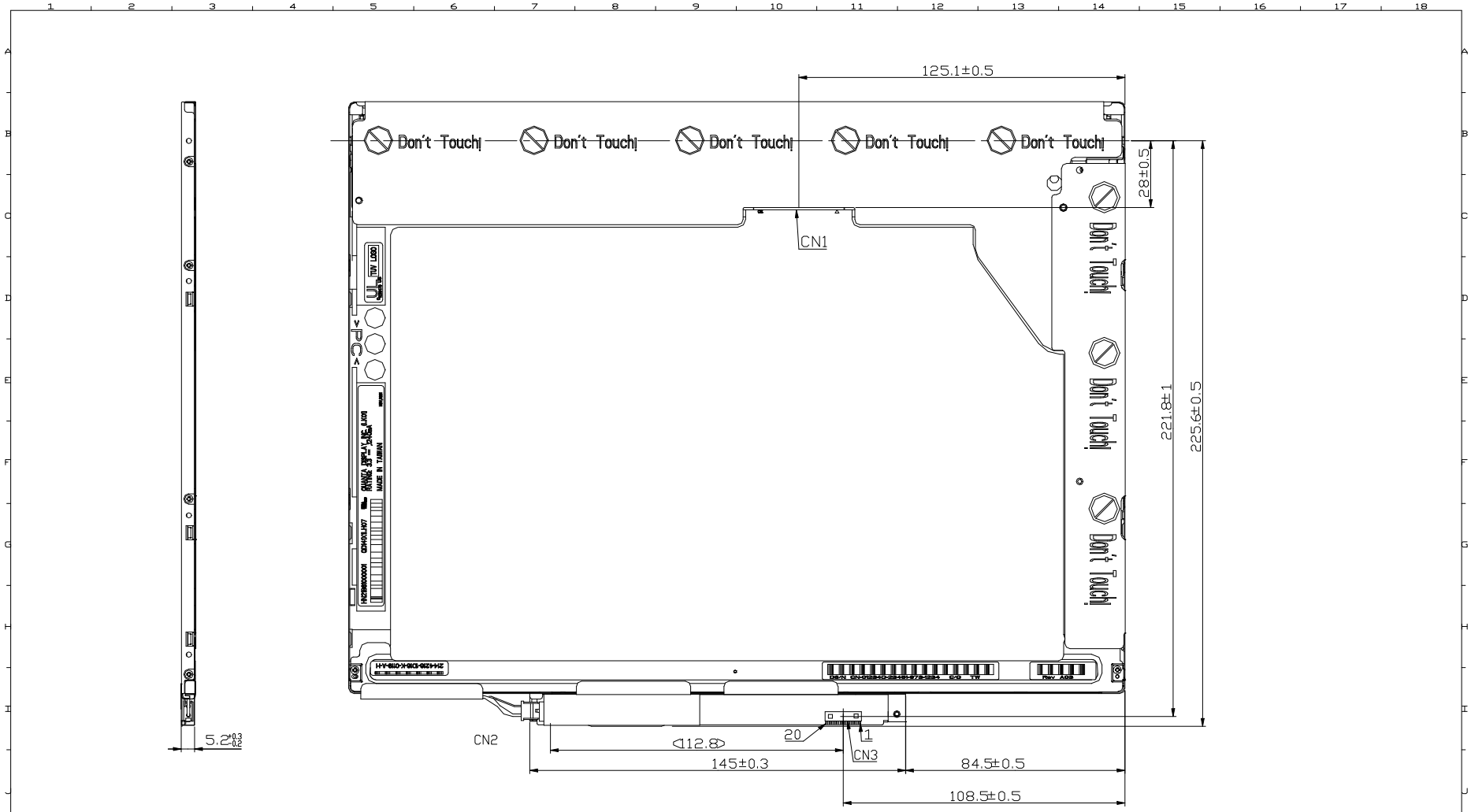
DEC / DIV	A	B	C	D	ANGLE
0~5	±0.02	±0.05	±0.1		0°~30° ±0.1°
5~10	±0.05	±0.1	±0.15		31°~60° ±0.3°
10~50	±0.1	±0.15	±0.2		61°~90° ±0.5°
50~100	±0.15	±0.2	±0.25		
100~	±0.15%	±0.2%	±0.25%		

NO	DATE	REVISE ITEMS	DWNER
<1>	2002.02.20	INCREASE THE LENGTH	PM

Quanta Display Inc.
CONFIDENTIAL

UNIT	mm	SHEET	1 OF 2
SCALE	1:1	SIZE	A2
DATE	2002,02,18		
DESIGN	DSN CK	DSN CK	ENG APPD
KEVIN			LIN

ORIGINAL MODEL	QD141X1LH07
MATERIAL FINISH	
PART NAME	OUTLINE
PART NUMBER	
DRAWING NUMBER	



CN1:INTERFACE CONNECTOR
IF-XB30S-HF10 (JAE)
CN2:CCFT CONNECTOR
BHSR-02VS-1 (JST)
CN3:INVERTER CONNECTOR
LVC-D20SFYG (HONDA)

DEC DIV	A	B	C	D	ANGLE
0-5	±0.02	±0.05	±0.1		0°-30° ±0.1°
5-10	±0.05	±0.1	±0.15		31°-60° ±0.3°
10-50	±0.1	±0.15	±0.2		61°-90° ±0.5°
50-100	±0.15	±0.2	±0.25		
100-	±0.15%	±0.2%	±0.25%		

NO	DATE	REVISE ITEMS	OWNER

Quanta Display Inc.
CONFIDENTIAL

UNIT	mm	SHEET	2 OF 2
SCALE	1:1	SIZE	A2
DATE	2001.12.18		
DESIGN	DSN CK	DSN CK	ENG APPR
KEVIN			

ORIGINAL MODEL	QD141X1LH07
MATERIAL FINISH	
PART NAME	OUTLINE
PART NUMBER	
DRAWING NUMBER	P08AA01B