QUANTUM DIGITAL™
Technology

Quantum Digital Compact Flash

General Description and Key Features

Quantum Digital's flash storage products meet the latest industry compliance and regulatory standards including UL, FCC, and RoHS. Each device incorporates a proprietary cutting edge flash memory controller (hyperstone f3 series) that provides the greatest flexibility to customer-specific applications while supporting key flash management features resulting in the industry's highest reliability and endurance. Key features include: Built-in ECC engine detects up to 5-byte and corrects up to 4-byte errors Sophisticated block management and wear leveling algorithms guarantees 2,000,000 write/erase cycles Power-down data protection ensures data integrity and errors in case of power loss Lifecycle management feature allows users to monitor the device's block management Quantum Digital's CF Card is the product of choice in applications requiring high reliability and high tolerance to shock, vibration, humidity, altitude, ESD, and temperature. The rugged industrial design combined with industrial temperature (40°C to 85°C) testing and adherence to rigid JEDEC JESD22 standards ensures flawless execution in the harshest environments.

In addition to custom hardware and firmware designs, Quantum Digital also offers value-added services including:

Solid-State Memory Card (No Moving Parts)
Capacity: 128MB to 16GB
CFA 4.1 and ATA-7 Compatible
ATA Transfer modes:
  UDMA 0-6, MWDMA 0-4
UDMA 0-6, MWDMA 0-2
Supports True IDE and PC Card Memory and I/O Modes
Form Factors:
  Compact Flash Type I
  Compact Flash Type II
  Compact Flash Adapter
Advanced Wear-Leveling for Greater Flash Endurance
Card Information Structure (CIS) Programmed into Internal Memory
PC Card and Socket Services Release 2.1 or later compatible
5V or 3.3V Power Supply
Commercial and Industrial Operating Temperature Ranges Available
Full Data-Path Protection with built-in ECC Engine
10 Year Data Retention
RoHS-6 Compliant

- Custom labeling and packaging
- Custom software imaging and ID strings
- Full BOM control and product change notification
- Total supply-chain management to ensure continuity of supply
- In-field application engineering to help customers through product designing

Ordering Information: Compact Flash Card

Ordering Information:

Part Number	CF Foam FACTOR	Capacity	
QDCF-128MUH1(I)	Type I	128	Mbytes
QDCF-256MUH1(I)	Type I	256	Mbytes
QDCF-512MUH1(I)	Type I	512	Mbytes
QDCF- 1 GUH1(I)	Type I	1	Gbytes
QDCF-2 GUH1(I)	Type I	2	Gbytes
QDCF-4 GUH1(I)	Type I	4	Gbytes
QDCF-8 GUH1(I)	Type I	8	Gbytes
QDCF-16GUH1(I)	Type II	16	Gbytes

QDCF= QDT standard CF Card part number prefix.

(M/G) = proceeding capacity (xxx) is in Megabytes (M) or Gigabytes (G).

H1 = QDT H1 controller.

U = RoHS-6 compliant lead-free.

Part numbers without (I) = Commercial temperature range (0ºC to 70ºC).

(I) = Industrial temperature range (-40ºC to +85 ºC).

F = media set to fixed storage for non-removable IDE applications. Use with operating systems, such as Windows XP, that require storage media to be identified as a fixed drive before it can be used as a bootable drive.

This document is for information use only and is subject to change without prior notice.

Revision History

Rev.	*Description*	*Update*
1.0	*Preliminary release and general changes*	*2006/07/31*
2.0	*- Rugged CF Card added* *- New part number Decoder and part number list*	*2008/11/5*
2.1	*- Optional Conformal Coating Specification added*	*2008/11/27*
2.2	*- Specification of PIO mode and UDMA mode updated* *- 2.2 System Power Requirements updated*	*2008/12/09*
2.3	*General revised*	*2009/10/01*
2.4	*- Typo corrected* *- Table format changed* *- Table 3: System Performances updated* *- Table 4: System Reliability updated* *- Table 6: Flash memory chips part no. updated*	*2010/7/21*
3.0	*- Table 6: Device Parameter updated* *- New part number Decoder and part number list*	*2011/2/23*
4.0	*- Capacity 16MB CF Card added* *- Capacity 32GB CF Card added* *- General revised*	*2011/9/09*

CONTENTS

1. *Introduction*

The Industrial Compact Flash (CF) Card is designed to follow ATAPI-6 (ATA-100) standard. The main used Flash memories are Samsung SLC-NAND Type Flash memory chips from 32MB up to 8GB, and Micron SLC-NAND Type Flash memory chips for 16GB only. The operating temperature grade is optional for commercial level 0°C ~ 70°C and wide temperature level -40°C ~ +85°C. The Industrial Compact Flash (CF) Cards are designed electrically complies with the conventional IDE hard Card and support True IDE Mode. The data transfer modes supports PIO mode 0, 1, 2, 3, 4 or MWDMA- 0, 1, 2 or UDMA- 0, 1, 2, 3, 4. The fastest reading speed is up to 40 MB/sec (Max. / 32GB) and writing speed is up to 27.8 MB/sec (Max. / 32GB). In order to sustain various harsh and tough operating environments, we especially deliver Compact Flash frame kit in rugged metal as well as provide the optional treatment of conformal coating upon customers' request.

The Industrial CF products provide a high level interface to the host computer. This interface allows a host computer to issue commands to the Compact Flash (CF) Card to read or write blocks of memory. Each sector is protected by a powerful 4 bits Error Correcting Code (ECC). The Industrial Compact Flash (CF) Card's intelligent controller manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management and clock control.

Figure 1 shows a block diagram of the used high tech Industrial Compact Flash (CF) Card controller.

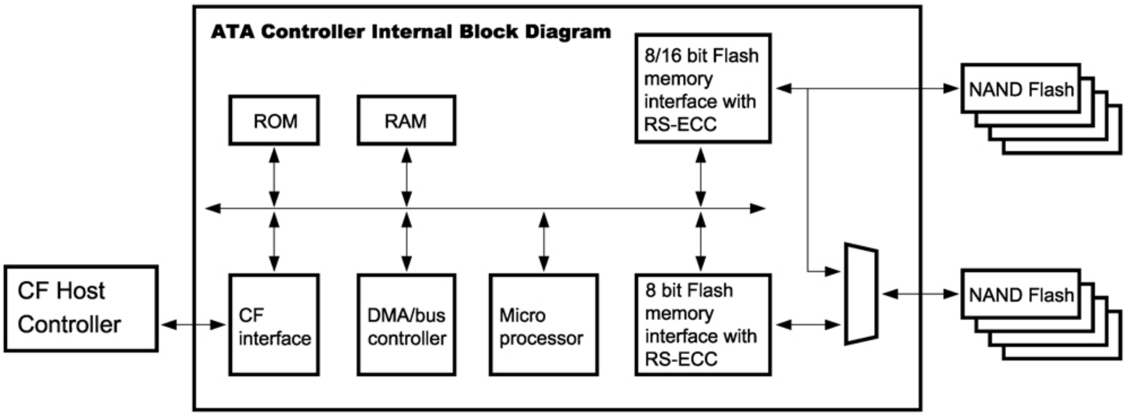


Figure 1: Compact Flash Card Controller Block Diagram

1.1. *Scope*

This document describes the features, specifications and installation guide of the Industrial CF Cards. In the appendix, there provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

1.2. *System Features*

- Optional Rugged metal Compact Flash casing to sustain the harshest environments
- Non-volatile memory and no moving parts
- SLC-NAND type flash technology
- Card capacity from 16MB to 32GB
- ATA interface and support PC Card Memory mode, PC Card I/O mode and True IDE mode
- Data transfer supports PIO-4 and UDMA-4 (Default setting)
- Performance up to 40 MB/sec
- Automatic 4 bits error correction (ECC) and retry capabilities
- +5 V ±10％ or +3.3 V ±5％ operation
- MTBF 3,000,000 hours.
- Shock : 1,500G , compliance to MIL-STD-810F
- Vibration : 15G, compliance to MIL-STD-810F
- Support various rugged and harsh environments
- Very high performance, very low power consumption
- Low weight, Noiseless
- Conformal coating upon special request

1.3. *CFA 3.0 Specification*

Industrial CF Card is fully compatible with the CFA 3.0 specification.

1.4. *ATA/ATAPI-6 Standard*

Industrial CF Card is compliant to ATA/ATAPI-6 and below version.

1.5. *Technology Independence - Static Wear Leveling*

In order to gain the best management for flash memory, the Industrial CF Card supports Static Wear Leveling technology to manage the Flash system. The life of flash memory is limited; the management is to increase the life of the flash product.

A static wear-leveling algorithm evenly distributes data over an entire Flash cell array and searches for the least used physical blocks. The identified low cycled sectors are used to write the data to those locations. If blocks are empty, the write occurs normally. If blocks contain static data, it moves that data to a more heavily used location before it moves the newly written data. The static wear leveling maximizes effective endurance Flash array compared to no wear leveling or dynamic wear leveling.

1.6. *Conformal coating*

Conformal coating is a protective, dielectric coating designed to conform to the surface of an assembled printed circuit board. Commonly used conformal coatings include silicone, acrylic, urethane and epoxy. We apply only silicone on our storages products upon requested especially by customers. The type of silicone coating features good thermal shock resistance due to flexibility. It is also easy to apply and repair.

Conformal coating offers protection of circuitry from moisture, fungus, dust and corrosion caused by extreme environments. It also prevents damage from those Flash storages handling during construction, installation and use, and reduces mechanical stress on components and protects from thermal shock. The greatest advantage of conformal coating is to allow greater component density due to increased dielectric strength between conductors.

We use MIL-I-46058C silicon conformal coating.

2. *Product Specifications*

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. *System Environmental Specifications*

Table 1: Environmental Specification

Industrial Compact Flash Card		Commercial Grade	Industrial Grade
Temperature	**Operating:**	0ºC ~ +70ºC	-40ºC ~ +85ºC
	Non-operating:	-20ºC ~ +80ºC	-50ºC ~ +95ºC
Humidity	**Operating & Non-operating:**	10% ~ 95% non-condensing	
Vibration	**Operating & Non-operating:**	15G peak-to-peak maximum	
Shock	**Operating & Non-operating:**	1,500G maximum	
Altitude	**Operating & Non-operating:**	70,000 feet	

2.2. *System Power Requirements*

Table 2: Power Requirement

Industrial Compact Flash Card	Commercial Grade	Industrial Grade
DC Input Voltage (VCC)	5V±10% or 3.3V±5%	
Reading mode	1 channel 78ma(Max.) / 2 channel 124ma(Max) UDMA-4 mode	
Writing mode	1 channel 67ma(Max.) / 2 channel 121ma(Max) UDMA-4 mode	
Idle mode	1 channel 1.2ma(Max.) / 2 channel 1.8ma(Max) UDMA-4 mode	

2.3. *System Performance*

Table 3: System Performances

Data Transfer Mode supporting			- PIO mode : 0, 1, 2, 3, **4 (PIO – 4 defaulted)** - DMA SW Mode: Not supported - DMA MW Mode:0,1 and 2 - UDMA Mode: 0,1,2,3, **4 (UDMA-4 defaulted)**											
Data Transfer Rate To/From Host			16.6Mybtes/sec burst under PIO Mode 4 as defaulted 66.6Mbytes/sec burst under UDMA-4 Mode as defaulted											
Average Access Time			0.2 ms(estimated)											
Maximum Performance	**Capacity**		16MB	32MB	64MB	128MB	256MB	512MB	1GB	2GB	4GB	8GB	16GB	32GB
	Sequential Read (MB/s)	**PIO- 4**	4.0	4.0	4.0	4.0	4.0	4.0	4.7	4.7	4.7	4.6	4.7	4.7
		UDMA -4	18.5	18.5	18.5	18.5	18.5	21.1	39.6	39.6	39.6	39.6	39.0	40.0
	Sequential Write(MB/s)	**PIO- 4**	4.2	4.2	4.2	4.2	4.2	4.0	4.6	4.6	4. 6	4.0	4.5	4.5
		UDMA -4	18.6	18.6	18.6	18.6	18.6	19.7	19.9	19.9	19.9	19.4	18.7	27.8
The number of Channel			Single	Single	Single	Single	Single	Single	Dual	Dual	Dual	Dual	Dual	Dual

Note:

(1). All values quoted are typically at 25℃ and nominal supply voltage.

(2). Testing of the Industrial Compact Flash (CF) Card maximum performance was performed under the following platform:

- *Computer with AMD 3.0GHz processor*
- *Windows XP Professional operating system*

(3). Above performance data are for reference only for the performance would be different for various factors such like flash memory chips, system configuration and software for performance testing,…etc.

2.4. *System Reliability*

Table 4: System Reliability

MTBF	3,000,000 hours
Wear-leveling Algorithms	Static wear-leveling algorithms
ECC Technology	4 bits per 512 bytes block
Endurance	Greater than 2,000,000 cycles Logically contributed by static wear-leveling and advanced bad sector management
Data Retention	10 years

2.5. *Physical Specifications*

Refer to Table 5 and see Figure 2 for Industrial CF physical specifications and dimensions.

Table 5: Physical Specifications

Industrial Compact Flash Card (Type I Compact Flash)	
Length:	36.40±0.15mm(1.433±0.006 in)
Width:	42.80±0.10mm(1.685±0.004 in)
Thickness:	3.3mm±0.10mm(.130±0.004 in) (Excluding Lip)
Weight:	12.0g(0.42oz) typical, 14.2 g (.0.5 oz) maximum

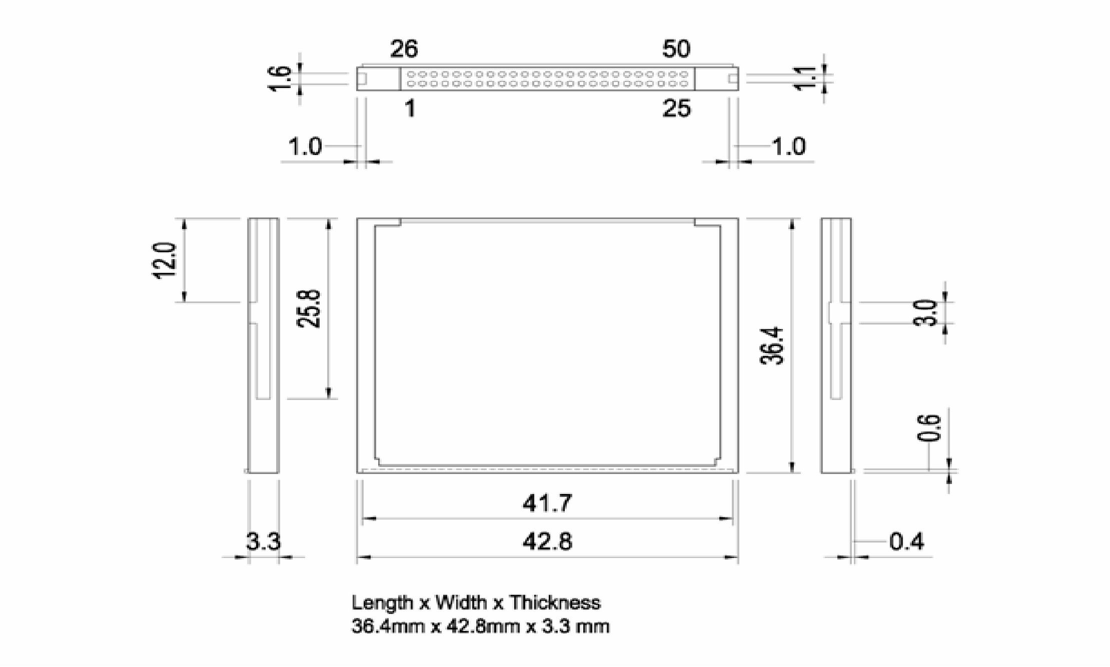


Figure 2: Compact Flash Card Dimension

2.6. *Capacity Specifications*

The table 6 shows the specific capacity for the various models and the default number of heads, sectors/track and cylinders.

Table 6: Device Parameter

Unformatted Capacity	Default Cylinder	Default Head	Default Sector	LBA Total Sectors
16MB	248	4	32	31,744
32MB	500	8	16	64,000
64MB	500	8	32	112,000
128MB	497	16	32	254,464
256MB	984	16	32	503,808
512MB	1,001	16	63	1,009,008
1GB	2,002	16	63	2,018,016
2GB	4,003	16	63	4,035,024
4GB	8,006	16	63	8,070,048
8GB	16,000	16	63	16,128,000
16GB	16,383	16	63	32,492,880
32GB	16,383	16	63	64,331,568

3. *Interface Description*

3.1. *CF interface (Compact Flash Type I)*

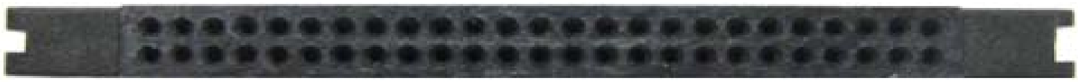


Figure 3: 50-pin Compact Flash Type I Connector

3.2. *Pin Assignments*

3.3. Signals whose source is the host is designated as inputs while signals that the Industrial Compact Flash (CF) Card sources are outputs. The pin assignments are listed in below table 7.

The signal/pin assignments are listed in below Table 7. Low active signals have a “-” prefix. Pin types are Input, Output or Input/Output.

Table 7: Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	**Signal Name**	**Pin Type**	**In, Out Type**	**Pin Num**	**Signal Name**	**Pin Type**	**In, Out Type**	**Pin Num**	**Signal Name**	**Pin Type**	**In, Out Type**
1	GND		Ground	**1**	GND		Ground	**1**	GND		Ground
2	D03	I/O	11Z,OZ3	**2**	D03	I/O	11Z,OZ3	**2**	D03	I/O	11Z,OZ3
3	D04	I/O	11Z,OZ3	**3**	D04	I/O	11Z,OZ3	**3**	D04	I/O	11Z,OZ3
4	D05	I/O	11Z,OZ3	**4**	D05	I/O	11Z,OZ3	**4**	D05	I/O	11Z,OZ3
5	D06	I/O	11Z,OZ3	**5**	D06	I/O	11Z,OZ3	**5**	D06	I/O	11Z,OZ3
6	D07	I/O	11Z,OZ3	**6**	D07	I/O	11Z,OZ3	**6**	D07	I/O	11Z,OZ3
7	-CE1	I	13U	**7**	-CE1	I	13U	**7**	-CS0	I	13Z
8	A10	I	11Z	**8**	A10	I	11Z	**8**	A10[2]	I	11Z
9	-OE	I	13U	**9**	-OE	I	13U	**9**	-ATA SEL	I	13U
10	A09	I	11Z	**10**	A09	I	11Z	**10**	A09[2]	I	11Z
11	A08	I	11Z	**11**	A08	I	11Z	**11**	A08[2]	I	11Z
12	A07	I	11Z	**12**	A07	I	11Z	**12**	A07[2]	I	11Z
13	VCC		Power	**13**	VCC		Power	**13**	VCC		Power
14	A06	I	11Z	**14**	A06	I	11Z	**14**	A06[2]	I	11Z
15	A05	I	11Z	**15**	A05	I	11Z	**15**	A05[2]	I	11Z
16	A04	I	11Z	**16**	A04	I	11Z	**16**	A04[2]	I	11Z
17	A03	I	11Z	**17**	A03	I	11Z	**17**	A03[2]	I	11Z
18	A02	I	11Z	**18**	A02	I	11Z	**18**	A02	I	11Z
19	A01	I	11Z	**19**	A01	I	11Z	**19**	A01	I	11Z
20	A00	I	11Z	**20**	A00	I	11Z	**20**	A00	I	11Z
21	D00	I/O	11Z,OZ3	**21**	D00	I/O	11Z,OZ3	**21**	D00	I/O	11Z,OZ3
22	D01	I/O	11Z,OZ3	**22**	D01	I/O	11Z,OZ3	**22**	D01	I/O	11Z,OZ3
23	D02	I/O	11Z,OZ3	**23**	D02	I/O	11Z,OZ3	**23**	D02	I/O	11Z,OZ3
24	WP	O	OT3	**24**	-IOIS16	O	OT3	**24**	-IOCS16	O	ON3
25	-CD2	O	Ground	**25**	-CD2	O	Ground	**25**	-CD2	O	Ground
26	-CD1	O	Ground	**26**	-CD1	O	Ground	**26**	-CD1	O	Ground
27	D11[1]	I/O	11Z,OZ3	**27**	D11[1]	I/O	11Z,OZ3	**27**	D11[1]	I/O	11Z,OZ3
28	D12[1]	I/O	11Z,OZ3	**28**	D12[1]	I/O	11Z,OZ3	**28**	D12[1]	I/O	11Z,OZ3
29	D13[1]	I/O	11Z,OZ3	**29**	D13[1]	I/O	11Z,OZ3	**29**	D13[1]	I/O	11Z,OZ3
30	D14[1]	I/O	11Z,OZ3	**30**	D14[1]	I/O	11Z,OZ3	**30**	D14[1]	I/O	11Z,OZ3

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	**Signal Name**	**Pin Type**	**In, Out Type**	**Pin Num**	**Signal Name**	**Pin Type**	**In, Out Type**	**Pin Num**	**Signal Name**	**Pin Type**	**In, Out Type**
31	D15[1]	I/O	11Z,OZ3	**31**	D15[1]	I/O	11Z,OZ3	**31**	D15[1]	I/O	11Z,OZ3
32	-CE2[1]	I	13U	**32**	-CE2[1]	I	13U	**32**	-CS1[1]	I	13Z
33	-VS1	O	Ground	**33**	-VS1	O	Ground	**33**	-VS1	O	Ground
34	-IORD	I	13U	**34**	-IORD	I	13U	**34**	-IORD[7] HSTROBE[8] -HDMARDY[9]	I	13Z
35	-IOWR	I	13U	**35**	-IOWR	I	13U	**35**	-IOWR[7] STOP[8.9]	I	13Z
36	-WE	I	13U	**36**	-WE	I	13U	**36**	-WE[3]	I	13U
37	READY	O	OT1	**37**	-IREQ	O	OT1	**37**	INTRQ	O	OZ1
38	VCC		Power	**38**	VCC		Power	**38**	VCC		Power
39	-CSEL[5]	I	12Z	**39**	-CSEL[5]	I	12Z	**39**	-CSEL	I	12U
40	-VS2	O	OPEN	**40**	-VS2	O	OPEN	**40**	-VS2	O	OPEN
41	RESET	I	12Z	**41**	RESET	I	12Z	**41**	-RESET	I	12Z
42	-WAIT	O	OT1	**42**	-WAIT	O	OT1	**42**	IORDY[7] -DDMARDY[8] DSTROBE[9]	O	ON1
43	-INPACK	O	OT1	**43**	-INPACK	O	OT1	**43**	DMARQ	O	OZ1
44	-REG	I	13U	**44**	-REG	I	13U	**44**	-DMACK[6]	I	13U
45	BVD2	O	OT1	**45**	-SPKR	O	OT1	**45**	-DASP	I/O	11U,ON1
46	BVD1	O	OT1	**46**	-STSCHG	O	OT1	**46**	-PDIAG	I/O	11U.ON1
47	D08[1]	I/O	11Z,OZ3	**47**	D08[1]	I/O	11Z,OZ3	**47**	D08[1]	I/O	11Z,OZ3
48	D09[1]	I/O	11Z,OZ3	**48**	D09[1]	I/O	11Z,OZ3	**48**	D09[1]	I/O	11Z,OZ3
49	D10[1]	I/O	11Z,OZ3	**49**	D10[1]	I/O	11Z,OZ3	**49**	D10[1]	I/O	11Z,OZ3
50	GND		Ground	**50**	GND		Ground	**50**	GND		Ground

Note:

1) *These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.*
2) *The signal should be grounded by the host.*
3) *The signal should be tied to VCC by the host.*
4) *The mode is optional for CF+ Cards, but required for Compact Flash Cards.*
5) *The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.*
6) *If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition*
7) *Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.*
8) *Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.*
9) *Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.*

3.4. *Electrical Description*

The Industrial Compact Flash Card is optimized for operation with hosts, which support the PCMCIA/ I/O interface standard conforming to the PC Card ATA specification. However, the Compact Flash Card may also be configured to operate in systems that support only the memory interface standard. The configuration of the Compact Flash Card will be controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the Compact Flash Card. Table 8: describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the Compact Flash Card sources are outputs. The Compact Flash Card logic levels conform to those specified in the *PCMCIA Release 2.1 Specification*. See Section 3.3 for definitions of Input and Output type.

Table 8: Signal Description

Signal Name	Dir	Pin	Description
A10 – A0 (PC Card Memory Mode) A10 – A0 (PC Card I/O Mode)	I	8,10,11,12,14,15,16,17,18,19,20	These address lines along with the –REG signal are used to select the following : The I/O port address registers within the Compact Flash Card or CF+ Card, the memory mapped port address registers within the Compact Flash Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers. This signal is the same as the PC Card Memory Mode signal.
A2 – A0 (True IDE Mode)	I	18,19,20	In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode) -STSCHG (PC Card I/O Mode) Status Changed -PDIAG (True IDE Mode)	I/O	46	This signal is asserted high, as BVD1 is not supported. This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. It use is controlled by the Card Config and Status Register. In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode) -SPKR (PC Card I/O Mode) -DASP (True IDE Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported. This line is the Binary Audio output from t he card. If the Card does not support the Binary Audio function, this line should be held negated. In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode) -CD1, -CD2 (PC Card I/O Mode) -CD1, -CD2 (True IDE Mode)	O	26,25	These Card Detect pins are connected to ground on the Compact Flash Card or CF+ Card. They are used by the host to determine that the Compact Flash Card or CF+ Card is fully inserte4d into its socket. This signal is the same for all modes. This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable -CE1, -CE2 (PC Card I/O Mode) Card Enable -CS0, -CS1 (True IDE Mode)	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, -CS0 is the chip select for the task file registers while –CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16bits.
-CSEL (PC Card Memory Mode) -CSEL (PC Card I/O Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.

Signal Name	Dir	Pin	Description
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When the pin is open, this device is configured as a Slave.
D15 – D00 (PC Card Memory Mode) D15 – D00 (PC Card I/O Mode) D15 – D00 (True IDE Mode)	I/O	31,30,29,28,27,49,48,47,6,5,4,3,2,23,22,21	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode) GND (PC Card I/O Mode) GND (True IDE Mode)	--	1,50	Ground This signal is the same for all modes. This signal is the same for all modes.
-INPACK (PC Card Memory Mode) -INPACK (PC Card I/O Mode) Input Acknowledge DMARQ (True IDE Mode)	O	43	This signal is not used in this mode. The Input Acknowledge signal is asserted by the Compact Flash Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the Compact Flash Card or CF+ Card and the CPU. This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by –IORD and –IOWR. This signal is used in a handshake manner with –DMACK, i.e., the device shall wait until the host asserts –DMACK before negating DMARQ and re-asserting DMARQ if there is more data to transfer. DMAARQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.
-IORD (PC Card Memory Mode) -IORD (PC Card I/O Mode) -IORD (True IDE Mode –Except Ultra DMA Protocol Active) -HDMARDY	I	34	This signal is not used in this mode. This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the Compact Flash Card or CF+ Card when the card is configured to use the I/O interface. In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode. In True IDE Mode when Ultra DMA mode DMA Read is active this

Signal Name	Dir	Pin	Description
(True IDE Mode – In Ultra DMA Protocol DMA Read) HSTROBE (True IDE Mode – In Ultra DMA Protocol DMA Write)			signal is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate –HDMARDY to pause an Ultra DMA transfer. In True IDE Mode when Ultra DMA mode DMA Write is active this signal is the data out strobe generated by the host. Both rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
-IOWR (PC Card Memory Mode) -IOWR (PC Card I/O Mode) -IOWR (True IDE Mode – Except Ultra DMA Protocol Active) STOP (True IDE Mode – Ultra DMA Protocol Active)	I	35	This signal is not used in this mode. The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the Compact Flash Card or CF+ Card controller registers when the Compact Flash Card or CF+ Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge). In True IDE Mode, while Ultra DMA mode protocol is not active this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol. In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
-OE (PC Card Memory Mode) -OE (PC Card I/O Mode) -ATA SEL (True IDE Mode)	I	9	This is an Output Enable Strobe Generated by the host interface. It is used to read data from the Compact Flash Card or CF+ Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. To enable True IDE Mode this input should be grounded by the host.
READY (PC Card Memory Mode) -IREQ (PC Card I/O Mode) INTRQ (True IDE Mode)	O	37	In Memory Mode, this signal is set high when the Compact Flash Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (bus) until the Compact Flash Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the Compact Flash Card or CF+ Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state. I/O Operation – After the Compact Flash Card or CF+ Card has been configured for I/O operation, this signal is used as –Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level ode interrupt. In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode) Attribute Memory Select -REG	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. The signal shall also be active (low) during I/O Cycles when the I/O

Signal Name	Dir	Pin	Description
(PC Card I/O Mode) -DMACK (True IDE Mode)			address is on the Bus. This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the –DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
RESET (PC Card Memory Mode) RESET (PC Card I/O Mode) -RESET (True IDE Mode)	I	41	The Compact Flash Card or CF+ Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The Compact Flash Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode) VCC (PC Card I/O Mode) VCC (True IDE Mode)	--	13,38	+5V, +3.3V power. This signal is the same for all modes. This signal is the same for all modes.
-VS1 -VS2 (PC Card Memory Mode) -VS1 -VS2 (PC Card I/O Mode) -VS1 -VS2 (True IDE Mode)	O	33 40	Voltage Sense Signals. –VS1 is grounded on the Card and sensed by the Host so that the Compact Flash Card or CF+ Card CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card. This signal is the same for all modes. This signal is the same for all modes.
-WAIT (PC Card Memory Mode) -WAIT (PC Card I/O Mode) IORDY (True IDE Mode –Except Ultra DMA Mode) -DDMARDY (True IDE Mode –Ultra DMA Write Mode) DSTROBE	O	42	The –WAIT signal is driven low by the Compact Flash Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY. In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate –DDMARDY to pause an Ultra DMA transfer. In True IDE Mode, when Ultra DMA mode DMA Write is active, this

Signal Name	Dir	Pin	Description
(True IDE Mode –Ultra DMA Read Mode)			signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
-WE (PC Card Memory Mode) -WE (PC Card I/O Mode) -WE (True IDE Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the Compact Flash Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect -IOIS16 (PC Card I/O Mode) -IOIS16 (True IDE Mode)	O	24	Memory Mode –The Compact Flash Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O Operation –When the Compact Flash Card or CF+ Card is configured for I/O Operation Pin 24 is used for the –I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

4. Electrical Specification

Table 10, Table 11, and Table 12 defines all D.C. Characteristics for the Industrial Compact Flash (CF) Card . Unless otherwise stated, a condition is as below Table 9:

Table 9: Electrical Condition

Commercial Grade	Industrial Grade
Vcc = 5V ±10%	Vcc = 5V ±10%
Vcc = 3.3V ± 10%	Vcc = 3.3V ± 10%
Ta = 0°C to 70°C	Ta = -40°C to 85°C

4.1. General DC Characteristics

4.1.1. Interface I/O at 5.0V

Table 10: Interface I/O at 5.0V

Symbol	Parameter	Min.	Max.	Units	Remark
V_{CC}	Power Supply	4.5	5.5	V	
V_{OH}	Output Voltage High Level	VCC-0.8		V	
V_{OL}	Output Voltage Low Level		0.8	V	
V_{IH}	Input Voltage High Level	2.92		V	Schmitt trigger[1]
V_{IL}	Input Voltage Low Level		1.70	V	Schmitt trigger[1]
T_{OPR-W}	Operating temperature for wide grade	-40	+85	□	
T_{OPR-S}	Operating temperature for standard grade	0	+70	□	
T_{STG}	Storage temperature	-40	125	□	
R_{PU}	Pull up resistance[2]	50	73	kOhm	
R_{PD}	Pull down resistance	50	97	kOhm	

4.1.2. Interface I/O at 3.3V

Table 11: Interface I/O at 3.3V

Symbol	Parameter	Min.	Max.	Units	Remark
V_{OH}	Power Supply	2.97	3.63	V	
V_{OL}	Output Voltage High Level	VCC-0.8		V	
V_{IH}	Output Voltage Low Level		0.8	V	
V_{IL}	Input Voltage High Level	2.05		V	Schmitt trigger[1]
V_{CC}	Input Voltage Low Level		1.25	V	Schmitt trigger[1]
T_{OPR-W}	Operating Temperature For Wide Grade	-40	+85	□	
T_{OPR-S}	Operating Temperature For Standard Grade	0	+70	□	
T_{STG}	Storage Temperature	-40	125	□	
R_{PU}	Pull up resistance2	52.7	141	kOhm	
R_{PD}	Pull down resistance	47.5	172	kOhm	

Notes:

1) *Include CE1, CE2, HREG, HOE, HIOE, HWE, HIOW pins.*
2) *Include CE1, CE2, HREG, HOE, HIOE, HWE, HIOW, CSEL, PDIAG, DASP pins.*

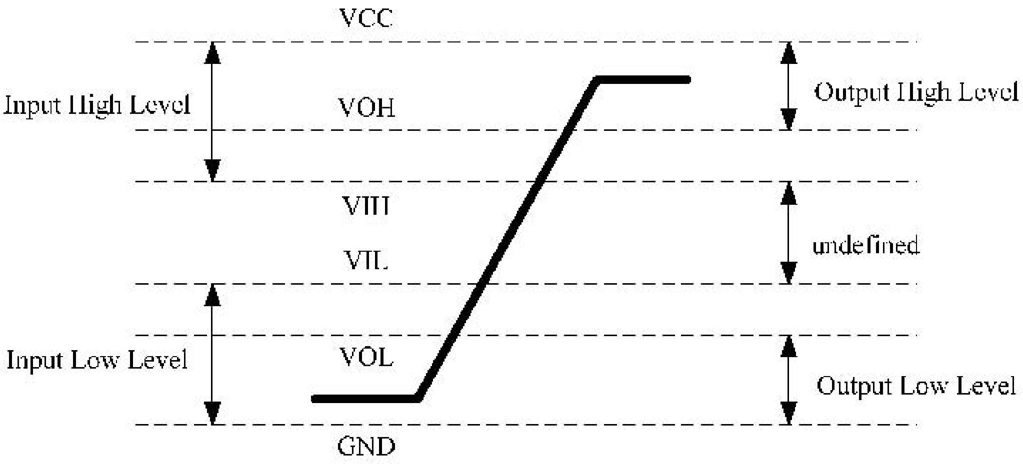


Figure 4: Interface I/O Voltage Diagram

4.2. *AC Characteristics*

4.2.1. Attribute Memory Read Timing

Table 12: Attribute Memory Read Timing

Speed Version	Symbol	300 ns	
Item		Min ns.	Max ns.
Read Cycle Time	tc (R)	300	
Address Access Time	ta (A)		300
Card Enable Access Time	ta (CE)		300
Output Enable Access Time	ta (OE)		150
Output Disable Time from CE	tdis (CE)		100
Output Disable Time from OE	tdis (OE)		100
Address Setup Time	tsu (A)	30	
Output Enable Time from CE	ten (CE)	5	
Output Enable Time from OE	ten (OE)	5	
Data Valid from Address Change	tv (A)	0	

Notes: All times are in nanoseconds. HD signifies data provided by the Compact Flash (CF) Card to the system. The CEx signal or both the HOE signal and the HWE signal shall be de-asserted between consecutive cycle operations.

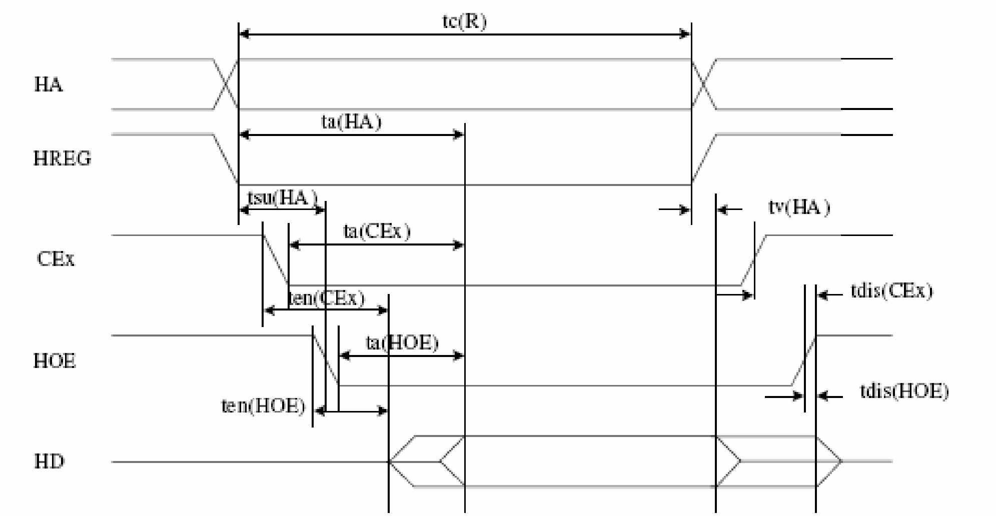


Figure 5: Attribute Memory Read Timing Diagram

4.2.2. Configuration Register (Attribute Memory) Write Time

Table 13: Configuration Register (Attribute Memory) Write Time

Speed Version	Symbol	250 ns	
Item		Min ns.	Max ns.
Write Cycle Time	tc (W)	250	
Write Pulse Width	tw (WE)	150	
Address Setup Time	tsu (A)	30	
Write Recovery Time	trec (WE)	30	
Data Setup Time for HWE	tsu (D-WEH)	80	
Data Hold Time	th (D)	30	

Notes: All times are in nanoseconds. HD signifies data provided by the system to the Compact Flash (CF) Card.

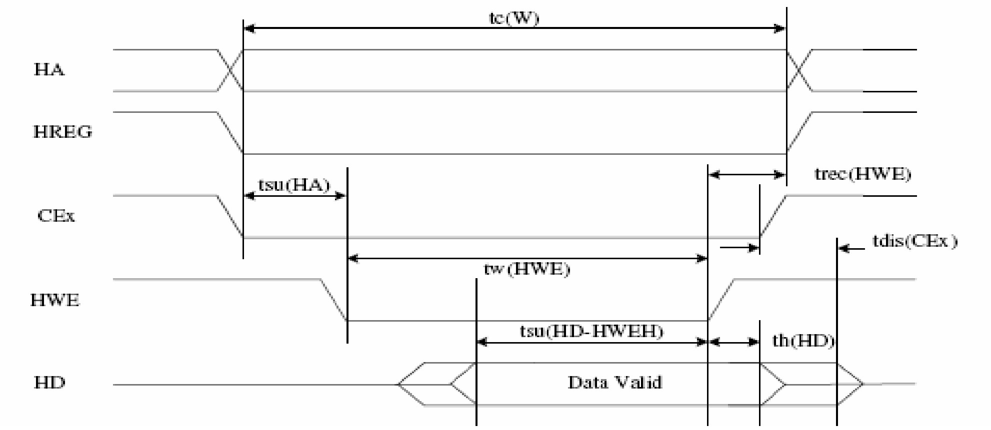


Figure 6: Configuration Register (Attribute Memory) Write Timing Diagram

4.2.3. Common Memory Read Timing

Table 14: Common Memory Read Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Output Enable Access Time	ta (OE)		125		60		50		40
Output Disable Time from	tdis (OE)		100		60		50		40
Address Setup Time	tsu (A)	30		15		10		10	
Address Hold Time	th (A)	20		15		15		10	
CE Setup before OE	tsu (CE)	0		0		0		0	
CE Hold following OE	th (CE)	20		15		15		10	
Wait Delay Falling from OE	tv (WT-OE)		35		35		35		Na[1]
Data Setup for Wait Release	tv (WT)		0		0		0		Na[1]
Wait Width Time [2]	tw (WT)		350		350		350		Na[1]

Notes:

1) *IORDY is not supported in this mode*

2) *The Maximum load on IORDY is 1 LSTTL with 50pF (40pF below 120 nsec Cycle Time) total load. All times are in nanoseconds. HD signifies data provided by the Compact Flash (CF) Card to the system. The IORDYsignal may be ignored if the HOE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure.*

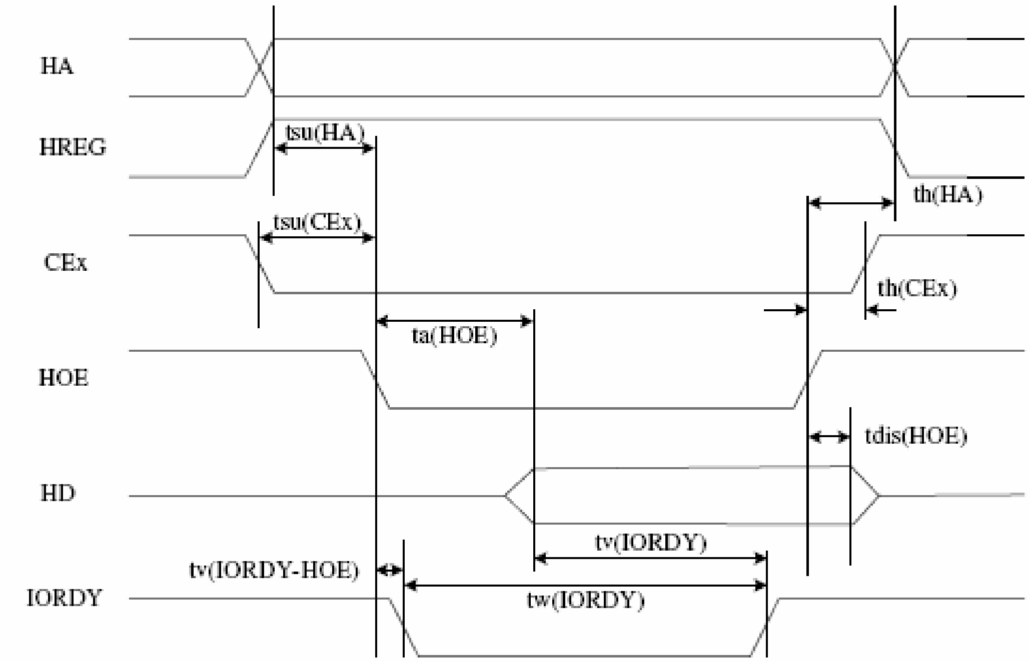


Figure 7: Common Memory Read Timing Diagram

4.2.4. Common Memory Write Timing

Table 15: Common Memory Write Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before WE	tsu (D-WEH)	80		50		40		30	
Data Hold following WE	th (D)	30		15		10		10	
WE Pulse Width	tw (WE)	150		70		60		55	
Address Setup Time	tsu (A)	30		15		10		10	
CE Setup before OE	tsu (CE)	0		0		0		0	
Write Recovery Time	trec (WE)	30		15		15		15	
Address Hold Time	th (A)	20		15		15		15	
CE Hold following OE	th (CE)	20		15		15		10	
Wait Delay Falling from OE	tv (WT-OE)		35		35		35		Na[1]
WE High from Wait Release	tv (WT)		0		0		0		Na[1]
Wait Width Time [2]	tw (WT)		350		350		350		Na[1]

Notes:

1) *IORDY is not supported in this mode*
2) *The Maximum load on IORDY is 1 LSTTL with 50pF (40pF below 120 nsec Cycle Time) total load. All times are in nanoseconds. HD signifies data provided by the Compact Flash (CF) Card to the system. The IORDYsignal may be ignored if the HOE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure.*

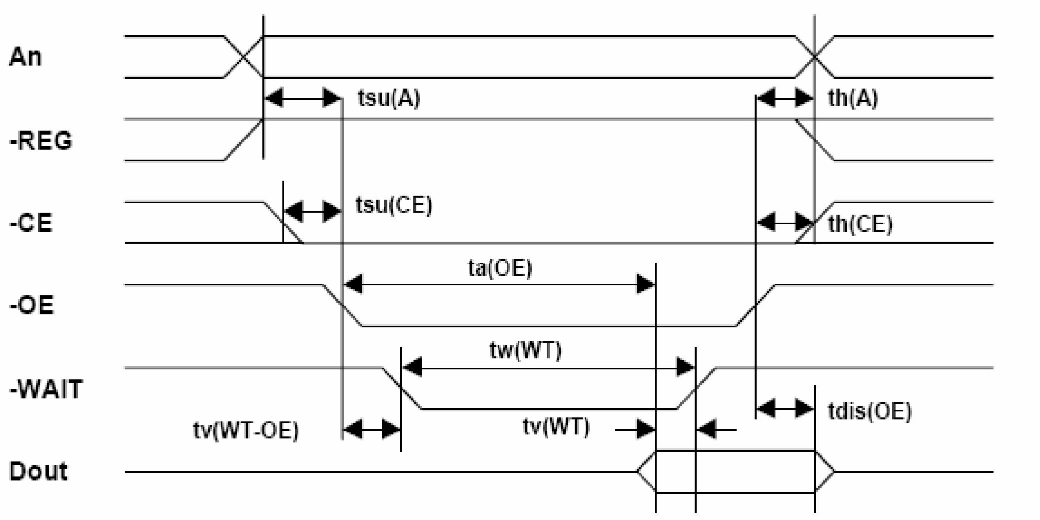


Figure 8: Common Memory Read Timing Diagram

4.2.5. I/O Read Timing

Table 16: I/O Read Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Delay after IORD	td (IORD)		100		50		50		45
Data Hold following IORD	th (IORD)	0		5		5		5	
IORD Width Time	tw (IORD)	165		70		65		55	
Address Setup before IORD	tsuHA (IORD)	70		25		25		15	
Address Hold following IORD	thA (IORD)	20		10		10		10	
CE Setup before IORD	tsuCE (IORD)	5		5		5		5	
CE Hold following IORD	thCE (IORD)	20		10		10		10	
REG Setup before IORD	tsuREG(IORD)	5		5		5		5	
REG Hold following IORD	thREG (IORD)	0		0		0		0	
INPACK Delay Falling from IORD	tdFINPACK (IORD)	0	45	0	Na[1]	0	Na[1]	0	Na[1]
INPACK Delay Rising from IROD	tdrINPACK(IORD)		45		Na[1]		Na[1]		Na[1]
IOIS16 Delay Falling From Address	tdfIOIS16(ADR)		35		Na[1]		Na[1]		Na[1]
IOIS16 Delay Rising From Address	tdrIOIS16(ADR)		35		Na[1]		Na[1]		Na[1]
Wait Delay Falling From IORD	tdWT(IORD)		35		35		35		Na[2]
Data Delay from Wait Rising	td(WT)		0		0		0		Na[2]
Wait Width Time [2]	tw(WT)		350		350		350		Na[2]

Notes:1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the Compact Flash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this spec.

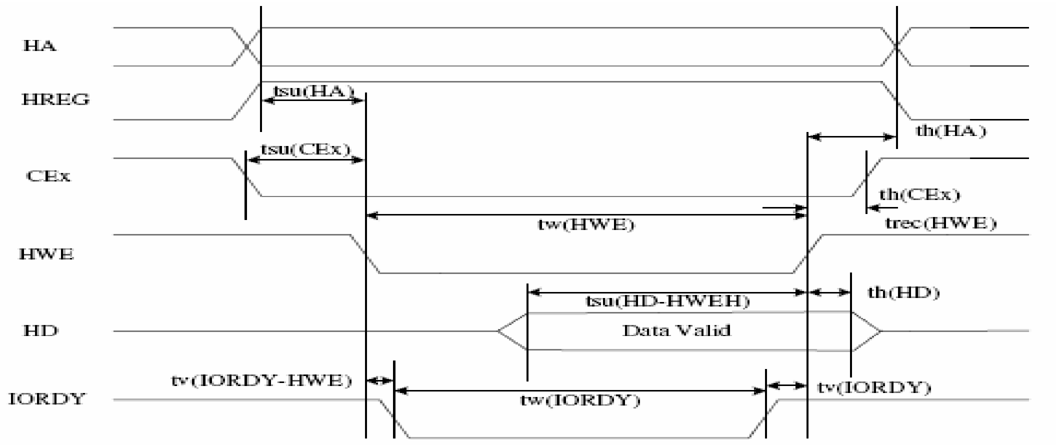


Figure 9: I/O Read Timing Diagram

4.2.6. I/O Write Timing

Table 17: I/O Write Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before IOWR	tsu (IOWR)	60		20		20		15	
Data Hold following IOWR	th (IOWR)	30		10		5		5	
IOWR Width Time	tw (IOWR)	165		70		65		55	
Address Setup before IOWR	tsuA (IOWR)	70		25		25		15	
Address Hold following IOWR	thA (IOWR)	20		20		10		10	
CE Setup before IOWR	tsuCE (IOWR)	5		5		5		5	
CE Hold following IOWR	thCE (IOWR)	20		20		10		10	
REG Setup before IOWR	tsuREG(IOWR)	5		5		5		5	
REG Hold following IOWR	thREG (IOWR)	0		0		0		0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)		35		Na[1]		Na[1]		Na[1]
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)		35		Na[1]		Na[2]		Na[2]
Wait Delay Falling from IOWR	tdWT(IOWR)		35		35		Na[2]		Na[2]
IOWR High from Wait High [2]	tdrIOWR(WT)	0		0		0			Na[2]
Wait Width Time [2]	tw(IORDY)		350		350		350		Na[1]

Notes: 1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall still be met. Din signifies data provided by the system to the Compact Flash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA specification of 12 μs but is intentionally less in this specification.

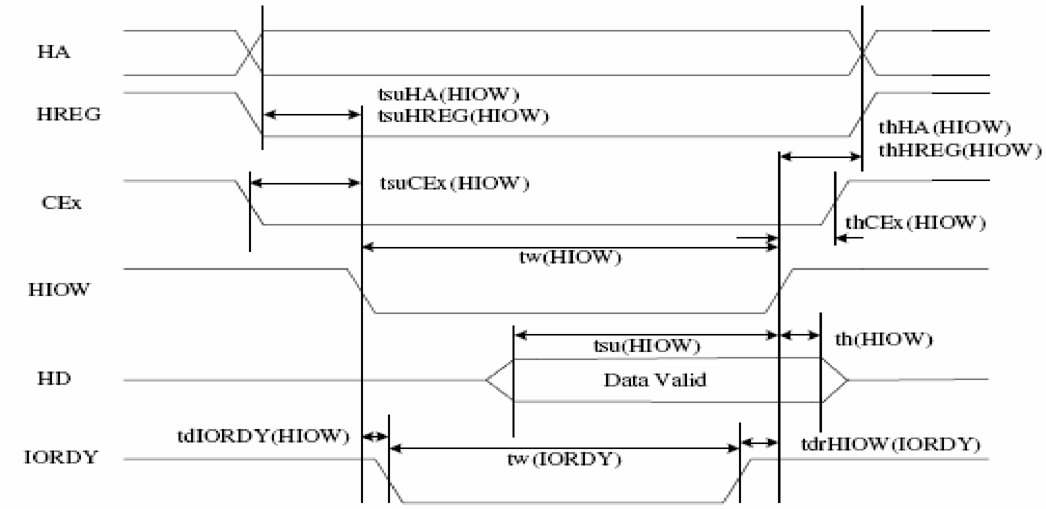


Figure 10: I/O Write Timing Diagram

4.2.7. True IDE PIO Mode Read/Write Timing

Table 18: True IDE PIO Mode Read/Write Timing

Item		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t0	Cycle time (min)1	600	383	240	180	120
t1	Address Valid to HIOR/HIOW setup (min)	70	50	30	30	25
t2	HIOR/HIOW (min)1	165	125	100	80	70
t2	HIOR/HIOW (min) Register (8 bit)1	290	290	290	80	70
t2i	HIOR/HIOW recovery time (min)1	-	-	-	70	25
t3	HIOW data setup (min)	60	45	30	30	20
t4	HIOW data hold (min)	30	20	15	10	10
t5	HIOR data setup (min)	50	35	20	20	20
t6	HIOR data hold (min)	5	5	5	5	5
t6Z	HIOR data tristate (max)2	30	30	30	30	30
t7	Address valid to IOCS16 assertion (max)4	90	50	40	n/a	n/a
t8	Address valid to IOCS16 released (max)4	60	45	30	n/a	n/a
t9	HIOR/HIOW to address valid hold	20	15	10	10	10
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0
tA	IORDY Setup time3	35	35	35	35	35
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250
tC	IORDY assertion to release (max)	5	5	5	5	5

Notes:

(1) All timings are in nanoseconds. The maximum load on IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from IORDY high to HIOE high is 0 nsec, but minimum HIOE width shall still be met. (1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data.

(2) This parameter specifies the time from the negation edge of HIOE to the time that the data bus is no longer driven by the device.

(3)The delay from the activation of HIOE or HIOW until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the device is not driving IORDY negated at tA after the activation of HIOE or HIOW, then t5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time tA after the activation of HIOE or HIOW, then tRD shall be met and t5 is not applicable. (4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid. (5) IORDY is not supported in this mode.

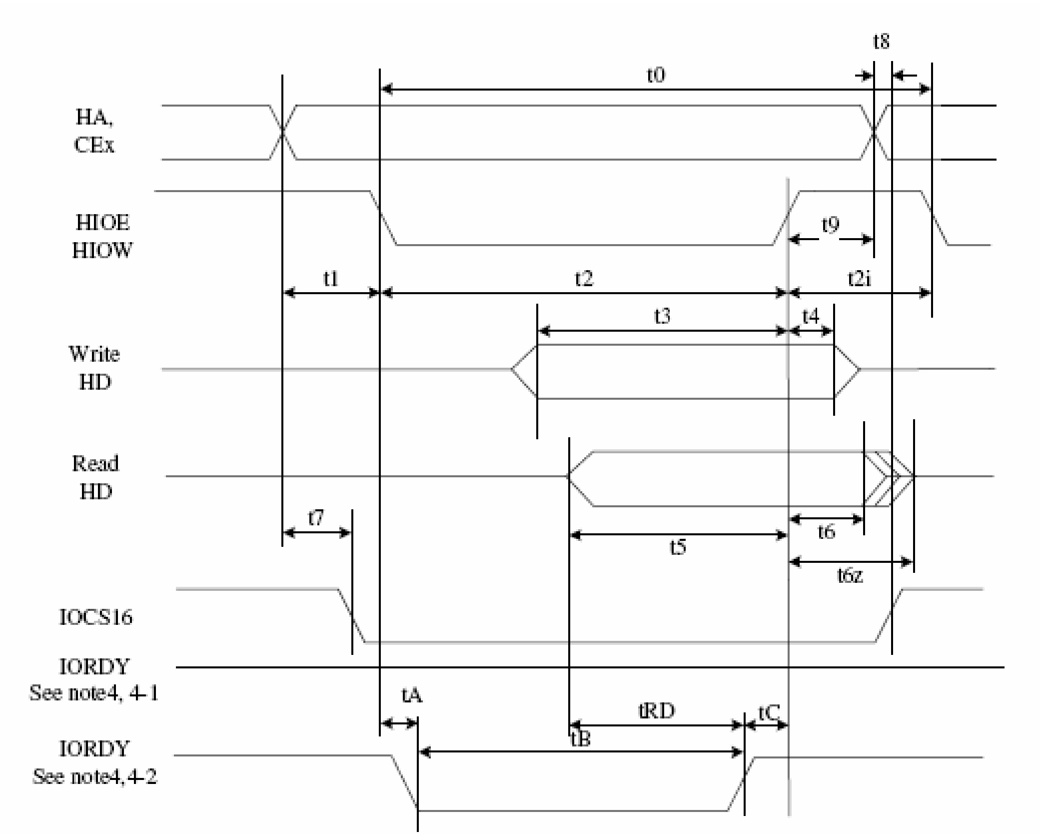


Figure 11: True IDE PIO Mode Read/Write Timing Diagram

Notes:

1) *Device address consists of CE0, CE1, and HA [2:0]*
2) *Data consist of HD [15:00] (16-bit) or HD [7:0] (8-bit)*
3) *IOCS16 is shown for PIO modes 0, 1, and 2. For other modes, this signal is ignored.*
4) *The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of HIOE or HIOW. The assertion and negation of IORDY is described in the following three cases:*
   - *4-1) Device never negates IORDY: No wait is generated.*
   - *4-2) Device drives IORDY low before tA: wait generated. The cycle complete after IORDY is reasserted. For cycles where a wait is generated and HIOE is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.*

4.2.8. True IDE Multiword DMA Mode Read/Write Timing

Table 19: True IDE Multiword DMA Mode Read/Write Timing

Item		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note
t_0	Cycle time (min)	480	150	120	100	80	1
t_D	HIOR / HIOW asserted width (min)	215	80	70	65	55	1
t_E	HIOR data access (max)	150	60	50	50	45	
t_F	HIOR data hold (min)	5	5	5	5	5	
t_G	HIOR/ HIOW data setup (min)	100	30	20	15	10	
t_H	HIOW data hold (min)	20	15	10	5	5	
t_I	DMACK(HREG) to HIOR/HIOW setup (min)	0	0	0	0	0	
t_J	HIOR / HIOW to -DMACK hold (min)	20	5	5	5	5	
t_{KR}	HIOR negated width (min)	50	50	25	25	20	1
t_{KW}	HIOW negated width (min)	215	50	25	25	20	1
t_{LR}	HIOR to DMARQ delay (max)	120	40	35	35	35	
t_{LW}	HIOW to DMARQ delay (max)	40	40	35	35	35	
t_M	CS1 CS0 valid to HIOR / HIOW	50	30	25	10	5	
t_N	CS1 CS0 hold	15	10	10	10	10	
t_Z	DMACK-	20	25	25	25	25	

Notes: t0 is the minimum total cycle time and tD is the minimum command active time, while tKR and tKW are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, tD, tKR, and tKW shall be met. The minimum total cycle time requirement is greater than the sum of tD and tKR or tKW for input and output cycles respectively. This means a host implementation can lengthen either or both of tD and either of tKR, and tKW as needed to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A device implementation shall support any legal host implementation.

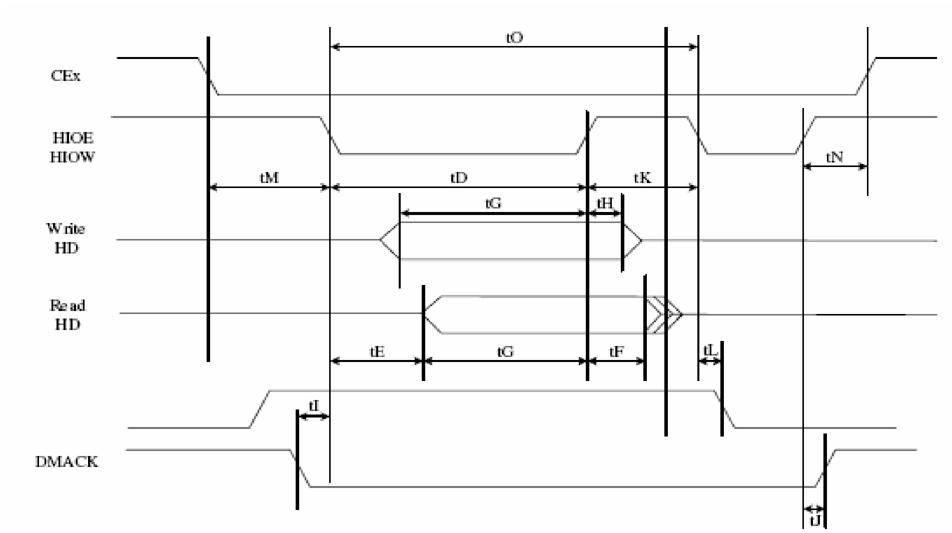


Figure 12: True IDE Multiword DMA Mode Read/Write Timing Diagram

Notes:

1) *If the Compact Flash (CF) Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.*

2) *This signal may be negated by the host to suspend the DMA transfer in progress.*

4.2.9. Ultra DMA Signal in Each Interface Mode

Table 20: Ultra DMA Signal in True IDE Mode

Signal	Type	(Non UDMA Memory Mode)	PC Card Memory Mode UDMA	PC Card IO Mode UDMA	TRUE IDE MODE UDMA
DMARQ	Output	(-INPACK)	-DMARQ	-DMARQ	DMARQ
HREG	Input	(-REG)	- DMARQ	DMARQ	- DMARQ
HIOW	Input	(-IOWR)	STOP[1]	STOP[1]	STOP[1]
HIOE	Input	(-IORD)	-HDMARDY(R) [1,2] HSTROBE(W) [1,3,4]	-HDMARDY(R) [1,2] HSTROBE(W) [1,3,4]	-HDMARDY(R) [1,2] HSTROBE(W) [1,3,4]
IORDY	Output	(-WAIT)	-DDMARDY(W) [1,3] DSTROBE(R) [1,2,4]	-DDMARDY(W) [1,3] DSTROBE(R) [1,2,4]	-DDMARDY(W) [1,3] DSTROBE(R) [1,2,4]
HD〔15:00〕	Bidir	(D〔15:00〕)	D〔15:00〕	D〔15:00〕	D〔15:00〕
HA〔10:00〕	Input	(A〔10:00〕)	A〔10:00〕[5]	A〔10:00〕[5]	A〔02:00〕[5]
CSEL	Input	(-CSEL)	-CSEL	-CSEL	-CSEL
HIRQ	Output	(READY)	READY	-INTRQ	INTRQ
CE1 CE2	Input	(-CE1) (-CE2)	-CE1 -CE2	-CE1 -CE2	-CS0 -CS1

Notes:

1) *The UDMA interpretation of this signal is valid only during an Ultra DMA data burst.*
2) *The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Read command.*
3) *The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.*
4) *The HSTROBE signals are active on both the rising and the falling edge.*
5) *Address lines 03 through 10 are not used in True IDE mode.*

4.2.10. Ultra DMA Data Burst Timing Requirement

Table 21: Ultra DMA Data Burst Timing Requirement

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		Measure Location2 (See Note 2)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t2CYCTYP	240		160		120		90		60		Sender
tCYC	112		73		54		39		25		Note3
t2CYC	230		153		115		86		57		Sender
tDS	15.0		10.0		7.0		7.0		5.0		Recipient
tDH	5.0		5.0		5.0		5.0		5.0		Recipient
tDVS	70.0		48.0		31.0		20.0		6.7		Sender
tDVH	6.2		6.2		6.2		6.2		6.2		Sender
tCS	15.0		10.0		7.0		7.0		5.0		Device
tCH	5.0		5.0		5.0		5.0		5.0		Device
tCVS	70.0		48.0		31.0		20.0		6.7		Host
tCVH	6.2		6.2		6.2		6.2		6.2		Host
tZFS	0		0		0		0		0		Device
tDZFS	70.0		48.0		31.0		20.0		6.7		Sender
tFS		230		200		170		130		120	Device
tLI	0	150	0	150	0	150	0	100	0	100	Note4
tMLI	20		20		20		20		20		Host
tUI	0		0		0		0		0		Host
tAZ		10		10		10		10		10	Note5
tZAH	20		20		20		20		20		Host
tZAD	0		0		0		0		0		Device
tENV	20	70	20	70	20	70	20	55	20	55	Host
tRFS		75		70		60		60		60	Sender
tRP	160		125		100		100		100		Recipient
tIORDYZ		20		20		20		20		20	Device
tZIORDY	0		0		0		0		0		Device
tACK	20		20		20		20		20		Host
tSS	50		50		50		50		50		Sender

Notes: All Timings in ns

1) *All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.*
2) *All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and -DMARDY transitions are measured at the sender connector.*
3) *The parameter tCYC shall be measured at the recipient's connector farthest from the sender.*
4) *The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.*
5) *The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.*
6) *See the AC Timing requirements in 4.2.12.Ultra DMA AC Signal Requirements.*

4.2.11. Ultra DMA Data Burst Timing Descriptions

Table 22: Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
T2CYCTYP	Typical sustained average two cycle time	
tCYC	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t2CYC	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge next falling edge of STROBE)	
tDS	Data setup time at recipient (from data valid until STROBE edge)	2,5
tDH	Data hold time at recipient (from STROBE edge until data may become invalid)	2,5
tDVS	Data valid setup time at sender (from data valid until STROBE edge)	3
tDVH	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
tCS	CRC word setup time at device	2
tCH	CRC word hold time device	2
tCVS	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
tCVH	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
tZFS	Time from STROBE output released-to-driving until the first transition of critical timing.	
tDZFS	Time from data output released-to-driving until the first transition of critical timing.	
tFS	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
tLI	Limited interlock time	1
tMLI	Interlock time with minimum	1
tUI	Unlimited interlock time	1
tAZ	Maximum time allowed for output drivers to release (from asserted or negated)	
tZAH	Minimum delay time required for output	
tZAD	drivers to assert or negate (from released)	
tENV	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
tRFS	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
tRP	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
tIORDYZ	Maximum time before releasing IORDY	
tZIORDY	Minimum time before driving IORDY	4
tACK	Setup and hold times for -DMACK (before assertion or negation)	
tSS	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

(1) The parameters tUI, tMLI (in Figure16: Ultra DMA Data-In Burst Device Termination Timing and Figure 17: Ultra DMA Data-In Burst Host Termination Timing), and tLI indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. tUI is an unlimited interlock that has no maximum time value. tMLI is a limited time-out that has a defined minimum. tLI is a limited time-out that has a defined maximum.

(2) 80-conductor cablingshall be required in order to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes greater than 2.

(3) Timing for tDVS, tDVH, tCVS and tCVH shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

(4) For all timing modes the parameter tZIORDY may be greater than tENV due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

(5) The parameters tDS, and tDH for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for tDS and tDH for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

4.2.12. Ultra DMA Sender and Recipient IC Timing Requirements

Table 23: Ultra DMA Sender and Recipient IC Timing Requirements

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tDSIC	14.7		9.7		6.8		6.8		4.8	
tDHIC	4.8		4.8		4.8		4.8		4.8	
tDVSIC	72.9		50.9		33.9		22.6		9.5	
tDVHIC	9.0		9.0		9.0		9.0		9.0	
tDSIC	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)									
tDHIC	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)									
tDVSIC	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)									
tDVHIC	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)									

Notes:

(1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

(2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V).

(3) The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

4.2.13. Ultra DMA AC Signal Requirements

Table 24: Ultra DMA AC Signal Requirements

Name	Comment	Min [V/ns]	Max [V/ns]	Notes
SRISE	Rising Edge Slew Rate for any signal		1.25	1
SFALL	Falling Edge Slew Rate for any signal		1.25	1

Notes:

(1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector. The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values. Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

4.2.14. Ultra DMA Data-In Burst Initiation Timing

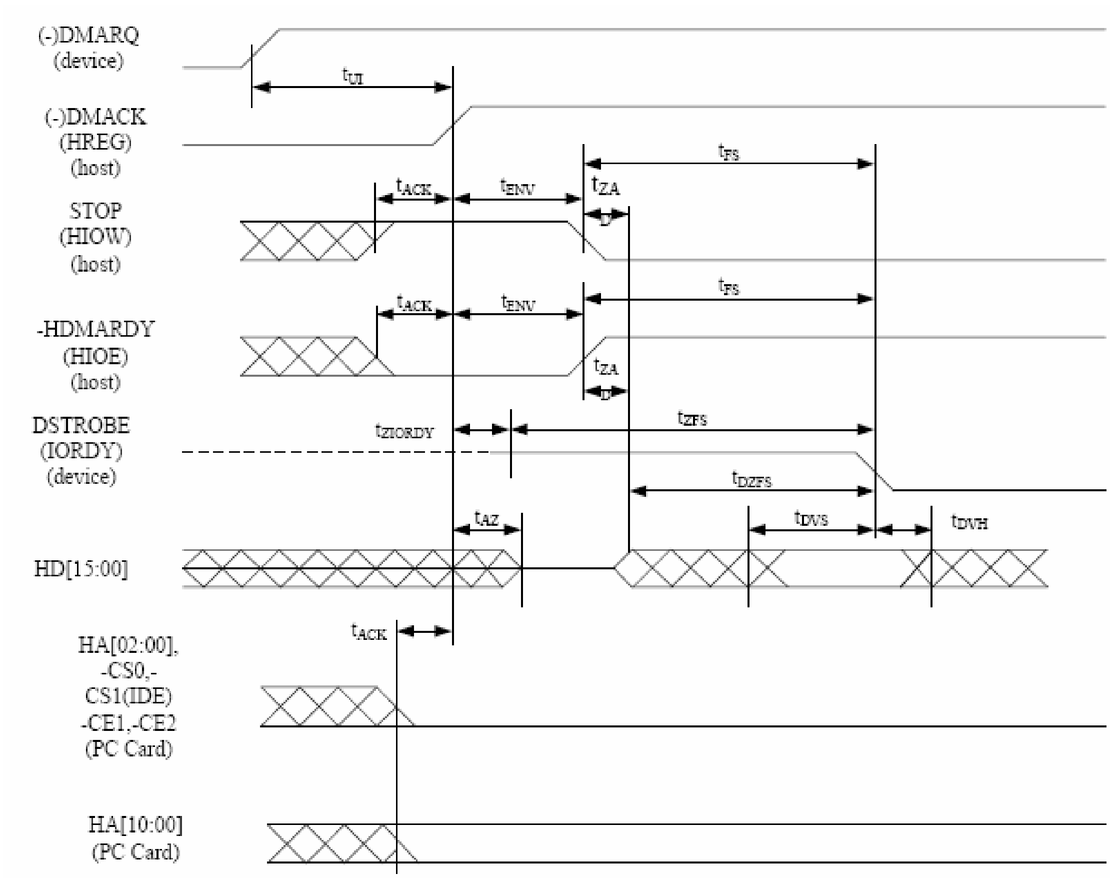


Figure 13: Ultra DMA Data-in Burst Initiation Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.
Notes: The definitions for the IORDY:-DDMARDY: DSTROBE,-IORD:-HDMARDY: HSTROBE,
and –IOWR:STOP signal lines are not in effect until DMARQ and –DMACK are asserted.
HA〔02:00〕,-CS0 & -CS1 are True IDE mode signal definitions. *HA*〔10:00〕,-CE1 and –CE2
are PC Card mode signals. The Bus polarity of (-) DMACK and (-) DMARQ are dependent
on interface mode active.

4.2.15. Sustained Ultra DMA Data-In Burst Timing

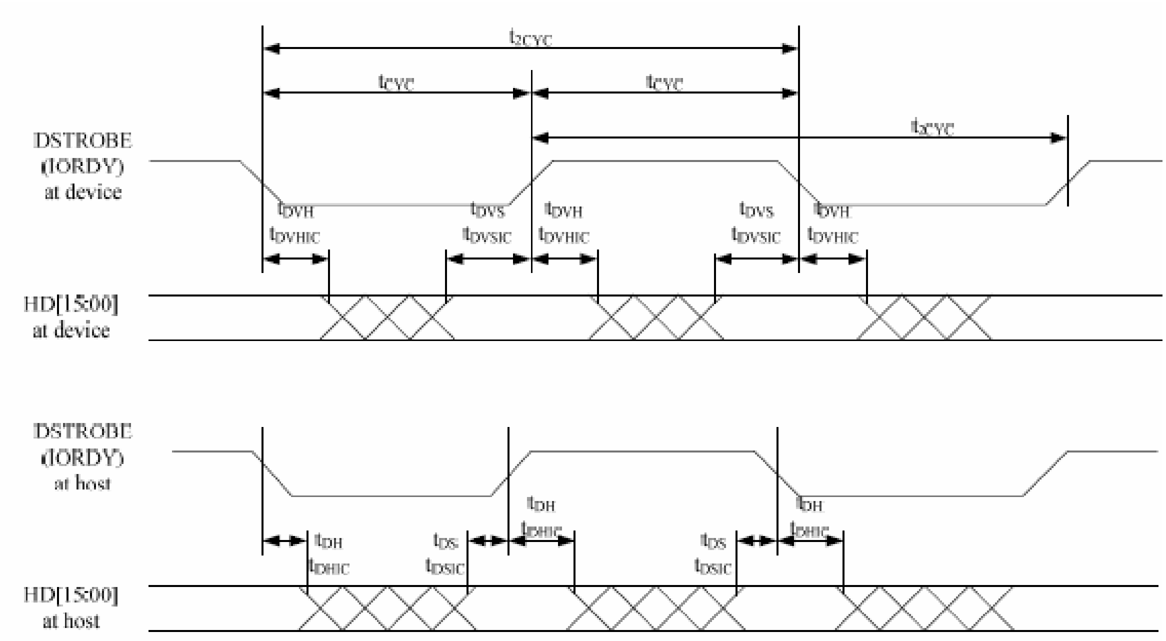


Figure 14: Sustained Ultra DMA Data-in Burst Initiation Timing Diagram

Note:
HD [15:00] and DSTROBE signals are shown at both the host and the device to emphasize that cable setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

4.2.16. Ultra DMA Data-In Burst Host Pause Timing

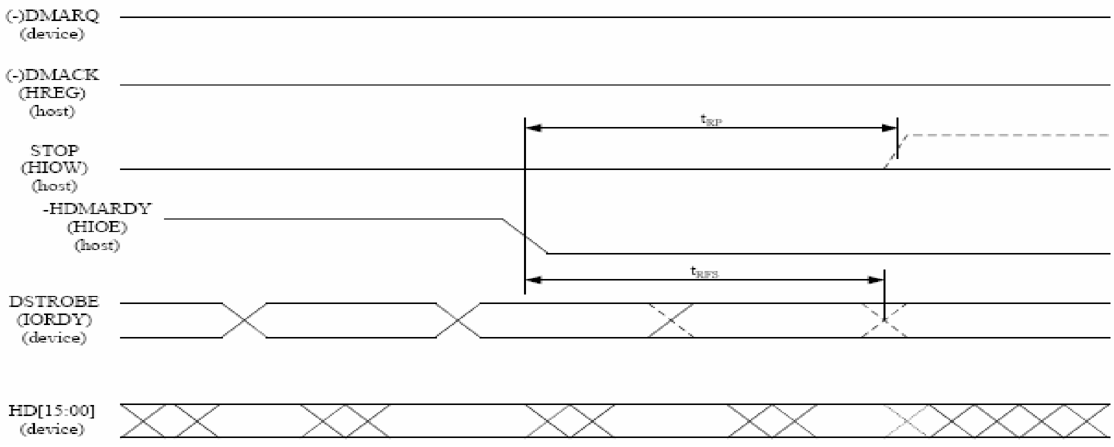


Figure 15: Ultra DMA Data-In Burst Host Pause Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

(1) The host may assert STOP to request termination of the Ultra DMA data burst no sooner than tRP after –HDMARY is negated.

(2) After negating –HDMARDY, the host may receive zero, one, two, or three more data words from the device.

(3) The bus polarity of the (-) DMARQ and (-) DMACK signals is dependent on the active interface mode.

4.2.17. Ultra DMA Data-In Burst Device Termination Timing

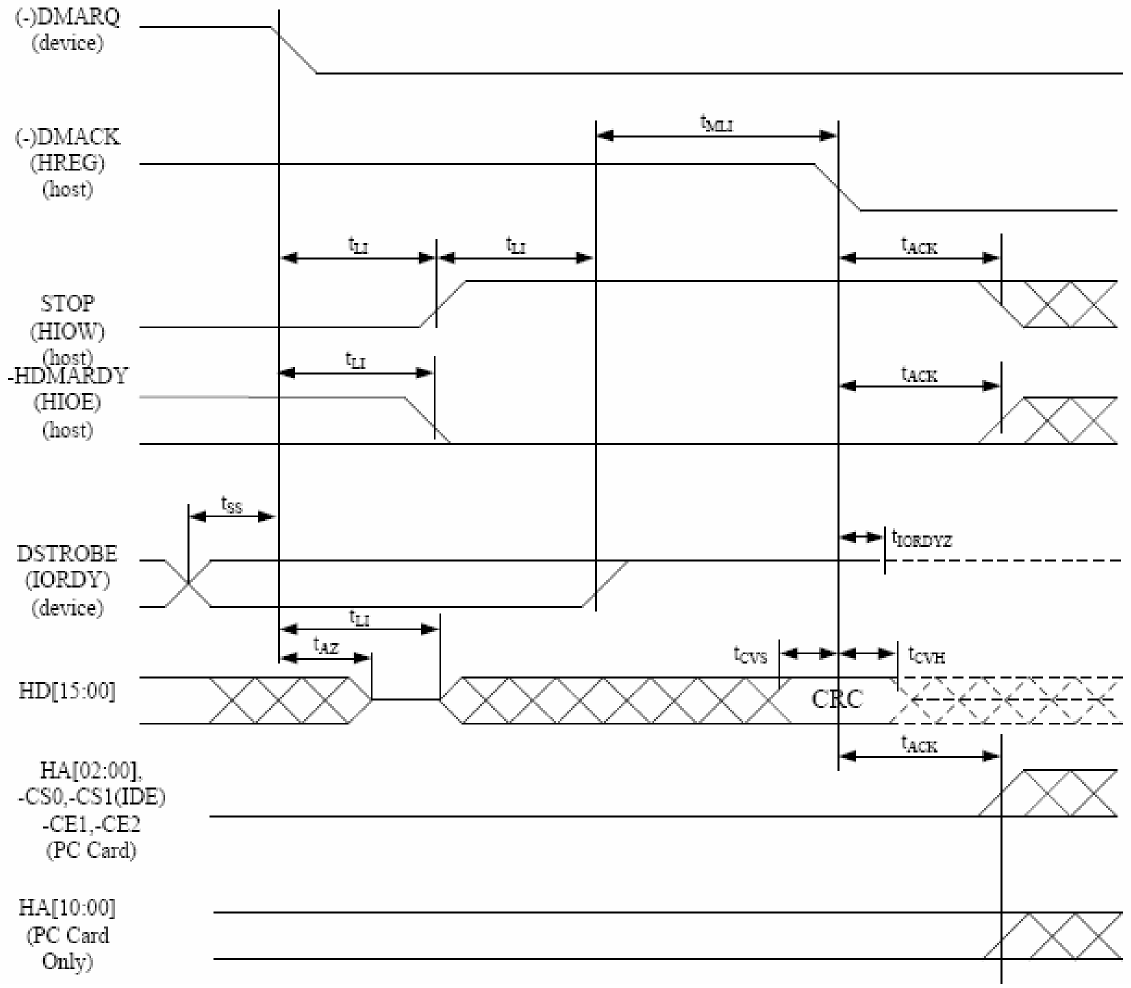


Figure 16: Ultra DMA Data-In Burst Device Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[02:00], -CS0& -CS1 are True IDE mode signal definitions. HA[10:00], -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

4.2.18. Ultra DMA Data-In Burst Host Termination Timing

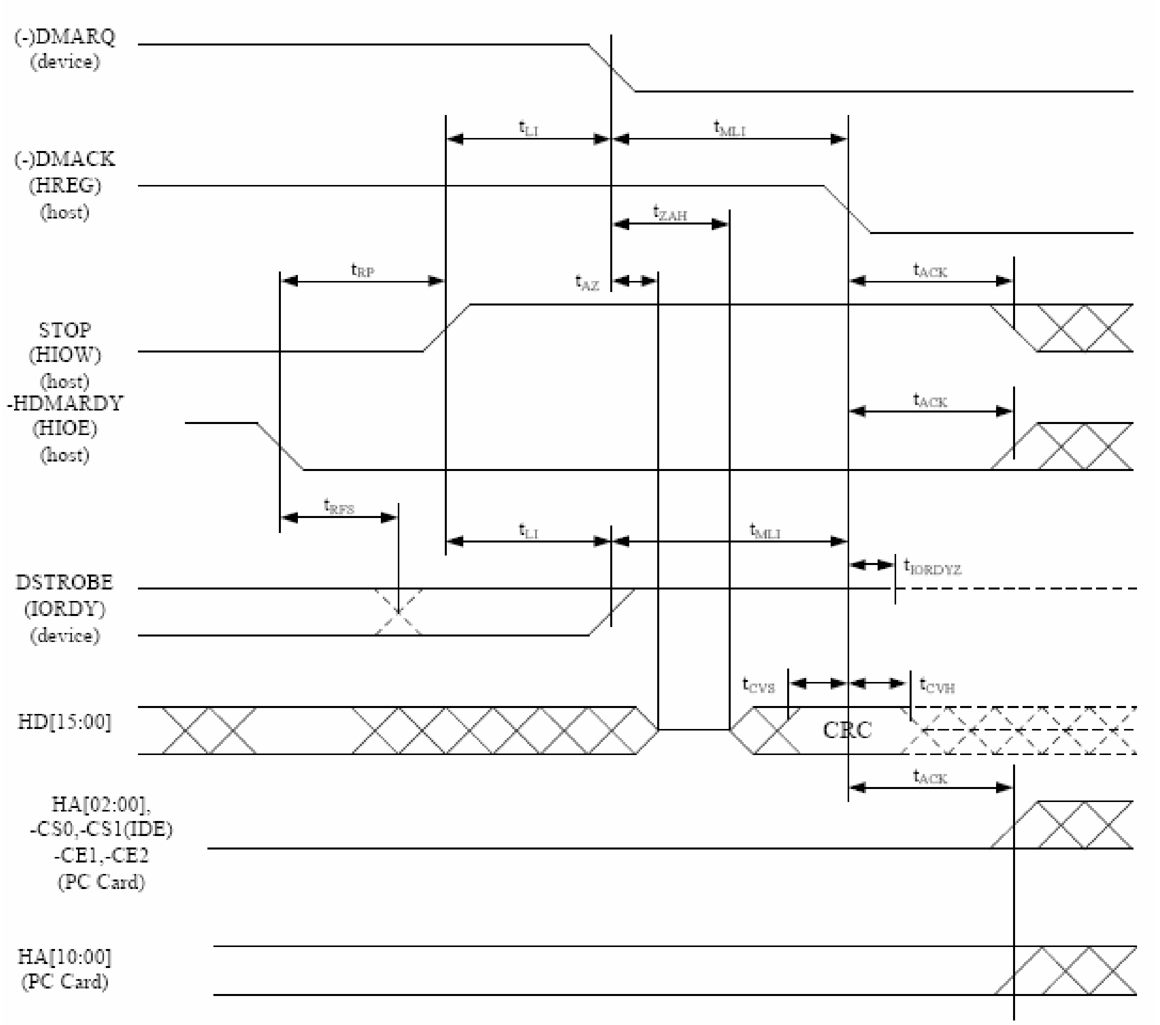


Figure 17: Ultra DMA Data-In Burst Host Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[02:00], -CS0& -CS1 are True IDE mode signal definitions. HA[10:00], -CE1 and –CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

4.2.19. Ultra DMA Data-Out Burst Host Initiation Timing

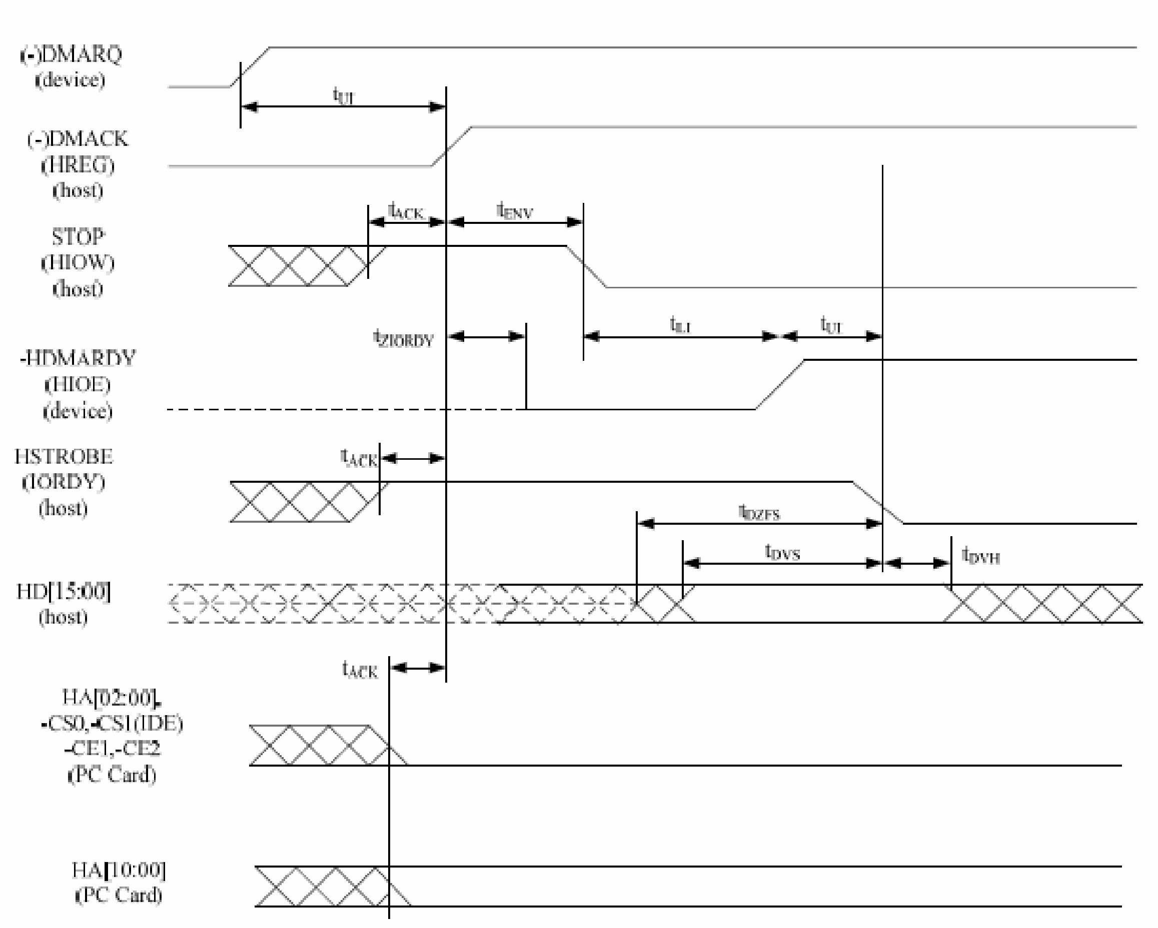


Figure 18: Ultra DMA Data-Out Burst Initiation Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, DDMARD, and HSTROBE signal lines are no in effect after DMARQ and DMACK are asserted. HA[02:00], -CS0& -CS1 are True IDE mode signal definitions. HA[10:00], -CE1 and -CE2 are PC Card mode signals definitions. The bus polarity of DMARQ and DMACK dependent on the active interface mode

4.2.20. Sustained Ultra DMA Data-Out Burst Host Initiation Timing

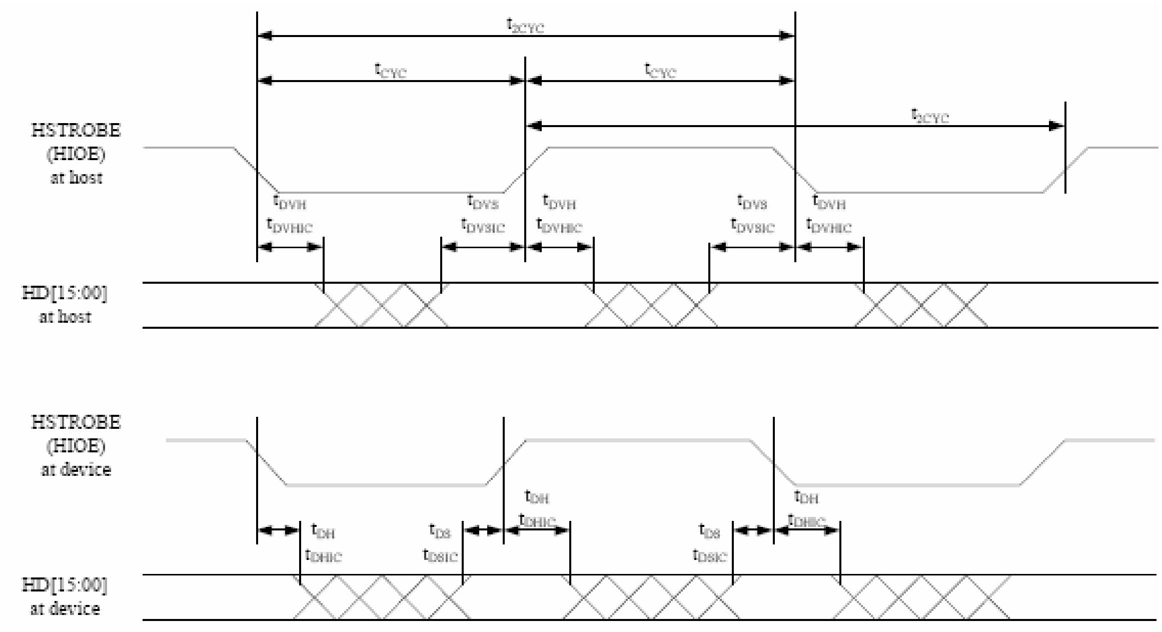


Figure 19: Sustained Ultra DMA Data-Out Burst Timing Diagram

Notes: Data (HD[15:00]) and HSTROBE signals are shown at both the device and the host to emphasize that cable Setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

4.2.21. Ultra DMA Data-Out Burst Device Pause Timing

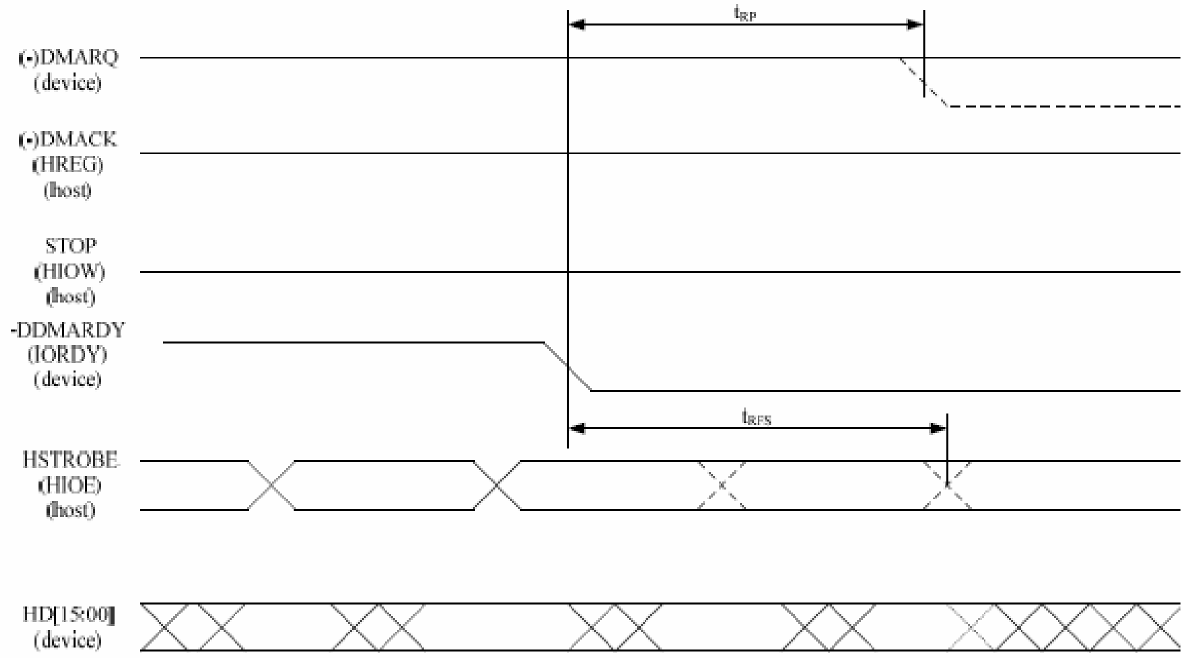


Figure 20: Ultra DMA Data-out Burst Device Pause Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: (1) The device may negate DMARQ to request termination of the Ultra DMA data burst no sooner than tRP after –DDMARDY, is negated.

(2) After negating –DDMARDY, the device may receive zero, one, two, or three more data words from the host.

(3) The bus polarity of DMARQ and DMACK depend on the active interface mode.

4.2.22. Ultra DMA Data-Out Burst Device Termination Timing

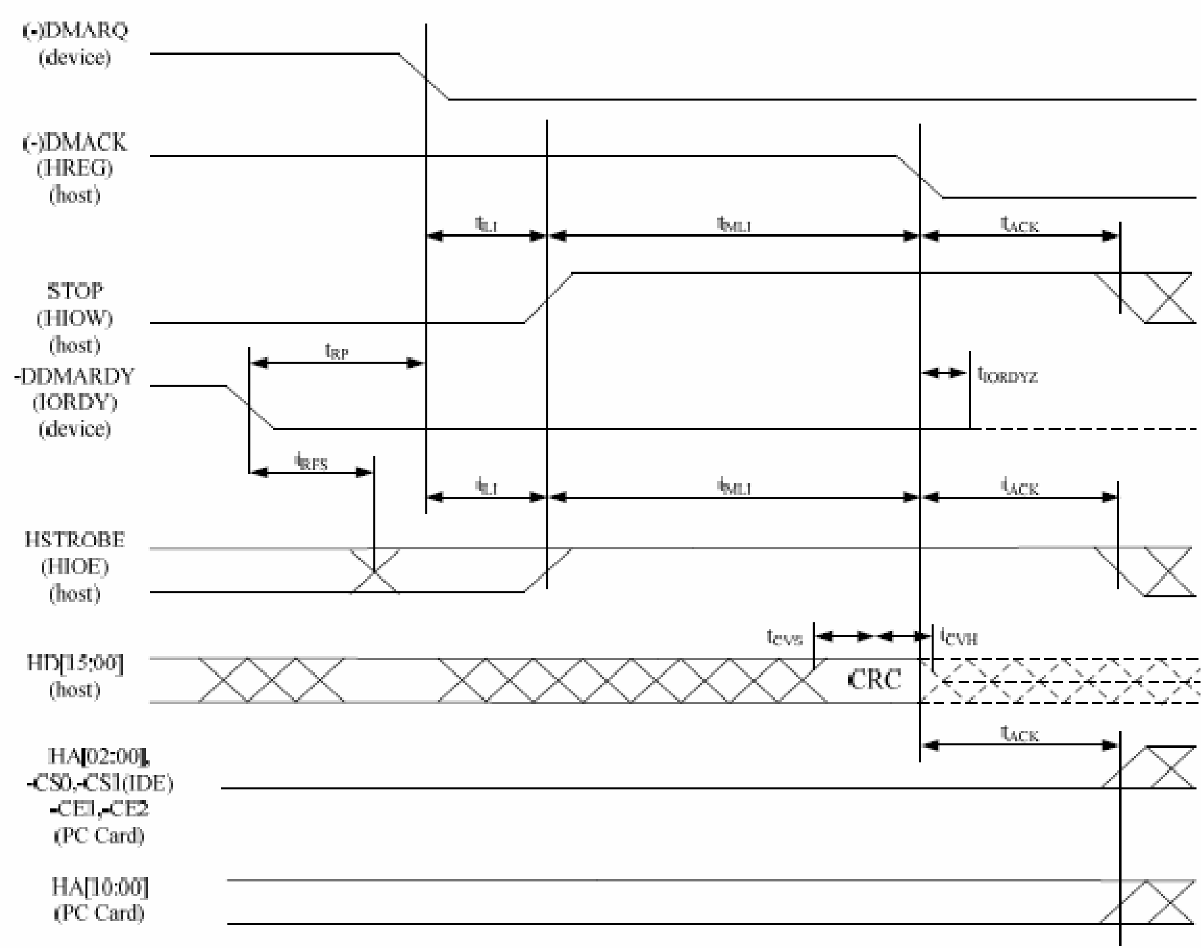


Figure 21: Ultra DMA Data-Out Burst Device Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[00:02], -CS0& -CS1 are True IDE mode signal definitions. HA[00:10], -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

4.2.23. Ultra DMA Data-Out Burst Host Termination Timing

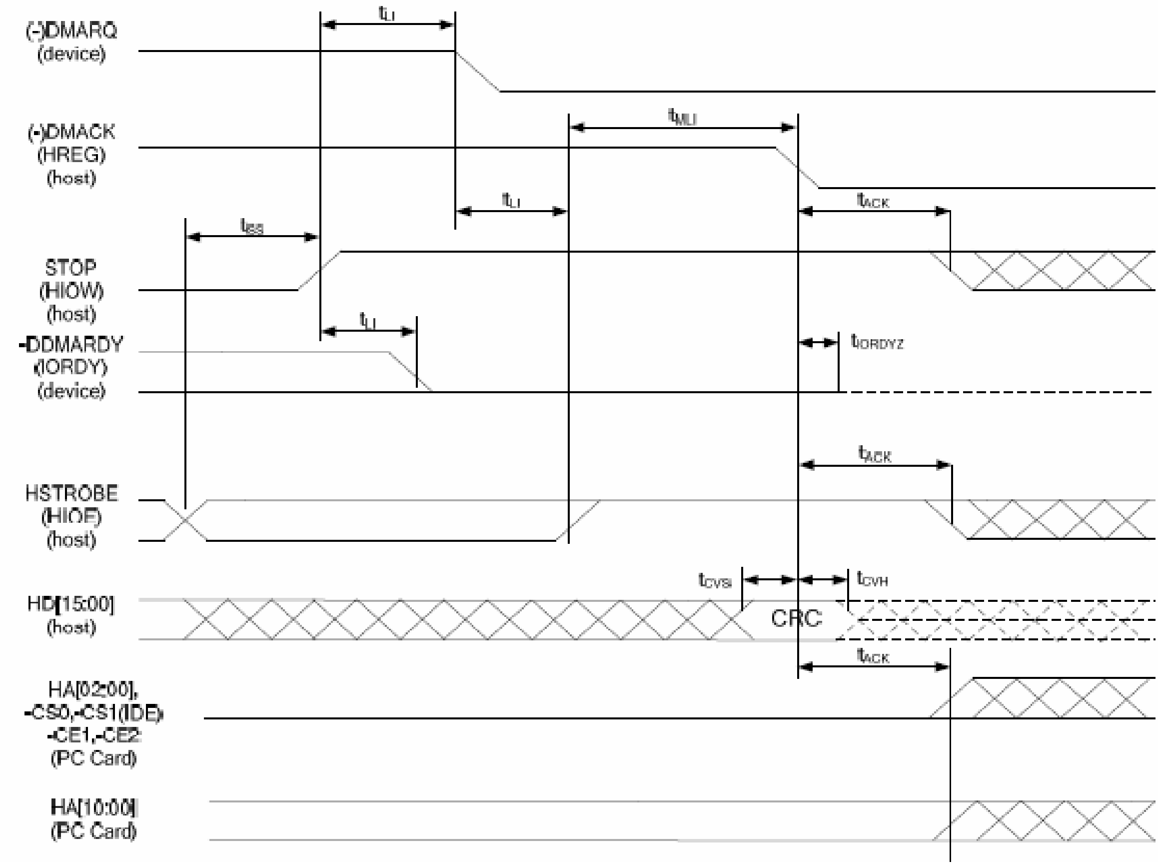


Figure 22: Ultra DMA Data-Out Burst Host Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[02:00], -CS0& -CS1 are True IDE mode signal definitions. HA[10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

5. *Interface Register Definition*

5.1. *Device Address*

This controller receives commands from the host only when it is the selected device by checking the DEV bit in the Device Register.

This interface is for the host to program and perform commands and return status.

Table 25: Device Address Commands

CS1–	CS0–	A2	A1	A0	DMACK–	DIOR– = L	DIOW– = L
1	0	0	0	0	X	Data register	Data register
1	1	X	X	X	0	DMA Data RD	DMA Data Write
1	0	0	0	1	X	Error register	Feature register
1	0	0	1	0	X	Sector Count register	Sector Count register
1	0	0	1	1	X	LBA Low register	LBA Low register
1	0	1	0	0	X	LBA Mid register	LBA Mid register
1	0	1	0	1	X	LBA High register	LBA High register
1	0	1	1	0	X	Device register	Device register
1	0	1	1	1	X	Status register	Command register
0	1	1	1	0	X	Alt. Status register	Device Control register

5.2. *I/O Register Descriptions*

The Command Block registers are used for the host to send commands to this controller or for this controller to post status. These registers include the LBA High, LBA Mid, LBA Low, Device, Sector Count, Command, Status, Features, Error and Data Registers. The Control Block register is used for device control and to post alternate status. These registers include Device Control and Alternate Status registers.
For the detail field/bit description of every register, please refer to the ATAPI-5 specification.

(4) Alternate Status Register
This register contains the same information as the Status register in the Command Block.

(5) Command Register
This register contains the command code being sent. This controller begins immediately to execute the command after receipt of the command

(6) DMA Data Port
This port is only accessed for the host DMA data transfers when DMACK– and DMARQ are asserted. The data is 16-bits in width.

(7) Data Register

This register is accessed for the host PIO data transfer only when DRQ is set to one and DMACK– is not asserted. The contents of this register are not valid while it is in the Sleep mode. This register is 16 bits wide.

(8) Device Register

This register is for the host to set bit 4, DEV, of this register to selects the device. Other bis in this register are command dependent.

(9) Device Control Register

This register allows the host to software reset attached devices and to enable or disable the assertion of the INTRQ signal by a selected device. When this register is written, the controller will respond to the write no matter the device is selected or not. And this controller will respond to the SRST bit when in the SLEEP mode.

(10)Error Register

At command completion of any command, the contents of this register are valid when the ERR bit is set to one in the Status register.

(11)Feature Register

This register is writing only, If this address is reading by the host, the content read by the host will be the Error register. The content of this register is command dependent.

(12)LBA High Register

This register contains the high order bits of logic block address and becomes a command parameter when Command register is written.

(13)LBA Low Register

This register contains the low order bits of logic block address and becomes a command parameter when Command register is written.

(14)LBA Mid Register

This register contains bit 15-8 of logic block address and becomes a command parameter when Command register is written.

(15)Sector Count Register

This register contains the numbers of sectors of data requested to be transferred on a read or write operation.

(16)Status Register

This register contains the device status. The contents of this register are updated to reflect the current state of the device.

6. *Software Specification*

6.1. *ATA Command Set*

The following table summarizes the commands supported by the controller.

Table 26: ATA Commands Supported

Item	Command	Code	FR	SC	SN	CY	DH	LBA	Controller Status	Note
1	Check Power Mode	E5 or 98h	–	–	–	–	Y	–	Support	
2	Execute Drive Diagnostic	90h	–	–	–	–	Y	–	Support	
3	Erase Sector	C0h	–	Y	Y	Y	Y	Y	Support	
4	Flush Cache	E7h	–	–	–	–	Y	–	NOT Support	#4
5	Format Track	50h	–	Y	–	Y	Y	Y	Support	
6	Identify Device	Ech	–	–	–	–	Y	–	Support	
7	Idle	E3h or 97h	–	Y	–	–	Y	–	Support	
8	Idle Immediate	E1h or 95h	–	–	–	–	Y	–	Support	
9	Initialize Drive Parameters	91h	–	Y	–	–	Y	–	Support	
10	Key Management Structure Read	B9 (Feature 0-127)	Y	Y	Y	Y	Y	–	NOT Support	#1
11	Key Management Read Keying Material	B9 (Feature 80)	Y	Y	Y	Y	Y	–	NOT Support	#1
12	Key Management Change Key Management Value	B9 (Feature 81)	Y	Y	Y	Y	Y	–	NOT Support	#1
13	NOP	00h	–	–	–	–	Y	–	Support	
14	Read Buffer	E4h	–	–	–	–	Y	–	Support	
15	Read DMA	C8h	–	Y	Y	Y	Y	Y	Support	
16	Read Long Sector	22h or 23h	–		Y	Y	Y	Y	NOT Support	#3
17	Read Multiple	C4h	–	Y	Y	Y	Y	Y	Support	
18	Read Sector(s)	20h or 21h	–	Y	Y	Y	Y	Y	Support	
19	Read Verify Sector(s)	40h or 41h	–	Y	Y	Y	Y	Y	Support	
20	Recalibrate	1Xh	–	–	–	–	Y	–	Support	
21	Request Sense	03h	–	–	–	–	Y	–	Support	
22	Security Disable Password	F6h	–	–	–	–	Y	–	NOT Support	#2, #5
23	Security Erase Prepare	F3h	–	–	–	–	Y	–	NOT Support	#2, #5
24	Security Erase Unit	F4h	–	–	–	–	Y	–	NOT Support	#2, #5
25	Security Freeze Lock	F5h	–	–	–	–	Y	–	NOT Support	#2, #5
26	Security Set Password	F1h	–	–	–	–	Y	–	NOT Support	#2, #5
27	Security Unlock	F2h	–	–	–	–	Y	–	NOT Support	#2, #5

28	Seek	7Xh	–	–	Y	Y	Y	Y	Support	
29	Set Feature	EFh	Y	–	–	–	Y	–	Support	
30	Set Multiple Mode	C6h	–	Y	–	–	Y	–	Support	
31	Set Sleep Mode	E6h or 99h	–	–	–	–	Y	–	Support	
32	Standby	E2 or 96h	–	–	–	–	Y	–	Support	
33	Standby Immediate	E0 or 94h	–	–	–	–	Y	–	Support	
34	Translate Sector	87h	–	Y	Y	Y	Y	Y	Support	
35	Wear Level	F5h	–	–	–	–	Y	–	Support	
36	Write Buffer	E8h	–	–	–	–	Y	–	Support	
37	Write DMA	CAh	–	Y	Y	Y	Y	Y	Support	
38	Write Long Sector	32h or 33h	–	–	Y	Y	Y	Y	Not Support	#3
39	Write Multiple	C5h	–	Y	Y	Y	Y	Y	Support	
40	Write Multiple w/o Erase	CDh	–	Y	Y	Y	Y	Y	Support	
41	Write Sector(s)	30h or 31h	–	Y	Y	Y	Y	Y	Support	
42	Write Sector(s) w/o Erase	38h	–	Y	Y	Y	Y	Y	Support	
43	Write Verify	3Ch	–	Y	Y	Y	Y	Y	Support	

Notes:

1) *These commands are optional, depending on the key Management scheme in use.*
2) *Use of this command is not recommended by CFA.*
3) *Use of this command is not recommended.*
4) *SM223 don't have cache.*
5) *Will support by firmware update, it will be available by September, 2010*
6) ***Definitions***

FR = Features Register
SC =Sector Count register (00H to FFH, 00H means 256 sectors) S
N = Sector Number register
CY = Cylinder Low/High register
DH = Head No. (0 to 15) of Drive/Head register
LBA = Logic Block Address Mode Support
– = Not used for the command
Y = Used for the command

6.2. *ATA Command Description*

(1) CFA Erase Sector(s) – C0h

This command pre-erases and conditions from 1 to 256 sectors in the Sector Count register. This command must be issued in advance of CFA Write without Erase or CFA Write Multiple without Erase command to increase the execution speed of the write operation.

(2) CFA Request Extended Error Code – 03h

This command requests extended error information for the previous command. The extended error code is returned to the host in the Error Register.

(3) CFA Translate Sector – 87h

This command allows the host a method of determining the exact times a user sector has been erased and programmed. This controller will respond with a 512-byte buffer of information containing the desired cylinder, head and sector, including its Logical Address.

(4) CFA Write Multiple w/o Erase – CDh

This command is similar to Write Multiple command with the exception that an implied erase before write operation is not performed.

(5) Write Sector(s) w/o Erase – 38h

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed.

(6) Check Power Mode – E5h

This command allows the host to determine the current power mode of the device. This command will not cause this controller to change power mode.

(7) Execute Device Diagnostic – 90h

This command causes the controller to perform the internal diagnostic tests.

(8) Identify Device – ECh

This command enables the host to receive parameter information from the device. The following table specifies each field in the data returned by Identify Device command.

Table 27: Identify Device Commands

Word address	F/V[1]	Description	Value
0	 F X F X	General configuration bit-significant information: 15 0 = ATA device 14-8 Reserved. 7 0 = the device is a fixed disk 6-0 Reserved.	**045Ah**
1	V	Number of logical cylinders	xxxxh[1]
2	V	Specific configuration	0000h
3	F	Number of logical heads	xxxxh
4 - 5	X	Reserved	xxxxh
6	F	Number of logical sectors per logical track	xxxxh
7 - 8	X	Reserved	xxxxh
9	X	Reserved	0000h
10 to 19	C	Serial number (20 ASCII characters)	aaaa[2]
20	X	Reserved	0001h
21 - 22	X	Reserved	0004h
23 - 26	F	Firmware revision (8 ASCII characters)	aaaa
27 - 46	C	Model number (40 ASCII characters)	aaaa
47	F F	15-8 80h 7-0 01h = Maximum number of sector on Read/Write Multiple command	8001h
48	F	Reserved	0000h
49	 F F F F F F F X	Capabilities 15-14 Reserved 13 0 = Standby timer is managed by this controller 12 Reserved 11 1 = IORDY supported. 10 1 = IORDY may be disabled. 9 1 = LBA mode addressing supported. 8 1 = DMA supported. 7 – 0 Reserved	0F00h
50	F	15- 0 0000h = the contents of word 50 is not valid.	0000h
51	F	Reserved.	0200h
52	X	Reserved	0000h
53	F F F	15- 3 Reserved. 2 1 = the field reported in word 88 are valid 1 1 = the field reported in word (70:64) are valid 0 1 = the field reported in word 54-58 are valid	0007h
54	V	Number of current logical cylinders	xxxxh
55	V	Number of current logical heads	xxxxh

56	V	Number of current logical sectors per track	xxxxh
57- 58	V	Current capacity in sectors	xxxxh
59	F V V	15- 9 Reserved 8 1 = multiple sector setting is valid 7- 0 xxh = current setting for number of sectors that is transferred per interrupt on R/W Multiple commands.	0101h
60 - 61	F	Total number of user addressable sectors	xxxxh
62	X	Reserved	0000h
63	F V F F F F	15-11 Reserved. 10- 8 Multiword DMA mode 2-0 selected. 7- 3 Reserved. 2 1 = Multiword DMA mode 2,1 and 0 are supported. 1 1 = Multiword DMA mode 1 and 0 are supported. 0 1 = Multiword DMA mode 0 is supported.	0407h
64	F C F	15- 2 Reserved 1 1 = PIO mode 4 is supported. 0 1 = PIO mode 3 is supported.	0003h
65	F	15- 0 0078h = minimum Multiword DMA transfer cycle time = 120 nano seconds.	0078h
66	F	15- 0 0078h = recommended Multiword DMA transfer cycle time = 120 nano seconds.	0078h
67	F	15- 0 0078h = minimum PIO transfer cycle time without flow control = 120 nano seconds.	0078h
68	F	15- 0 0078h = minimum PIO transfer cycle time with IORDY flow control = 120 nano seconds.	0078h
69 - 79	F	Reserved	0000h
80	F	15- 0 0000h = Major version number is not reported.	0000h
81	F	15- 0 0000h = Minor version number is not reported.	0000h
82	 X F F F X F F F F F F F F F F	Command set supported. 15 Reserved. 14 1 = NOP command supported. 13 1 = READ BUFFER command supported. 12 1 = WRITE BUFFER command supported. 11 Reserved. 10 1 = Host Protected Area feature set supported. 9 1 = DEVICE RESET command supported. 8 1 = SERVICE interrupt supported. 7 1 = release interrupt supported. 6 1 = look-ahead supported. 5 1 = write cache supported. 4 1 = Shall be cleared to zero. 3 1 = mandatory power management feature set supported. 2 1 = Removable Media feature set supported. 1 1 = Security Mode feature set supported.	3000h

	F	0 1 = SMART feature set supported.	
83 - 84	F	15- 0 0000h = features/command sets supported are not indicated.	0000h
85		Command set/ feature enabled.	3000h
	X	15 Reserved.	
	F	14 1 = NOP command enabled.	
	F	13 1 = READ BUFFER command enabled.	
	F	12 1 = WRITE BUFFER command enabled.	
	X	11 Reserved.	
	V	10 1 = Host Protected Area feature set enabled.	
	F	9 1 = DEVICE RESET command enabled.	
	V	8 1 = SERVICE interrupt enabled.	
	V	7 1 = release interrupt enabled.	
	V	6 1 = look-ahead enabled.	
	V	5 1 = write cache enabled.	
	F	4 1 = Shall be cleared to zero.	
	F	3 1 = power management feature set enabled.	
	F	2 1 = Removable Media feature set enabled.	
	V	1 1 = Security Mode feature set enabled.	
	V	0 1 = SMART feature set enabled.	
85 - 87	F	15- 0 0000h = features/command sets enabled are not indicated.	0000h
88	F	15-13 Reserved.	001Fh
	V	12 1 = Ultra DMA mode 4 is selected	
	V	11 1 = Ultra DMA mode 3 is selected.	
	V	10 1 = Ultra DMA mode 2 is selected	
	V	9 1 = Ultra DMA mode 1 is selected.	
	V	8 1 = Ultra DMA mode 0 is selected.	
	F	7- 5 Reserved	
	C	4 1 = Ultra DMA mode 4 and below are supported.	
	F	3 1 = Ultra DMA mode 3 and below are supported.	
	C	2 1 = Ultra DMA mode 2 and below are supported.	
	F	1 1 = Ultra DMA mode 1 and below are supported.	
	C	0 1 = Ultra DMA mode 0 is supported.	
89	F	Time required for security erase unit completion. 15- 0 0000h = value not specified.	0000h
90	F	Time required for Enhanced security erase unit completion. 15- 0 0000h = value not specified.	0000h
91	V	Current advanced power management value 15- 0 0000h = value not specified.	0000h
92	V	Master Password Revision Code.	0000h
93	V	Reserved.	0000h
94	V	15- 0 0000h = Automatic Acoustic Management feature set is not supported.	0000h
95 - 99	F	Reserved	0000h
100 - 103	V	The 48-bit Address feature set is not supported.	0000h

104 - 126	F	Reserved.	0000h
127	F F	Removable Media Status Notification feature set support 15 - 2 Reserved. 1- 0 00b = This feature set is not supported.	0000h
128	F F	Security Status 15 - 9 Reserved. 8 - 0 000h = Security Mode Feature set is no supported.	0000h
129 - 159	X	Reserved	0000h
160	F	15- 0 0000h = the CFA Power Mode 1 is not supported.	0000h
161 - 162	F	Reserved.	0000h
163	F	Reserved.	0000h
164	F	Reserved.	001Bh
165 - 175	F	Reserved.	aaaa
176 - 205	F	Current media serial number is not indicated.	0000h
206 - 254	F	Reserved.	0000h
255	F	Integrity word 15- 8 Checksum 7 -0 Signature.	0000h

Notes:

(1) F/V = Fixed/Variable content
F = the content of the word is fixed and does not change.
V = the content of the word is variable and may be changed depending on the state of the device, commands executed.
X = the content of the word may be fixed or variable.
C = vendor specific data which can be customized before device shipping.

(2) aaaa indicates an ASCII vendor string; x indicates a numeric nibble value.

(9) Idle – E3h

This command allows the host to place the device in the Idle mode and also set the Standby timer.

(10)Idle Immediate – E1h

This command allows the host to immediately place the device in the Idle mode.

(11)Initialize Device Parameters – 91h

This command enables the host to set the number of sectors per track and number of heads per cylinder.

(12)NOP – 00h

This controller will respond with command abort upon receipt of the NOP command.

(13)Read Buffer – E4h

This command enables the host to read the current contents of the device's sector buffer.

(14)Read DMA – C8h

This command allows the host to read data using the DMA data transfer protocol.

(15)Read Multiple – C4h

This command reads the number of sectors specified in the Sector Count register. The number of sectors per block is defined by the content of word 59 in the Identify Device response. A successful Set Multiple Mode command has to precede this command.

(16)Read Sector(s) – 20h

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 will be treated as 256 sectors. The transfer begins at the sector specified in the LBA Low, LBA Mid, LBA High and Device registers.

(17)Read Verify Sector(s) – 40h

This command is identical to Read Sector(s) command, except that DRQ is never set and no data is transferred to the host.

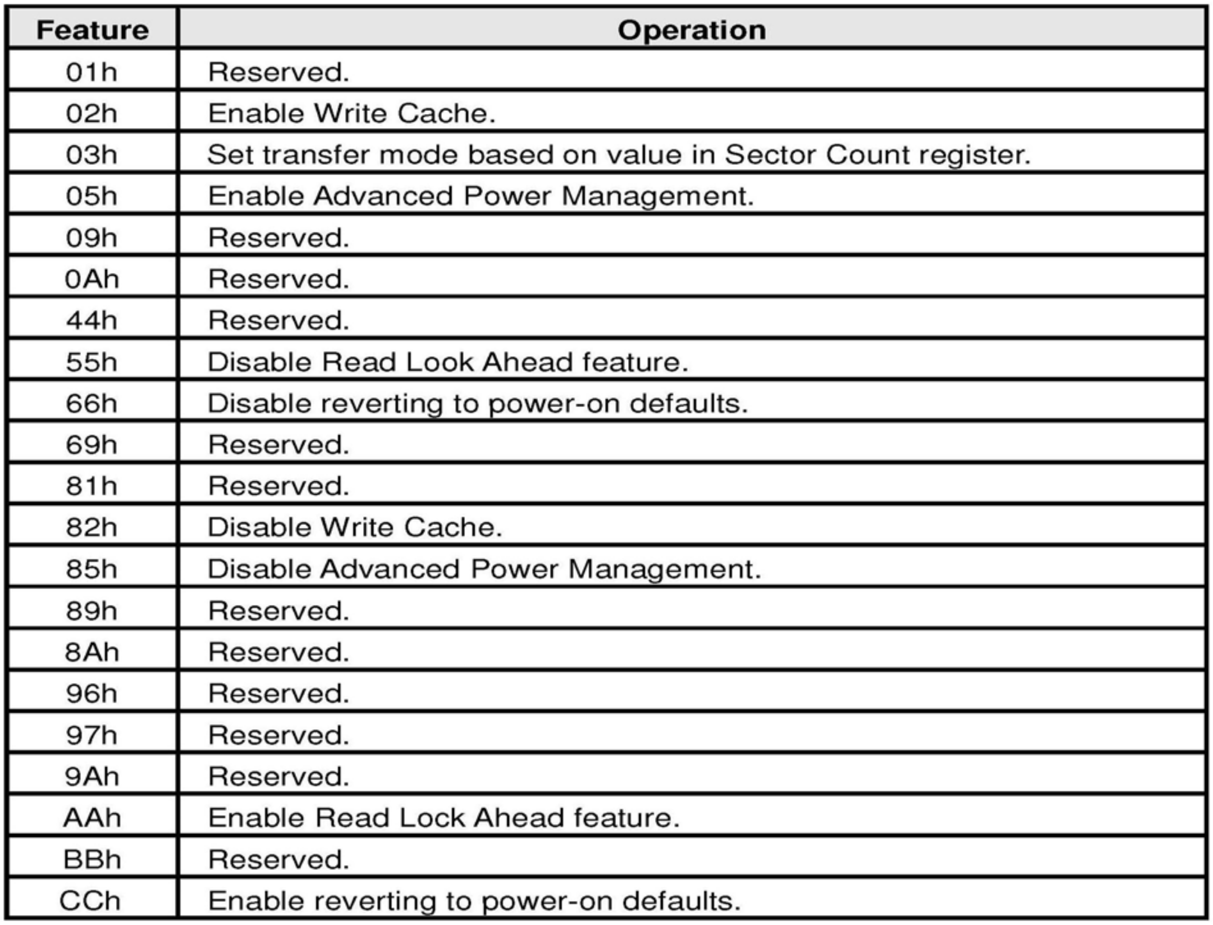
(18)Seek – 70h

This command allows the host to provide advanced notification that particular data may be requested by the host in a subsequent command.

(19)Set Features – EFh

This command is used by the host to establish parameters that affect the execution of certain features. The following table defines all features that are supported by this controller. If any subcommand input value is not supported or is invalid, this controller will return command aborted.

Table 28: Set Feature Commands



Feature	Operation
01h	Reserved.
02h	Enable Write Cache.
03h	Set transfer mode based on value in Sector Count register.
05h	Enable Advanced Power Management.
09h	Reserved.
0Ah	Reserved.
44h	Reserved.
55h	Disable Read Look Ahead feature.
66h	Disable reverting to power-on defaults.
69h	Reserved.
81h	Reserved.
82h	Disable Write Cache.
85h	Disable Advanced Power Management.
89h	Reserved.
8Ah	Reserved.
96h	Reserved.
97h	Reserved.
9Ah	Reserved.
AAh	Enable Read Lock Ahead feature.
BBh	Reserved.
CCh	Enable reverting to power-on defaults.

(20)Set Multiple Mode – C6h

Upon receipt of this command, the controller will perform Read and Write Multiple operations and establishes the block count for these commands. This controller will set BSY to 1 and checks the Sector Register for the number of sectors per block.

(21)Sleep – E6h

Upon receipt of this command, the controller will set BSY and enter Sleep mode, clear BSY and generate an interrupt.

(22)Standby – E2h

This command will cause the device to enter Standby mode. The value in the Sector Count register is used to determine the time programmed into the Standby timer.

(23)Standby Immediate – E0h or 94h

This command will cause the device to immediately enter Standby mode.

(24)Write Buffer – E8h

This command allows the host to overwrite contents of a sector buffer with any data pattern desired.

(25)Write DMA – CAh

This command allows the host to write data using the DMA data transfer protocol.

(26)Write Multiple – C5h

This command is similar to the Write Sector(s) command. Interrupts are not presented on each sector but on the transfer of a block that contains the number of sectors defined by Set Multiple.

(27)Write Sector(s) – 30h

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 will be treated as 256 sectors. This controller will interrupt for each DRQ block transferred.

6.3. *ID Table Information*

Table 29: Identify Data Information

Word Address	Default value	Total Bytes	Data Field Type information
0	045Ah	2	General configuration
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0240h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	XXXXh	20	Serial number in ASCII (Right Justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands
23-26	XXXXh	8	Firmware revision in ASCII. Big Endean Byte Order in Word
27-46	XXXXh	40	Model number in ASCII (Left Justified) Big Endean Byte Order in Word
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0300h	2	Capabilities
50	0000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0007h	2	Field validity

Word Address	Default value	Total Bytes	Data Field Type information
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word57=LSW , Word58=MSW)
59	0101h	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0407h	2	Multiword DMA transfer. In PCMCIA mode this value shall be oh
64	0003h	2	Advanced PIO modes supported
65	0078h	2	Minimum Multiword DMA transfer cycle time per word.
66	0078h	2	Recommended Multiword DMA transfer cycle time.
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	20	Reserved
80	0010h	2	Major version number
81	0000h	2	Minor version number
82	7008h	2	Command sets supported 0
83	400Ch	2	Command sets supported 1
84	4002h	2	Command sets supported 2
85	0001h	2	Command sets Enable 0
86	0000h	2	Command sets Enable 1
87	0002h	2	Command sets Enable 2
88	001Fh	2	True IDE Ultra DMA Mode Supported and Selected (UDMA0~4)
89	0000h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management level value
92-127	0000h	72	Reserved
128	0000h	2	Security status
129-159	0000h	64	vendor unique bytes
160	81F4h	2	Power requirement description
161	0000h	2	Reserved for assignment by the CFA
162	0000h	2	Key management schemes supported
163	0492h	2	CF Advanced True IDE Timing Mode Capability and Setting
164	001Bh	2	CF Advanced PCMCIA I/O and Memory Timing Mode Capability and set
165-175	0000h	22	80ns cycle in memory and IO mode
176-255	0000h	140	Reserved for assignment by the CFA

Notes:

Word 1: Default number of cylinders .

Word 3: Default number of heads .

Word 6: Default number of sectors per track .

Word 10~19: Serial number in ASCII .
Word 23~26: Firmware revision in ASCII.
Word 27~26: Model number in ASCII

Appendix A. Ordering Information

Part Number List:

◆ **Standard Casing Industrial CF Cards –**

Capacity	0° C~ 70° C	-40° C~ +85° C
16MB		
32MB		
64MB		
128MB		
256MB		
512MB		
1GB		
2GB		
4GB		
8GB		
16GB		
32GB		

◆ **Rugged Metal Casing Industrial CF Cards –**

Capacity	0° C~ 70° C	-40° C~ +85° C
16MB		
32MB		
64MB		
128MB		
256MB		
512MB		
1GB		
2GB		
4GB		
8GB		
16GB		
32GB		

Remarks:

1) The optional data-transfer modes and disk types are:

1. *PF: optional as PIO-4 mode / Fixed disk type*
2. *PR: optional as PIO-4 mode / Removable disk type*
3. *PA: optional as PIO-4 mode / Fixed disk & Removable disk type Auto-detection*
4. ***UF: defaulted as UDMA-4 mode / Fixed disk type***
5. *UR: optional as UDMA-4 mode / Removable disk type*
6. *UA: optional as UDMA-4 mode / Fixed disk & Removable disk type Auto-detection*
7. *AF: optional as UDMA & PIO mode auto-detection / Fixed disk type*
8. *AR: optional as UDMA & PIO mode Auto-detection / Removable disk type*
9. *AA: optional as UDMA & PIO mode Auto-detection / Fixed disk & Removable disk type Auto-detection*