QL16x24B
pASIC® 1 Family
Very-High-Speed CMOS FPGA

Rev C

pASIC HIGHLIGHTS

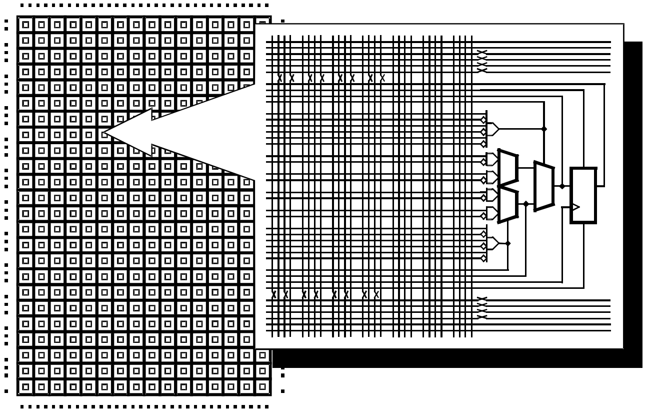
- **Very High Speed** – ViaLink® metal-to-metal programmable–via antifuse technology, allows counter speeds over 150 MHz and logic cell delays of under 2 ns.
- **High Usable Density** – A 16-by-24 array of 384 logic cells provides 4,000 usable ASIC gates (7,000 PLD gates) in 84-pin PLCC, 100-pin and 144-pin TQFP, 144-pin CPGA and 160-pin CQFP packages.

…4,000 usable ASIC gates, 122 I/O pins

- **Low-Power, High-Output Drive** – Standby current typically 2 mA. A 16-bit counter operating at 100 MHz consumes less than 50 mA. Minimum IOL of 12 mA and IOH of 8 mA
- **Low-Cost, Easy-to-Use Design Tools** – Designs entered and simulated using QuickLogic's new Quick*Works*® development environment, or with third-party CAE tools including Viewlogic, Synopsys, Mentor, Cadence and Veribest. Fast, fully automatic place and route on PC and workstation platforms using QuickLogic software.

QL16x24B Block Diagram

384 Logic Cells



▪ = Up to 114 prog. I/O cells, 6 Input high-drive cells, 2 Input/Clk (high-drive) cells

QUICKLOGIC

PRODUCT SUMMARY

The QL16x24B is a member of the pASIC 1 Family of very-high-speed CMOS user-programmable ASIC devices. The 384 logic cell field-programmable gate array (FPGA) offers 4,000 usable ASIC gates (equivalent to 7,000 PLD gates) of high-performance general-purpose logic in 84-pin PLCC, 100-pin and 144-pin TQFP, 144-pin CPGA, and 160-pin CQFP.

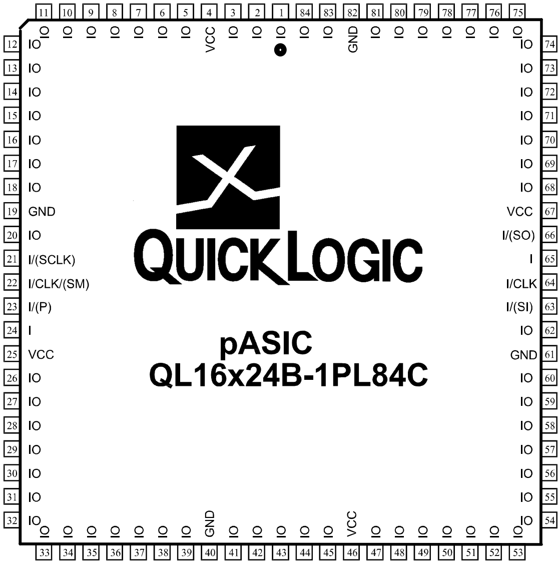
Low-impedance, metal-to-metal, ViaLink interconnect technology provides nonvolatile custom logic capable of operating above 150 MHz. Logic cell delays under 2 ns, combined with input delays of under 1.5 ns and output delays under 3 ns, permit high-density programmable devices to be used with today's fastest microprocessors and DSPs.

Designs can be entered using QuickLogic's Quick*Works* Toolkit or most populart third-party CAE tools. Quick*Works* combines Verilog/VHDL design entry and simulation tools with device-specific place & route and programming software. Ample on-chip routing channels allow fast, fully automatic place and route of designs using up to 100% of the logic and I/O cells, while maintaining fixed pin-outs.

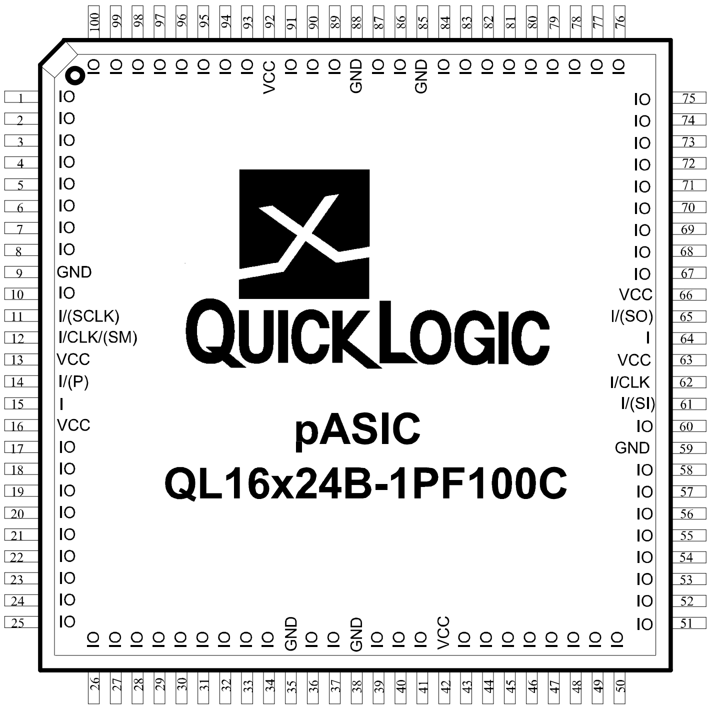
FEATURES

- Total of 122 I/O pins
  - 114 Bidirectional Input/Output pins
  - 6 Dedicated Input/High-Drive pins
  - 2 Clock/Dedicated input pins with fanout-independent, low-skew clock networks
- Input + logic cell + output delays under 6 ns
- Chip-to-chip operating frequencies up to 110 MHz
- Internal state machine frequencies up to 150 MHz
- Clock skew < 0.5 ns
- Input hysteresis provides high noise immunity
- Built-in scan path permits 100% factory testing of logic and I/O cells and functional testing with Automatic Test Vector Generation (ATVG) software after programming
- Packages are 84-pin PLCC, 100-pin and 144-pin TQFP, 144-pin CPGA, and 160-pin CQFP
- 84-pin PLCC compatible with QL12x16B
- 100-pin TQFP compatible with QL8x12B and QL12x16B
- 144-pin TQFP compatible with QL24x32B
- 0.65µ CMOS process with ViaLink programming technology

Pinout Diagram 84-pin PLCC



Pinout Diagram 100-pin TQFP



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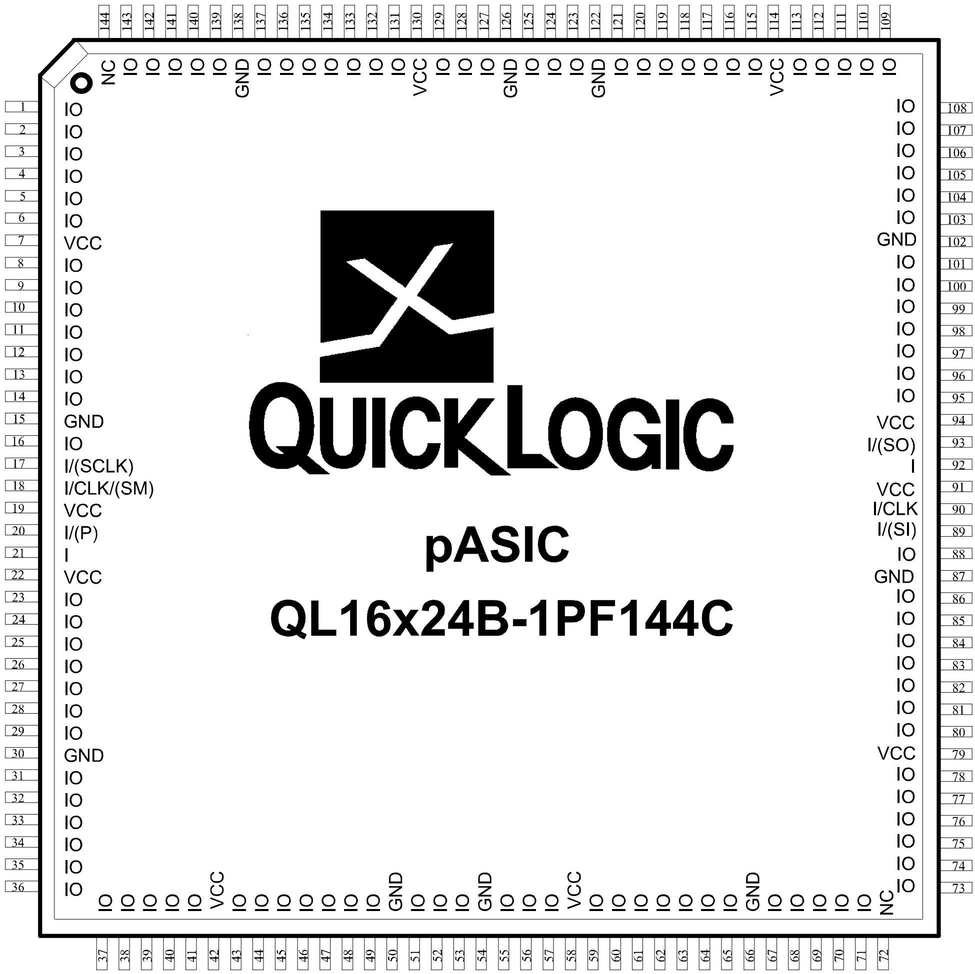
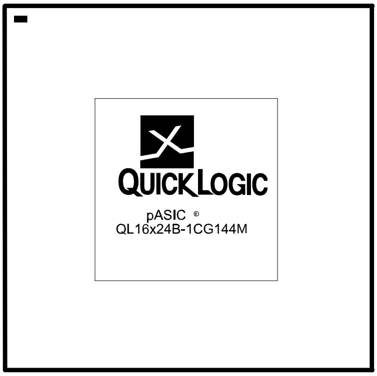
Pinout Diagram
144-pin TQFP

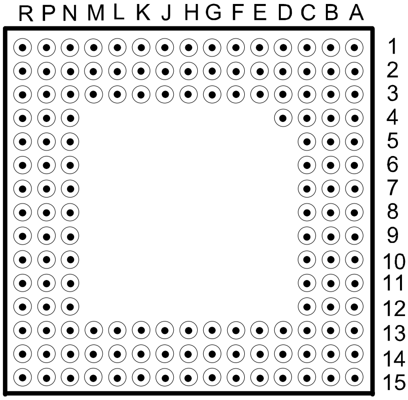


Pinout Diagram
144-pin CPGA

TOP VIEW



BOTTOM VIEW



CPGA 144 Function/Connector Table

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
A2	IO	B15	IO	R14	IO	P1	IO
B3	IO	C14	IO	P13	IO	N2	IO
C4	IO	D13	IO	N12	IO	M3	IO
A3	IO	C15	IO	R13	IO	N1	IO
B4	IO	D14	IO	P12	IO	M2	IO
A4	IO	E13	VCC	R12	IO	L3	VCC
C3	VCC	D15	IO	N13	VCC	M1	IO
B5	IO	E14	IO	P11	IO	L2	IO
A5	IO	E15	IO	R11	IO	L1	IO
C6	IO	F13	IO	N10	IO	K3	IO
B6	IO	F14	IO	P10	IO	K2	IO
A6	IO	F15	IO	R10	IO	K1	IO
A7	IO	G15	IO	R9	IO	J1	IO
B7	IO	C13	GND	P9	IO	N3	GND
C5	GND	G14	IO	N11	GND	J2	IO
A8	IO	H15	IO	R8	IO	H1	IO
B8	I/(SCLK)	H14	IO	P8	I/(SI)	H2	IO
C8	I/CLK/(SM)	G13	GND	N8	I/CLK	J3	GND
C7	VCC	H13	IO	N9	VCC	H3	IO
A9	I/(P)	J15	IO	R7	I	G1	IO
B9	I	J14	IO	P7	I/(SO)	G2	IO
C11	VCC	J13	VCC	N5	VCC	G3	VCC
A10	IO	K15	IO	R6	IO	F1	IO
A11	IO	L15	IO	R5	IO	E1	IO
B10	IO	K14	IO	P6	IO	F2	IO
A12	IO	M15	IO	R4	IO	D1	IO
B11	IO	L14	IO	P5	IO	E2	IO
C10	IO	K13	IO	N6	IO	F3	IO
A13	IO	N15	IO	R3	IO	C1	IO
C9	GND	L13	GND	N7	GND	E3	GND
B12	IO	M14	IO	P4	IO	D2	IO
A14	IO	P15	IO	R2	IO	B1	IO
B13	IO	N14	IO	P3	IO	C2	IO
C12	IO	M13	IO	N4	IO	D3	IO
A15	IO	R15	IO	R1	IO	A1	IO
B14	IO	P14	nc	P2	IO	B2	nc

Pinout Daigram
160-pin CQFP

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pASIC 1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... −0.5 to 7.0V
Input Voltage .... −0.5 to VCC +0.5V
ESD Pad Protection .... ±2000V
DC Input Current .... ±20 mA
Latch-up Immunity .... ±200 mA

Storage Temperature ....−65°C to + 150°C
Lead Temperature ....300°C

OPERATING RANGE

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
VCC	Supply Voltage		4.5	5.5	4.5	5.5	4.75	5.25	V
TA	Ambient Temperature		-55		-40	85	0	70	°C
TC	Case Temperature			125					°C
K	Delay Factor	-X Speed Grade			0.4	2.75	0.46	2.55	
		-0 Speed Grade	0.39	1.82	0.4	1.67	0.46	1.55	
		-1 Speed Grade	0.39	1.56	0.4	1.43	0.46	1.33	
		-2 Speed Grade			0.4	1.35	0.46	1.25	

DC CHARACTERISTICS over operating range

Symbol	Parameter	Conditions	Min	Max	Unit
VIH	Input HIGH Voltage		2.0		V
VIL	Input LOW Voltage			0.8	V
VOH	Output HIGH Voltage	IOH = -4 mA	3.7		V
		IOH = -8 mA	2.4		V
		IOH = -10 μA	VCC-0.1		V
VOL	Output LOW Voltage	IOL = 12 mA*		0.4	V
		IOL = 10 μA		0.1	V
II	Input Leakage Current	VI = VCC or GND	-10	10	μA
IOZ	3-State Output Leakage Current	VI = VCC or GND	-10	10	μA
CI	Input Capacitance [1]			10	pF
IOS	Output Short Circuit Current [2]	VO = GND	-10	-80	mA
		VO = VCC	30	140	mA
ICC	D.C. Supply Current [3]	VI, VIO = VCC or GND		10	mA

*IOL = 12 mA for commercial range only. IOL = 8 mA for the industrial and military ranges.

Notes:

[1] Capacitance is sample tested only. CI = 20 pF max on I/(SI).
[2] Only one output at a time. Duration should not exceed 30 seconds.
[3] Commercial temperature grade only. Maximum Icc for industrial grade is 15mA and for military grade is 20 mA. For AC conditions use the formula described in the Section 9 — Power vs Operating Frequency.
[4] Stated timing for worst case Propagation Delay over process variation at VCC = 5.0V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.
[5] These limits are derived from a representative selection of the slowest paths through the pASIC logic cell ***including net delays***. Worst case delay values for specific paths should be determined from timing analysis of your particular design .

AC CHARACTERISTICS at VCC = 5V, TA = 25°C (K = 1.00)

Logic Cell

Symbol	Parameter	Propagation Delays (ns)				
		Fanout				
		1	2	3	4	8
tPD	Combinatorial Delay [5]	1.7	2.2	2.6	3.2	5.3
tSU	Setup Time [5]	2.1	2.1	2.1	2.1	2.1
tH	Hold Time	0.0	0.0	0.0	0.0	0.0
tCLK	Clock to Q Delay	1.0	1.5	1.9	2.6	4.7
tCWHI	Clock High Time	2.0	2.0	2.0	2.0	2.0
tCWLO	Clock Low Time	2.0	2.0	2.0	2.0	2.0
tSET	Set Delay	1.7	2.2	2.6	3.2	5.3
tRESET	Reset Delay	1.5	1.9	2.2	2.7	4.4
tSW	Set Width	1.9	1.9	1.9	1.9	1.9
tRW	Reset Width	1.8	1.8	1.8	1.8	1.8

Input Cells

Symbol	Parameter	Propagation Delays (ns) [4]					
		1	2	3	4	6	8
tIN	High Drive Input Delay [6]	2.8	2.9	3.0	3.1	4.0	5.3
tINI	High Drive Input, Inverting Delay [6]	3.0	3.1	3.2	3.3	4.1	5.7
tIO	Input Delay (bidirectional pad)	1.4	1.9	2.2	2.9	4.7	6.5
tGCK	Clock Buffer Delay [7]	2.7	2.8	2.9	3.0	3.1	3.3
tGCKHI	Clock Buffer Min High [7]	2.0	2.0	2.0	2.0	2.0	2.0
tGCKLO	Clock Buffer Min Low [7]	2.0	2.0	2.0	2.0	2.0	2.0

Output Cell

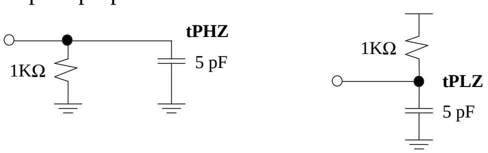
Symbol	Parameter	Propagation Delays (ns) [4]				
		Output Load Capacitance (pF)				
		30	50	75	100	150
tOUTLH	Output Delay Low to High	2.7	3.4	4.2	5.0	6.7
tOUTHL	Output Delay High to Low	2.8	3.7	4.7	5.6	7.6
tPZH	Output Delay Tri-state to High	4.0	4.9	6.1	7.3	9.7
tPZL	Output Delay Tri-state to Low	3.6	4.2	5.0	5.8	7.3
tPHZ	Output Delay High to Tri-state [8]	2.9				
tPLZ	Output Delay Low to Tri-state [8]	3.3				

Notes:

[6] See High Drive Buffer Table for more information.

[7] Clock buffer fanout refers to the maximum number of flip flops per half column. The number of half columns used does not affect clock buffer delay.

[8] The following loads are used for tPXZ:



High Drive Buffer

Symbol	Parameter	Clock Drivers Wired Together	Propagation Delays (ns) [4] Fanout				
			12	24	48	72	96
tIN	High Drive Input Delay	1	5.3	6.7			
		2		4.5	6.6		
		3			5.3	6.2	7.2
		4				5.4	6.2
tINI	High Drive Input, Inverting Delay	1	5.7	7.2			
		2		4.6	6.8		
		3			5.5	6.4	7.4
		4				5.6	6.4

AC Performance

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified in the Delay Factor table (Operating Range). The effects of voltage and temperature variation are illustrated in the graphs on page 4-47, K Factor versus Voltage and Temperature. The pASIC Development Tools incorporate data sheet AC Characteristics into the QDIF database for pre-place-and-route timing analysis. The SpDE Delay Modeler extracts specific timing parameters for precise path analysis or simulation results following place and route.

ORDERING INFORMATION

QL 16x24B - 1 PF144 C

QuickLogic pASIC device

pASIC device part number
B = 0.65 micron CMOS

Speed Grade
X = quick
0 = fast
1 = faster
2 = fastest

Package Code
PL84 = 84-pin PLCC
PF100 = 100-pin TQFP
PF144 = 144-pin TQFP
CG144 = 144-pin CPGA
CF160 = 160-pin CQFP

Operating Range
C = Commercial
I = Industrial
M = Military
M/883C = MIL STD 883