

Dual N-Ch Fast Switching MOSFETs

General Description

The QM3807M6 is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent R_{DS(on)} and gate charge for most of the synchronous buck converter applications.

The QM3807M6 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		Die1	Die2	
V _{DS}	Drain-Source Voltage	30	30	V
V _{GS}	Gate-Source Voltage	±20	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	57	83	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	36	52	A
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	12	17.3	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	9.6	14	A
I _{DM}	Pulsed Drain Current ²	130	170	A
EAS	Single Pulse Avalanche Energy ³	130	317	mJ
I _{AS}	Avalanche Current	34	53.8	A
P _D @T _C =25°C	Total Power Dissipation ⁴	46	46	W
P _D @T _A =25°C	Total Power Dissipation ⁴	2	2	W
T _{STG}	Storage Temperature Range	-55 to 150	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	62	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	2.7	°C/W

Product Summary

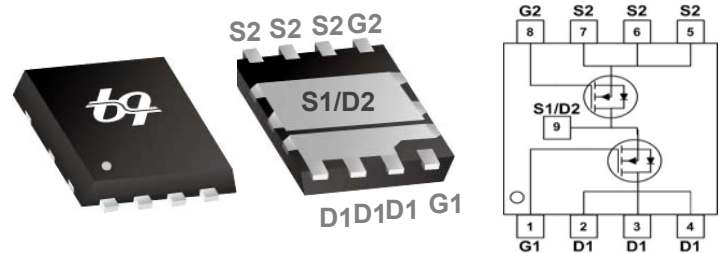


BVDSS	R _{DS(on)}	ID
30V	9mΩ	57A
30V	4mΩ	83A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- CCFL Back-light Inverter

PRPAK5X6 Pin Configuration



Die1 N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	35	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.024	---	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=30A$	---	7.2	9	m Ω
		$V_{GS}=4.5V, I_D=15A$	---	10.5	13.5	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.5	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-3.5	---	mV/ $^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=30A$	---	42	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.45	2.4	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=15A$	---	10.6	14.8	nC
Q_{gs}	Gate-Source Charge		---	4.2	5.9	
Q_{gd}	Gate-Drain Charge		---	4.0	5.6	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega, I_D=15A$	---	6.4	12.8	ns
T_r	Rise Time		---	70.6	127	
$T_{d(off)}$	Turn-Off Delay Time		---	22.4	45	
T_f	Fall Time		---	8.0	16	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	1127	1578	μF
C_{oss}	Output Capacitance		---	194	272	
C_{riss}	Reverse Transfer Capacitance		---	77	108	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	$V_{DD}=25V, L=0.1\text{mH}, I_{AS}=20A$	45	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,6}	$V_G=V_D=0V$, Force Current	---	---	57	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	130	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=30A, di/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	12	---	nS
Q_{rr}	Reverse Recovery Charge		---	3.7	---	nC

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating. The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=34A$
- The power dissipation is limited by 150°C junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Die2 N-Channel Electrical Characteristics ($T_J=25\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to $25\text{ }^\circ\text{C}$, $I_D=1mA$	---	0.0213	---	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=30A$	---	3.4	4	m Ω
		$V_{GS}=4.5V, I_D=15A$	---	5.2	6	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.5	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.73	---	mV/ $^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25\text{ }^\circ\text{C}$	---	---	1	μA
		$V_{DS}=24V, V_{GS}=0V, T_J=55\text{ }^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=30A$	---	26.5	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	1.4	2.3	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=15A$	---	31.6	44	nC
Q_{gs}	Gate-Source Charge		---	8.6	12	
Q_{gd}	Gate-Drain Charge		---	11.7	16.4	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega, I_D=15A$	---	9	18	ns
T_r	Rise Time		---	19	34	
$T_{d(off)}$	Turn-Off Delay Time		---	58	116	
T_f	Fall Time		---	15.2	30	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	---	3075	4305	pF
C_{oss}	Output Capacitance		---	400	560	
C_{riss}	Reverse Transfer Capacitance		---	315	440	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	$V_{DD}=25V, L=0.1mH, I_{AS}=30A$	98	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,6}	$V_G=V_D=0V$, Force Current	---	---	83	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	170	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25\text{ }^\circ\text{C}$	---	---	1	V
t_{rr}	Reverse Recovery Time	$I_F=30A, di/dt=100A/\mu s$,	---	18	---	nS
Q_{rr}	Reverse Recovery Charge	$T_J=25\text{ }^\circ\text{C}$	---	8	---	nC

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating. The test condition is $V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=53.8A$
- The power dissipation is limited by $150\text{ }^\circ\text{C}$ junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Dual N-Ch Fast Switching MOSFETs

N-Channel Typical Characteristics (Die1)

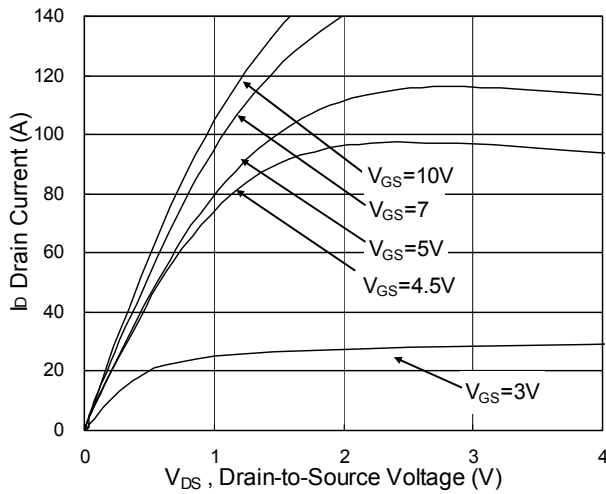


Fig.1 Typical Output Characteristics

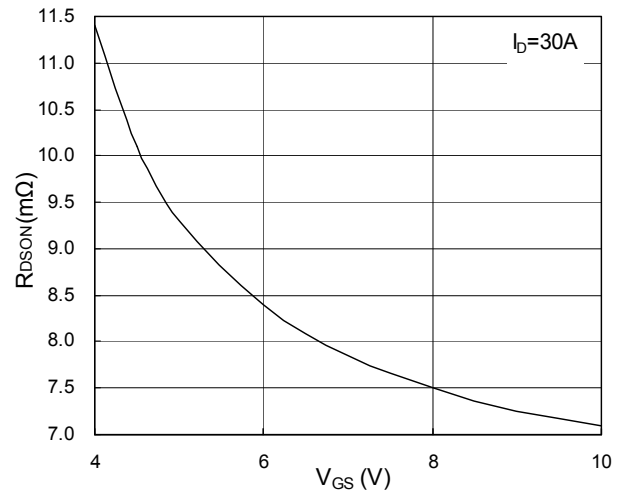


Fig.2 On-Resistance vs. Gate-Source

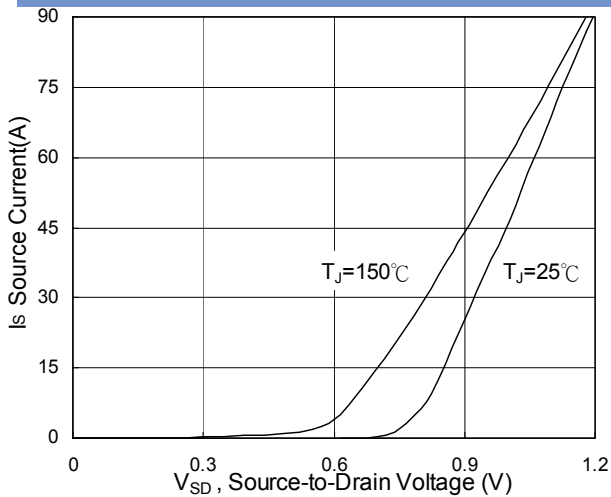


Fig.3 Forward Characteristics of Reverse

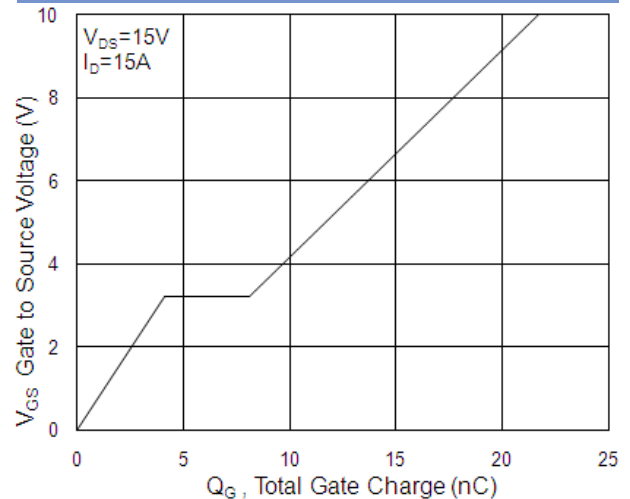


Fig.4 Gate-Charge Characteristics

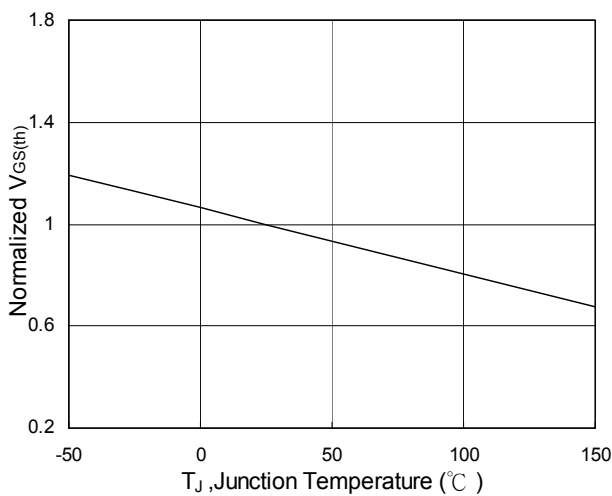


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

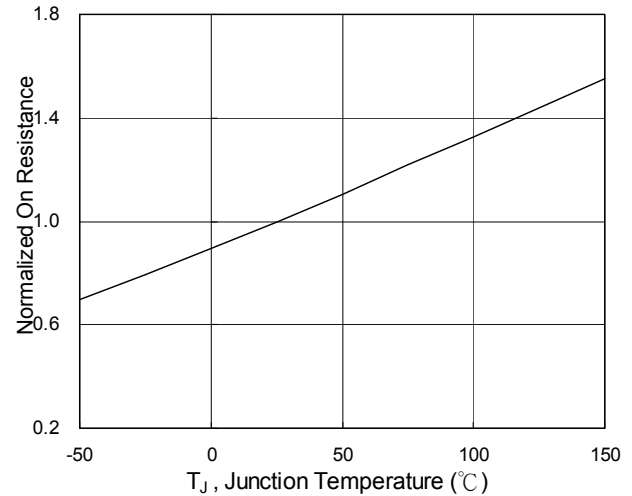


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

Dual N-Ch Fast Switching MOSFETs

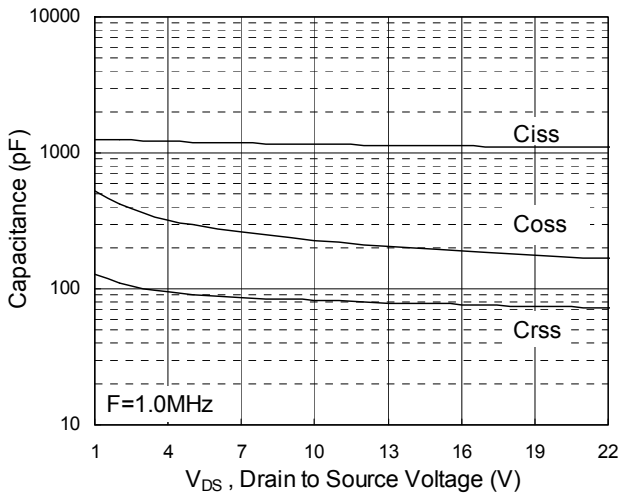


Fig.7 Capacitance

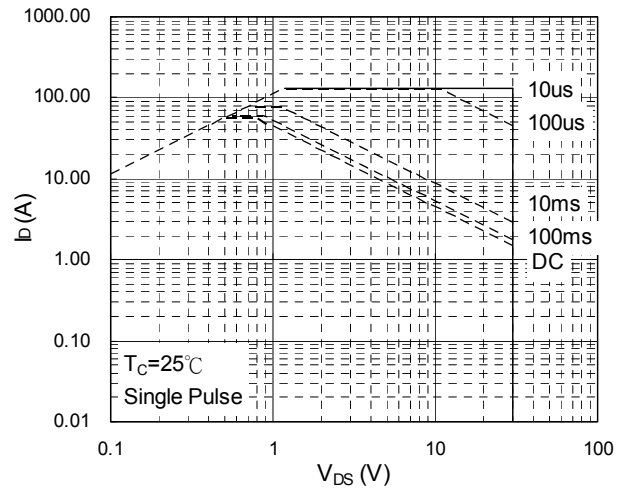


Fig.8 Safe Operating Area

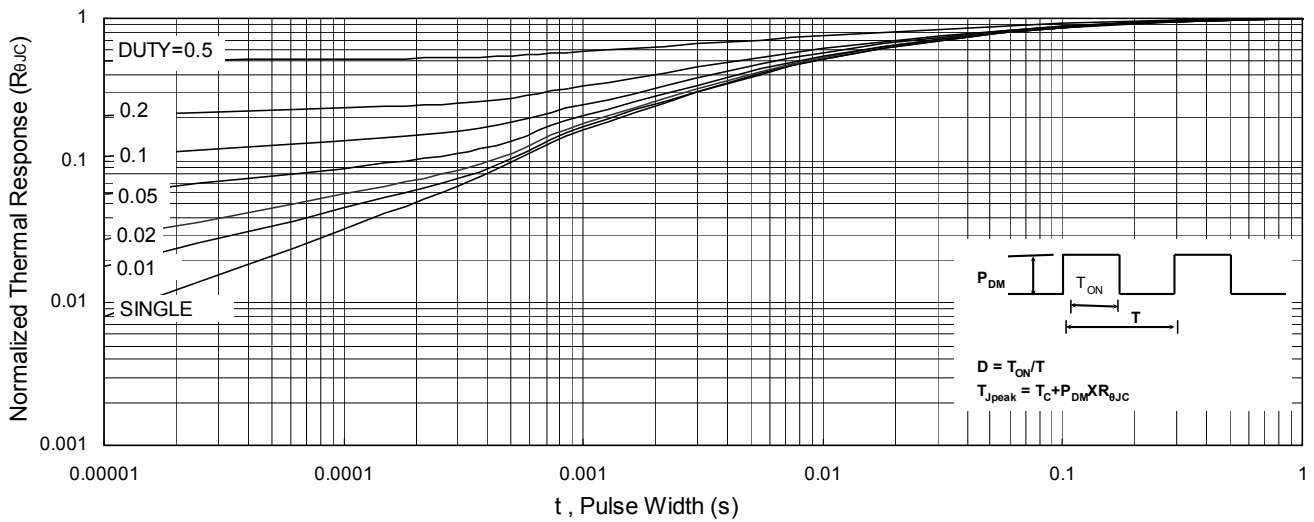


Fig.9 Normalized Maximum Transient Thermal Impedance

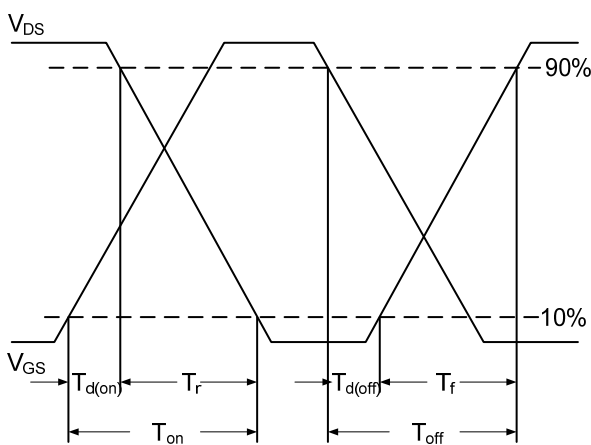


Fig.10 Switching Time Waveform

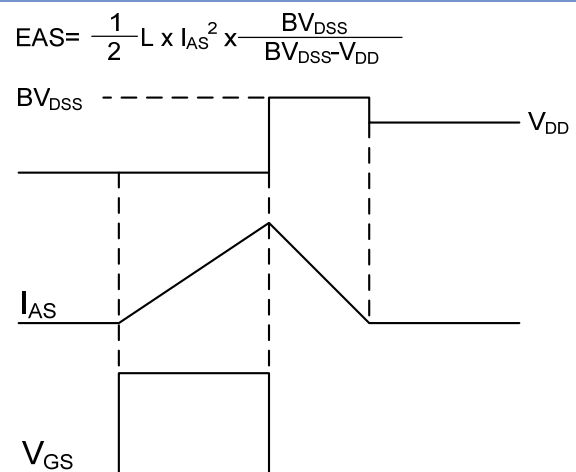


Fig.11 Unclamped Inductive Switching Waveform

N-Channel Typical Characteristics (Die2)

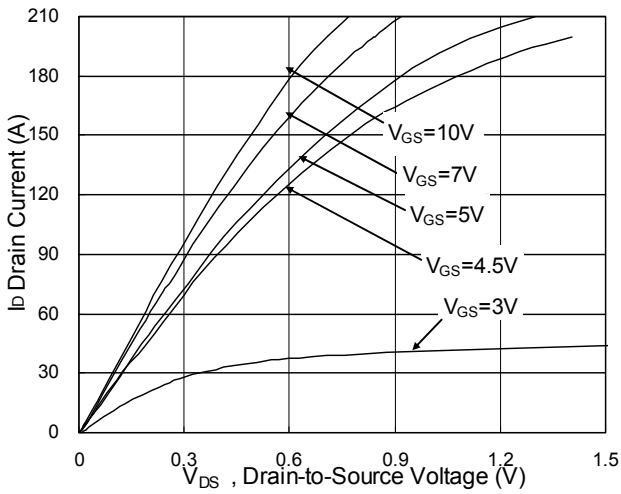


Fig.1 Typical Output Characteristics

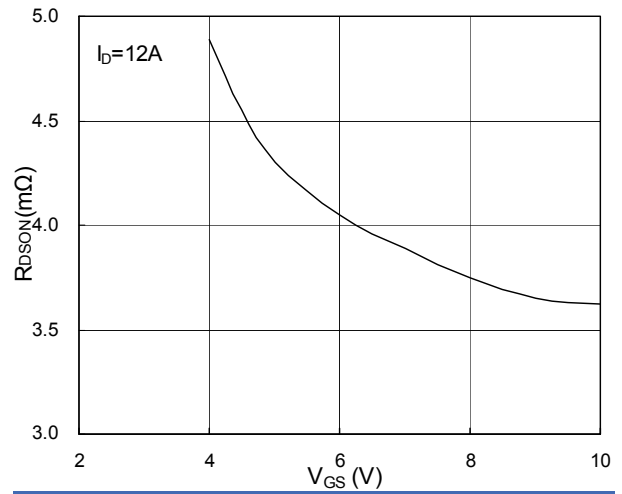


Fig.2 On-Resistance vs. G-S Voltage

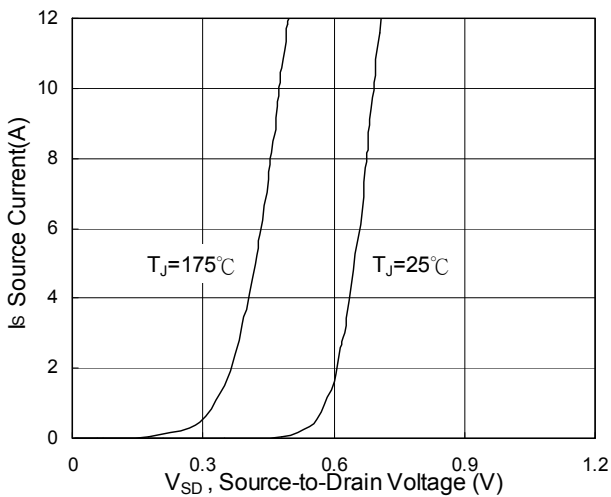


Fig.3 Forward Characteristics of Reverse

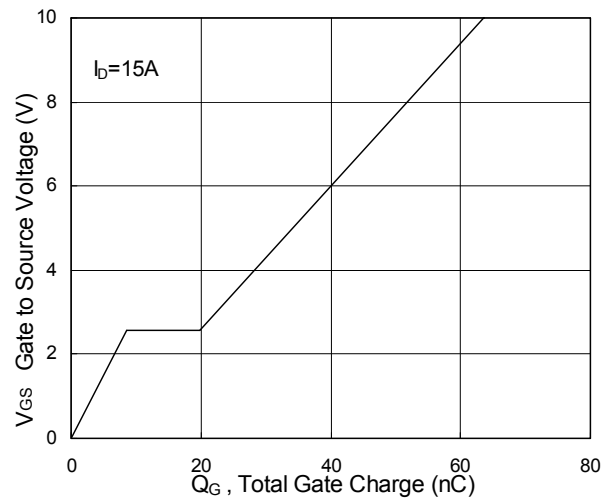


Fig.4 Gate-Charge Characteristics

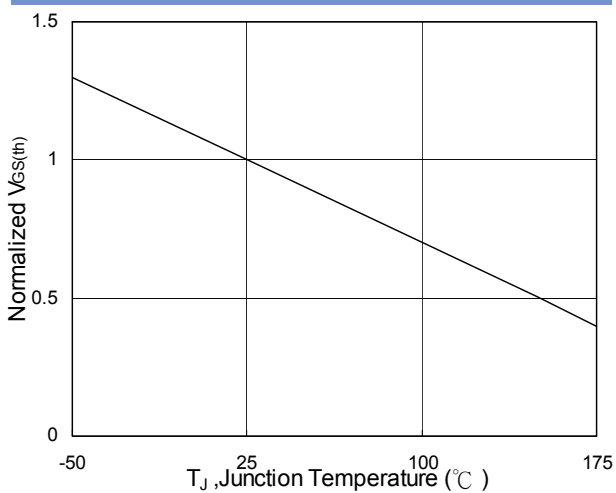


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

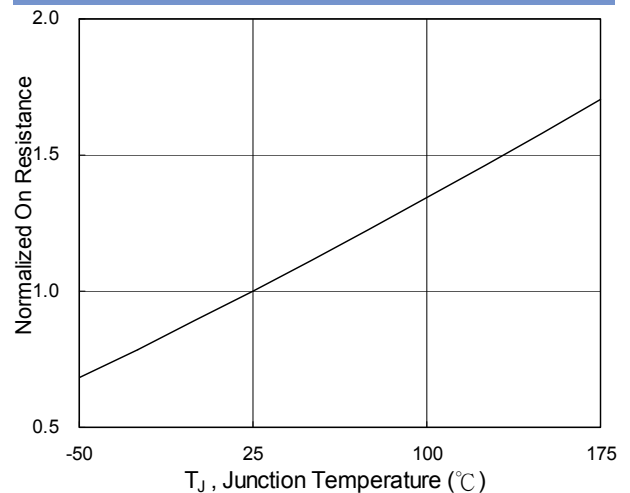


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

Dual N-Ch Fast Switching MOSFETs

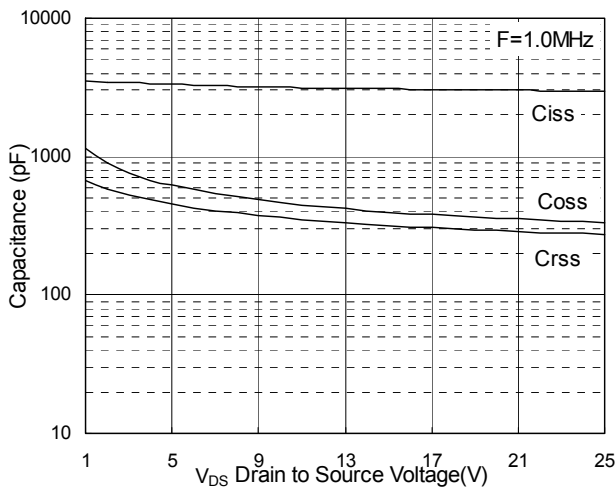


Fig.7 Capacitance

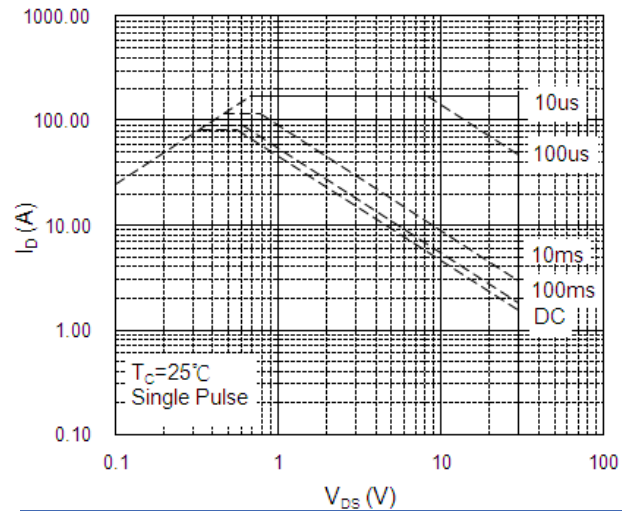


Fig.8 Safe Operating Area

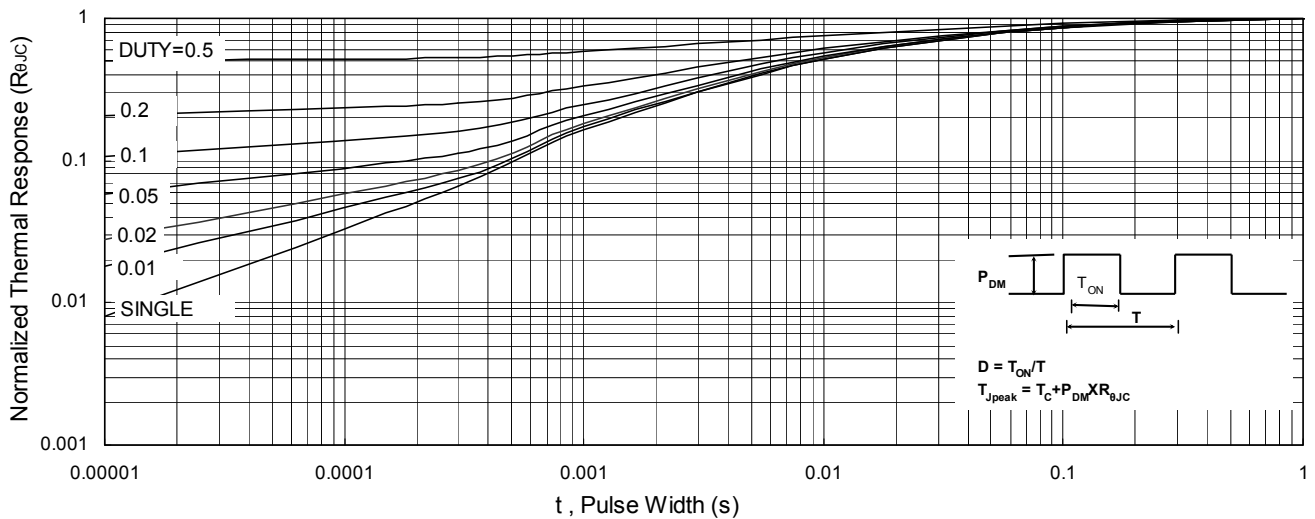


Fig.9 Normalized Maximum Transient Thermal Impedance

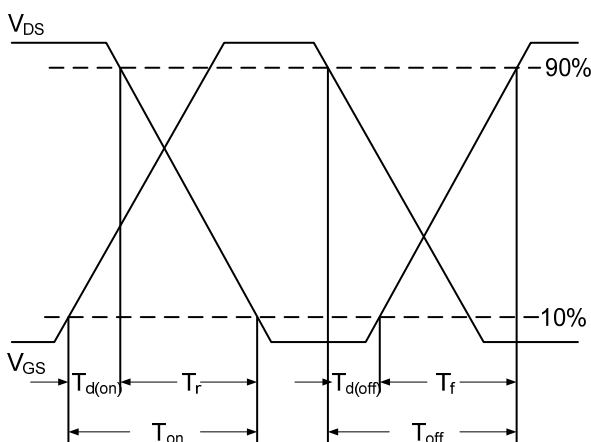


Fig.10 Switching Time Waveform

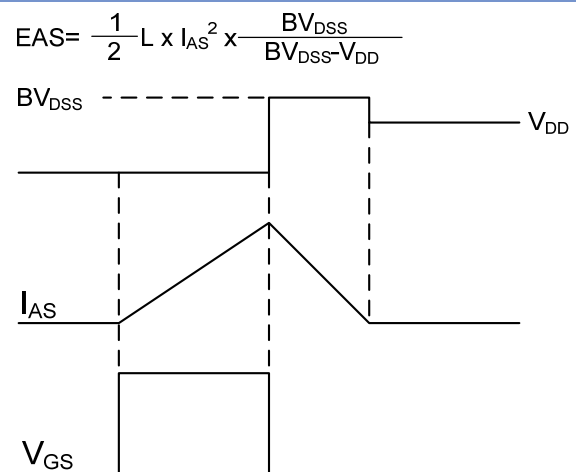


Fig.11 Unclamped Inductive Switching Waveform