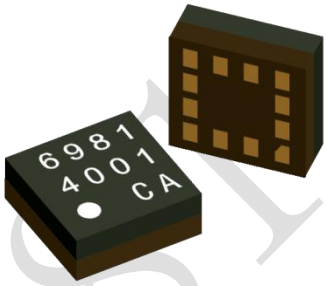
SingleChip 3-Axis Accelerometer QMA6981

Advanced Information

The QMA6981 is a single chip three-axis accelerometer. This surface-mount, small sized chip has integrated acceleration transducer with signal condition ASIC, sensing tilt, motion, shock and vibration, targeted for applications such as screen rotation, step counting, sleep quality, gaming and personal navigation in mobile and wearable smart devices.



The QMA6981 is based on our state-of-the-art, high resolution single crystal silicon MEMS technology. Along with custom-designed 10-bit ADC ASIC, it offers the advantages of low noise, high accuracy, low power consumption, and offset trimming. The I²C serial bus allows for easy interface.

The QMA6981 is in a 2x2x0.95mm3 surface mount 12-pin land grid array (LGA) package.

FEATURES	BENEFIT
3-Axis Accelerometer in a 2x2x0.95 mm^3 Land Grid Array Package (LGA), guaranteed to operate over a temperature range of -40 °C to +85 °C.	Small size for highly integrated products. Signals have been digitized and factory trimmed.
10 Bit ADC with low noise accelerometer sensor	High resolution allows for motion and tilt sensing
I^2C Interface with Standard and Fast modes.	High-Speed Interfaces for fast data communications. Maximum 2000Hz data output rate
Built-In Self-Test	Enables low-cost functionality test after assembly in production
Wide range operation voltage (2.4V To 3.6V) and low power consumption (27-50μA low power conversion current)	Automatically maintains sensor's sensitivity under wide operation voltage range and compatible with battery powered applications
Integrated FIFO with a depth of 32 frames	For higher Data-Read rate
RoHS compliant , halogen-free	Environmental protection and wide applications
Built–in motion algorithm	Low power and easy applications including step counting, sleep quality, gaming and personal navigation

CONTENTS

1 INTERNAL SCHEMATIC DIAGRAM

1.1 Internal Schematic Diagram

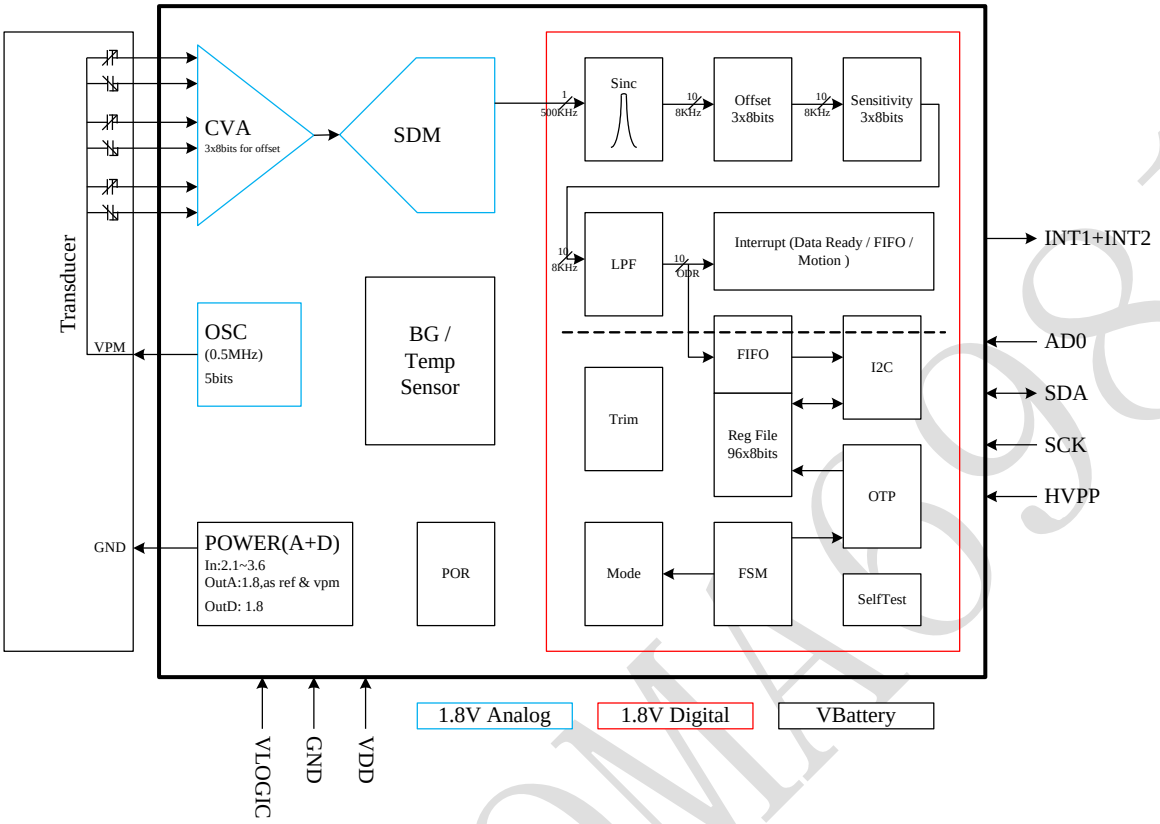


Figure 1. Block Diagram

Table 1. Block Function

Block	Function
Transducer	3 axis acceleration sensor
CVA	Charge-to-Voltage amplifier for sensor signals
Interrupt	Digital interrupt engine, to generate interrupt signal on data conversion, FIFO, and motion function
FIFO	Embedded 32-level FIFO
FSM	Finite state machine, to control device in different mode
I2C	Interface logic data I/O
OSC	Internal oscillator for internal operation
Power	Power block, including LDO

2 SPECIFICATIONS AND I/O CHARACTERISTICS

2.1 Product Specifications

Table 2. Specifications (* Tested and specified at 25°C except stated otherwise.)

Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage	AVDD, for internal blocks	2.4	3.3	3.6	V
I/O voltage	DVDD, for IO only	1.7	3.3	3.6	V
Standby current	DVDD and AVDD on.		2		μA
Low power current	BW=500 Hz, ODR=1 Hz		27		μA
Low power current	BW=500 Hz, ODR=10 Hz		29		μA
Low power current	BW=500 Hz, ODR=20 Hz		31		μA
Low power current	BW=500 Hz, ODR=40 Hz		37		μA
Low power current	BW=500 Hz, ODR=100 Hz		50		μA
Full run current	All blocks on, device in run state		220	300	uA
Sleep current	For analog, AFE is off, BG, Transducer and oscillator are on or in low power mode For digital, only counter and FSM are on		55		uA
Deep sleep current	For analog, only BG and oscillator are on For digital, only counter and FSM are on		26		uA
BW	Programmable bandwidth		3.9~500		Hz
Data output rate (ODR)	4*BW (ODRH=1)		15.6~2000		Samples /sec
Conversion time	in full speed		1/(4*BW)		mS
Startup time	From the time when VDD reaches to 90% of final value to the time when device is ready for conversion		2		mS
Wakeup time	From the time device enters into active mode to the time device is ready for conversion		1		mS
Operating temperature		-40		85	℃
Acceleration Full Range			+-2 +-4 +-8		G
Sensitivity	FS=±2g		256		LSB/G
Sensitivity	FS=±4g		128		LSB/G
Sensitivity	FS=±8g		64		LSB/G
Sensitivity Temperature Drift	FS=±2g, Normal VDD Supplies		±0.02		%/K
Sensitivity tolerance	Gain accuracy		+-5		%
Zero-g offset	FS=±2g, Normal VDD Supplies		80		mg
Zero-g offset Temperature Drift	FS=±2g, Normal VDD Supplies		2		mg/K
Noise density	FS=±2g, run state		800		ug/sqrtHz
Nonlinearity	FS=±2g, Best fit straight line,		±0.5		%FS
Cross Axis Sensitivity			1		%

2.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings (Tested at 25°C except stated otherwise.)

Parameters	Condition	Min	Max	Units
VDD		-0.3	5.4	V
VDDIO		-0.3	5.4	V
ESD	HBM		2	kV
Shock Immunity	Duration < 200uS		10000	Gee
Storage temperature		-50	150	℃

2.3 I/O Characteristics

Table 4. I/O Characteristics

Parameter	Symbol	Pin	Condition	Min.	TYP.	Max.	Unit
Voltage Input High Level 1	$V_{IH}1$	SDA, SCL		0.7*VDDIO		VDDIO+0.3	V
Voltage Input Low Level 1	$V_{IL}1$	SDA, SCL		-0.3		0.3*VDDIO	V
Voltage Output High Level	V_{OH}	INT1, INT2	Output Current ≥-100uA	0.8*VDDIO			V
Voltage Output Low Level	V_{OL}	INT1, INT2, SDA	Output Current ≤100uA(INT) Output Current ≤1mA (SDA)			0.2*VDDIO	V

3 PACKAGE PIN CONFIGURATIONS

3.1 Package 3-D View

Arrow indicates direction of G field that generates a positive output reading in normal measurement configuration.

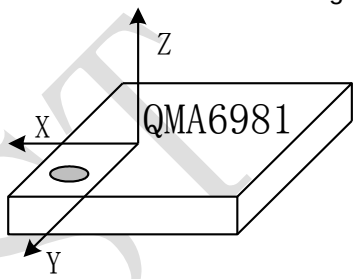


Figure 2. Package 3-D View

Table 5. Pin Configurations

PIN No.	PIN NAME	I/O	Power Supply	TYPE	Function
1	AD0	I	VDD	CMOS	LSB of I^2C address
2	SDA	I/O	VLOGIC	CMOS	Serial data for I^2C
3	VDDIO			Power	Power supply for digital interface
4	NC				Not Open to Customer
5	INT1	O	VLOGIC	CMOS	Interrupt 1
6	INT2	O	VLOGIC	CMOS	Interrupt 2
7	VDD			Power	Power supply to internal block

8	GNDIO			Power	Ground for digital interface
9	GND			Power	Ground for internal block
10	NC				Not Open to Customer
11	NC				Not Open to Customer
12	SCK	I	VLOGIC	CMOS	Serial clock for I^2C

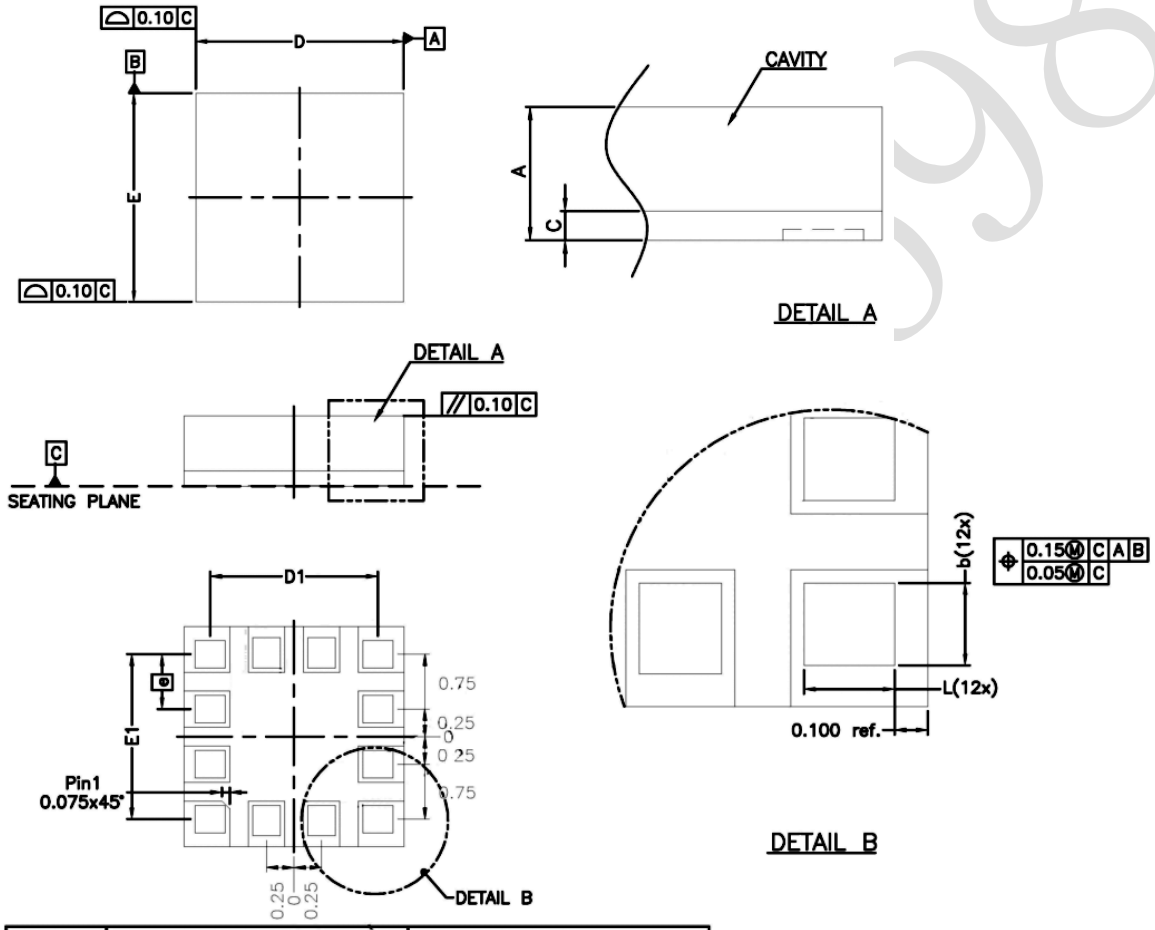
3.2 Package Outlines

3.2.1 Package Type

LGA (Land Grid Array)

3.2.2 Package Outline Drawing:

2.0mm (Length)*2.0mm (Width)*0.95mm (Height)



SYMBOL	DIMENSION (MM)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	0.95	1.00	0.035	0.037	0.039
C	0.16	0.20	0.24	0.006	0.008	0.009
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.95	2.00	2.05	0.077	0.079	0.081
D1	1.525 BSC			0.060 BSC		
E	1.95	2.00	2.05	0.077	0.079	0.081
E1	1.50 BSC			0.059 BSC		
e	0.50 BSC			0.020 BSC		
L	0.225	0.275	0.325	0.010	0.012	0.014

Figure 3. Package Outline Drawing

3.2.3 Marking:

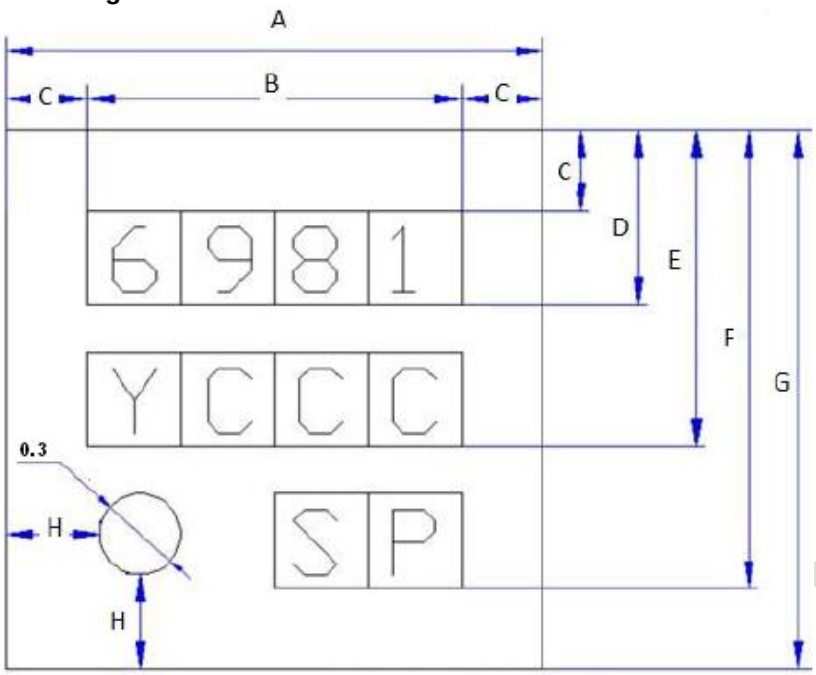


Figure 4. Chip Marking

Marking format and specification：

1) Laser marking, marking font：Arial

2) Marking dimensions: (Unit: mm)

	A	B	C	D	E	F	G	H	Pin 1	Letter style
Customer(T)	**2**	**1.4**	**0.3**	**0.65**	**1.175**	**1.7**	**2**	**0.3**	**0.3**	**Arial**
ChipMOS(T)	**2**	**1.38**	**0.283**	**0.662**	**1.171**	**1.667**	**2**	**0.294**	**0.296**	**Arial**

3) Offset tolerance：±0.2mm

4) Marking definition：

Marking Text	Description	Comments
Line 1	Product Name	4 alphanumeric digits stand for product serials, such as “6981” stand for QMA6981 serials product.
Line 2	Y: the last digital of year CCC: lot code	3 alphanumeric digits, variable to generate mass production trace-code
Line3	P: Part number S: Sub-con ID	P: 1 alphanumeric digits, fixed to identify part number, such as “A” stand for the part number QMA6981A2. S: 1 alphanumeric digits, variable identify sub-con, such as “C” stand for ChipMOS.
	Pin 1 identifier	Pin1 marking is positioned accordingly with unfilled-corner PIN on substrate.

4 EXTERNAL CONNECTION

4.1 Dual Supply Connection

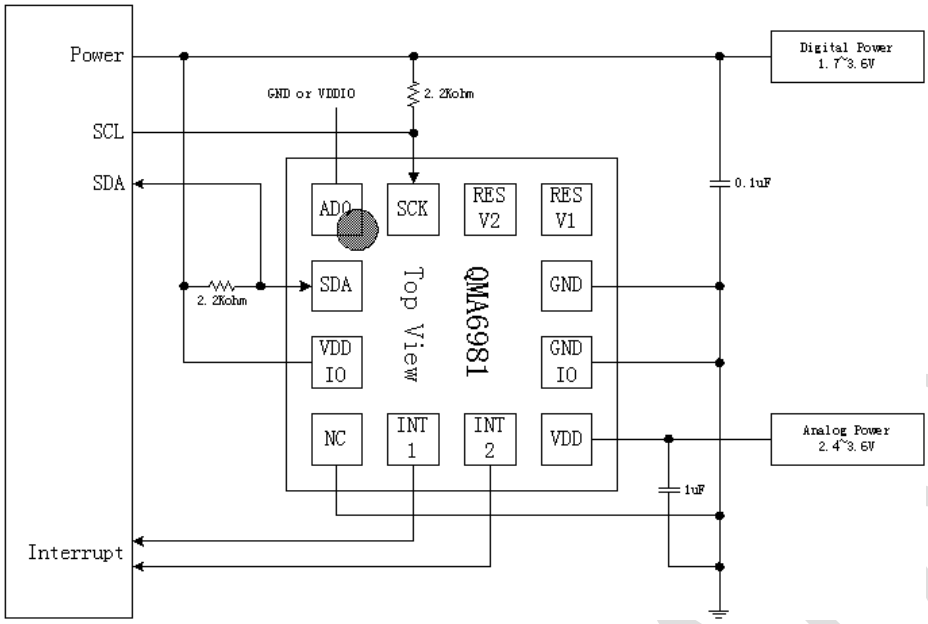


Figure 5. Dual Supply Connection

4.2 Single Supply connection

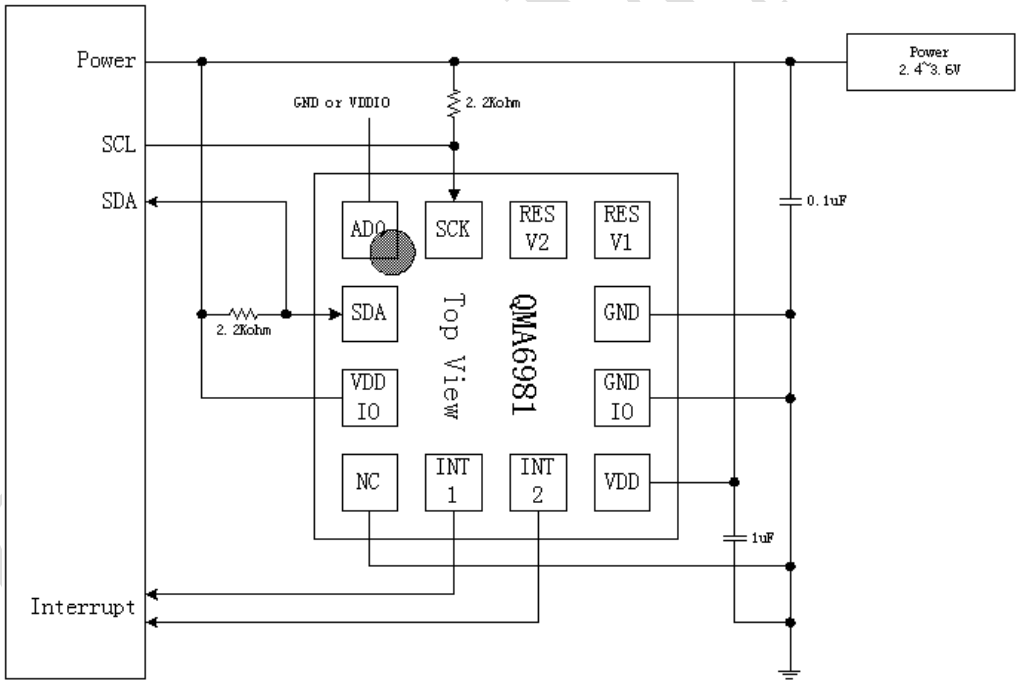


Figure 6. Single Supply Connection

5 BASIC DEVICE OPERATION

5.1 Acceleration Sensors

The QMA6981 acceleration sensor circuit consists of tri-axial sensors and application specific support circuits to measure the acceleration of device. With a DC power supply is applied to the sensor two terminals, the sensor converts any accelerating incident in the sensitive axis directions to a differential voltage output.

5.2 Power Management

Device has two power supply pins. VDD is the main power supply for all of the internal blocks, including analog and digital. VDDIO is a separate power supply, for digital interface only.There is no limitation on the voltage levels of VDD and VDDIO relative to each other, as long as they are within operating range.

The device contains a power-on-reset generator. It generates reset pulse as power on, which can load the register's default value, for the device to function properly.
To make sure the POR block functions well, we should have such constrains on the timing of VDD.

The device should turn-on both power pins in order to operate properly. When the device is powered on, all registers are reset by POR, then the device transits to the standby mode and waits for further commends.

Table 6 provides references for four power states. Transitions between power state 2 and power state 3 are prohibited, due to leakage current concerns.

Table 6: Power States

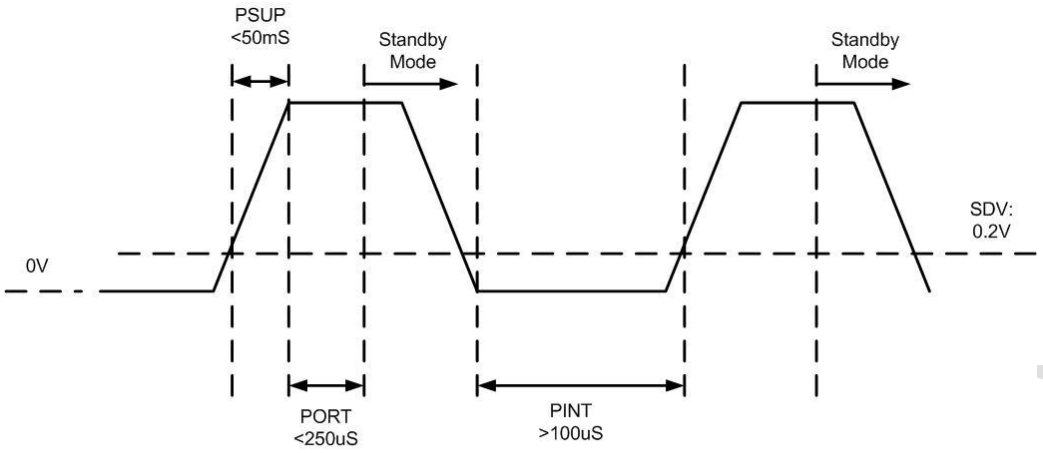
Power State	VDD	VLOGIC	Power State description
1	0V	0V	Device Off, No Power Consumption
2	0V	1.7v~3.6v	Device Off, Unpredictable Leakage Current on VLOGIC due to Floating Node.
3	2.4v~3.6v	0	Device Off, Same Current as Standby Mode
4	2.4v~3.6v	1.7v~3.6v	Device On, Normal Operation Mode, Enters Standby Mode after POR

5.3 Power On/Off Time

After the device is powered on, some time periods are required for the device fully functional. The external power supply requires a time period for voltage to ramp up (PSUP), it is typically 50 milli-second. However it isn't controlled by the device. The Power –On –Reset time period (PORT) includes time to reset all the logics, load values in NVM to proper registers, enter the standby mode and get ready for analogy measurements. The power on/off time related to the device is in Table 7.

Table 7. Time Required for Power On/Off

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
POR Completion Time	PORT	Time Period After VDD and VLOGIC at Operating Voltage to Ready for I^2C Commend and Analogy Measurement.			350	uS
Power off Voltage	SDV	Voltage that Device Considers to be Power Down.			0.2	V
Power on Interval	PINT	Time Period Required for Voltage Lower Than SDV to Enable Next POR	100			uS



Power On/Off Timing

Figure 7. Power On/Off Timing

5.4 Communication Bus Interface I²C and Its Addresses

This device will be connected to a serial interface bus as a slave device under the control of a master device, such as the processor. Control of this device is carried out via I²C.

This device is compliant with I²C -Bus Specification, document number: 9398 393 40011. As an I²C compatible device, this device has a 7-bit serial address and supports I²C protocols. This device supports standard and fast speed modes, 100kHz and 400kHz, respectively. External pull-up resistors are required to support all these modes.

There are two I²C addresses selected by connecting pin 1 (AD0) to GND or VDD. The first six MSB are hardware configured to "001001" and the LSB can be configured by AD0.

Table 8. I2C Address Options

AD0 (pin 10)	I²C Slave Address(HEX)	I²C Slave Address(BIN)
Connect to GND	12	0010010
Connect to VDD	13	0010011

If more I²C address options are required, please contact factory for metal layer changes.

5.5 Internal Clock

The device has an internal clock for internal digital logic functions and timing management. This clock is not available to external usage.

6 MODES OF OPERATION

6.1 Modes Transition

The device has two different operational modes, controlled by register (11H), mode bit. The main purpose of these modes is for power management. The modes can be transited from one to another, as shown below, through I²C commends of changing mode bits. The default mode is Standby.

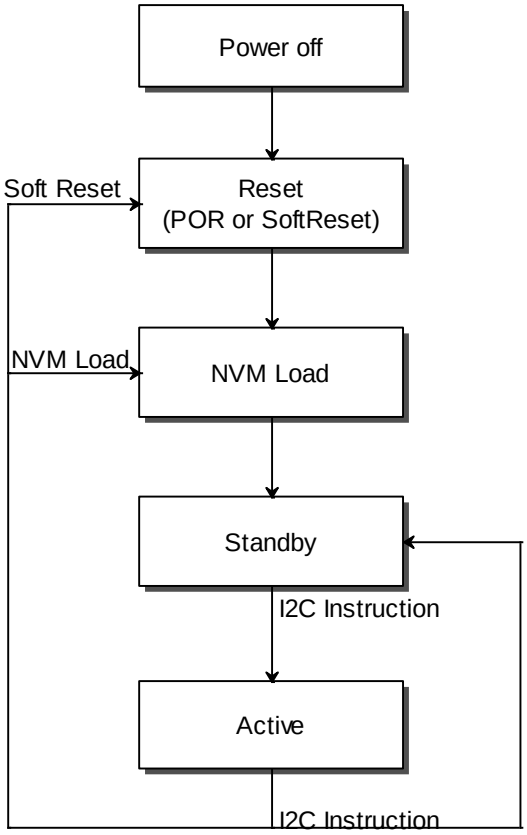


Figure 8. Basic operation flow after power-on

The default mode after power on is standby mode. Through I2C instruction, device can switch between standby mode and active mode. With SOFTRESET by writing 0xB6 into register 0x36, all of the registers will get default values. SOFTRESET can be done both in active mode and in standby mode. Also, by writing 1 in NVM_LOAD (0x33<3>) when device is in active mode, the NVM related image registers will get default value from NVM, however, other registers will keep the values of their own.

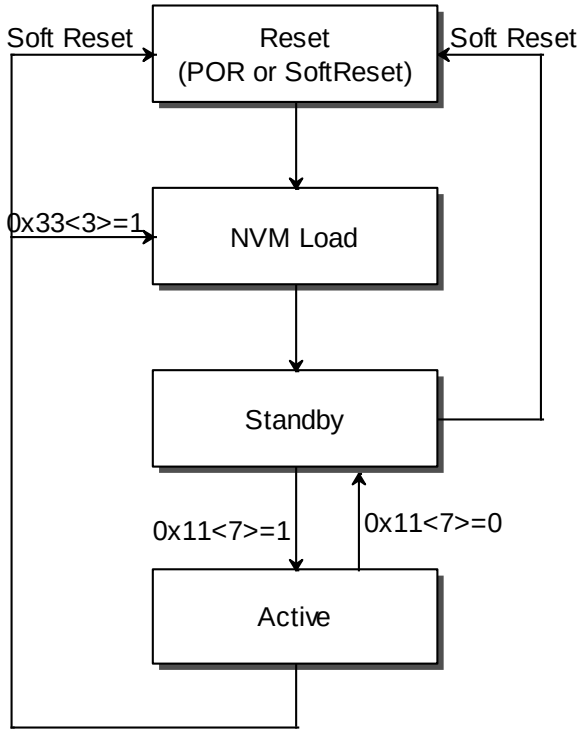


Figure 9. The work mode transferring

6.2 Description of Modes

6.2.1 Active Mode

In active mode, there are two states, run state, and deep sleep state.

6.2.1.1 Sleep State

In sleep state, whole signal chain is off, including analog and digital signal conditioning. And the rest blocks are on, including REF and OSC.

6.2.1.2 Run State

In run state, the ADC digitizes the charge signals from transducer, and digital signal processor conditions these signals in digital domain, processes the interrupts, and send data into FIFO (accessible through register 0x3F) and Data registers (0x01~0x06). After the signal conditioning, the signal chain will be off and ASIC enters back into sleep state, leaves timer and FSM on. Also in sleep state, reference and power blocks are on. This mode can also be called as power cycling. The power cycling duty is configurable through state registers SLEEP_DUR (0x11<3:0>). Device can enter into active mode by setting MODE_BIT (0x11<7>) to logic 1.

Besides the power cycling, device can also be configured as FULLRUN, by setting SLEEP_DUR=0000b. In this setting, no sleep state in the active mode, and device consumes most power, deliver the data most frequently.

6.2.1.3 Self-test State

In active mode, when user set SELFTEST_BIT (0x32<7>) to logic 1, ASIC will generate self-test signal onto the transducer, which transfer to electro-static force, to move the transducer. SELF_TEST_SIGN (0x32<2>) is used to set the force to negative.

For proper function of self-test, user should set SELFTEST_BIT to logic 1 for at least 4mS, for the settling of transducer due to self-test force.

User can compare the data before self-test with that after self-test. If the difference between these two data is larger than value listed in following, the device functions well. Also, please make sure that no external acceleration is added on the device.

	X axis	Y axis	Z axis
Effective self-test signal	0.3g	0.3g	0.3g

After done the self-test, please set the SELFTEST_BIT back to logic 0.

6.2.2 Standby Mode

In standby mode, most of the blocks are off, while device is ready for access through I2C. Standby mode is the default mode after power on or soft reset. Device can enter into this mode by set the soft reset register (0x36) to 0xB6 or set the MODE_BIT (0x11<7>) to logic 0.

Besides the above two modes, device also contains NVM loading state. This state is used to reset the value of the NVM related image registers. There are two bits related to this state. When NVM_LOAD (0x33<3>) is set to 1, NVM loading starts. When device is in NVM loading state, NVM_RDY (0x33<2>) is set to logic 0 by device. After NVM loading finished, NVM_RDY (0x33<2>) is set back to logic 1 by device, and NVM_LOAD is reset to 0 by device automatically. NVM loading can only happen when NVM_LOAD is set to 1 in active mode. If user set this NVM_LOAD bit to 1 in standby mode, device will not take the action until the device enters into active state by setting MODE_BIT (0x11<7>) to logic 1.

After loading NVM, the device will enter into standby mode directly.

The loading time for NVM is about 100uS.

7 Functions and interrupts

ASIC support interrupts, such as POL_INT, FOB_INT (4D/6D), FLAT_INT, FF_INT, TAP_INT, SHK_INT, SLO_NO_MOT_INT, DRDY_INT, FIFO_INT, LPF, etc. (these functions are first priority)

Also we support SLOPE_INT, HPF, high-g?, low-g, I2C watch dog timer, etc. (these functions are second priority)

If necessary, we support Master I2C and FIFO for mag. (these are third priority)

And, if necessary, we support SPI. (this is fourth priority)

7.1 POL_INT

The POL _INT stands for Portrait or Landscape interrupt, responses to the device in portrait direction or landscape direction. It includes 4 different event types, left, right, up and down events. The different type event stored and can be read from register ORIENT (0x0D<2:0>).

POLA(0x0D<2:0>)	Left	Right	Down	Up	comments
000	0	0	0	0	unknown
001	1	0	0	0	Left/Landscape
010	0	1	0	0	Right/Landscape
101	0	0	1	0	Down/portrait
110	0	0	0	1	Up/portrait

All different event can be detected by comparing the threshold set by register UD_X_TH(0x2D),RL_Y_TH(0x2F) with the sensor data , also have dependency on comparing result between the Z sensor readings and the register UD_Z_TH(0x2C) and RL_Z_TH(0x2E). Hysteresis can be introduced to the angle by decreasing a small offset for the threshold registers. All angle data inside the Hysteresis area will be regarded as unknown status in the orient status register (0x0D<2:0>).

Below Table shows the condition for kinds of orient events generation, the default threshold for X, Y is set to 40 degrees

Event	X	Y	Z
Up	|X|>UD_X_TH X <0		|Z|<UD_Z_TH
Down	|X|>UD_X_TH X >0		|Z|<UD_Z_TH
Right		|Y|>RL_Y_TH Y <0	|Z|<RL_Z_TH
Left		|Y|>RL_Y_TH Y >0	|Z|<RL_Z_TH

For the registers settings, all the orient events threshold 1 LSB bit stand for 3.9mg. For Z axis, it is 8-bit signed 2's complement number ranged from 0.3g to 1.29g, default value 0 as stands for 0.8g. X, Y axis are unsigned data, default value A4 stands for 640mg which angel be regards as 40 degree ,there will be around 10 degree dead band left. The degree value for event can be calculated by the equal arcsin(0.0039*ud_x_th) or arcsin(0.0039*rl_y_th).

The related interrupt status bit is ORIENT_INT (0x09<6>). When the POL status changed, the value of ORIENT_INT will be set to logic 1, and this will be cleared after the interrupt status register is read by user. ORIENT_EN (0x16<6>) is the enable bit for the POL_INT. Also, to get this interrupt on PIN_INT1 and/or PIN_INT2, we need to set INT1_ORIENT (0x19<6>) or INT2_ORIENT (0x1B<6>) to logic 1, to map the internal interrupt to the interrupt PINs.

7.2 FOB_INT

The Front/back event detected by comparing Z axis data with a low g value, ranged from 0.1g to 0.6g, which is defined by FB_Z_TH(0x30). The comparing condition shows below:

Event	X	Y	Z
Front			|Z|>FB_TH Z>0
Back			|Z|>FB_TH Z<0

The 2 different type events are stored and can be read from register ORIENT (0x0D<4:3>)

FOB(0x0D<4:3>)	status
00	unknown
01	Front
10	Back
11	Reserved

Angle between the Z-axis and g can have the relationship:
Acc_Z=1g X cos(theta).
Each threshold will introduce a dark area, which the Front/Back status cannot be recognized, the dark area angel is +/- (90-theta).
When the threshold register value is 0x00, the default value stands for 0.1g, and 1 LSB is 2mg. the minimum angel between sensor and g direction should be 84 degree, so the dark area should be +/-6 degree. When the value is 0xFF, the dark area should be +/-37 degree.
The related interrupt status bit is FOB_INT (0x09<7>). When the FOB status changed, the value of FOB_INT will be set to logic 1, and this will be cleared after the interrupt status register is read by user. FOB_EN (0x16<6>) is the enable bit for the FOB_INT. Also, to get this interrupt on PIN_INT1 and/or PIN_INT2, we need to set INT1_FOB (0x19<7>) or INT2_FOB (0x1B<7>) to logic 1, to map the internal interrupt to the interrupt PINs.

7.3 STEP/STEP_QUIT INT

The STEP/STEP_QUIT detect that the user is entering/exiting step mode. When the user enter into step mode, at least one axis sensor data will vary periodically, by numbering the variation periods the step counter can be calculated.

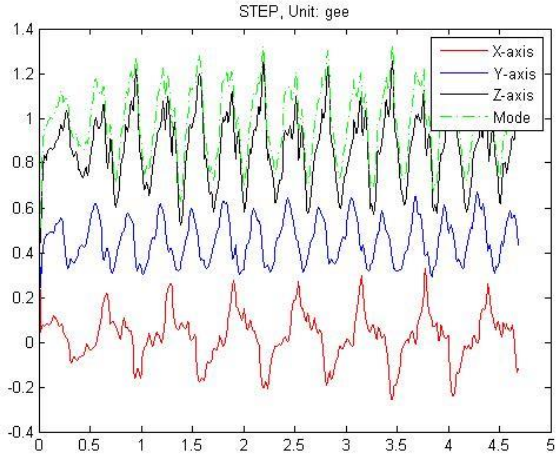


Figure 10. STEP/STEP_QUIT

Median data (max+min) /2 is called dynamic threshold, the max and min data can be updated by certainly samples, the sample number can be set by register STEP_SAMPLE_CNT (0x12). When the sensor data decreasing (or increasing) through the dynamic threshold, a user run step is detected.
Register STEP_PRECISION (0x13) is used as threshold when updating the new collected sensor data. Sensor data below the threshold will be discarded, this helps removing unstable variations causing failed detection.
The run step event happened at certain interval timing. All of the events outside the timing window will not be regarded as a run step and the step counter will not counted. The timing window can be set by register STEP_TIME_UP(0x15) and STEP_TIME_LOW(0x14), the conversion ODR numbers ranged from STEP_TIME_LOW *ODR to 8* STEP_TIME_UP*ODR . Also if no new run step event detected until the up limited timing threshold, STEP_QUIT INT will generation.
To remove unstable variation which will cause failing STEP event detection, only after 4 continuous step detected, it will be considered as valid step events , also the step counter register STEP_CNT_LSB/ STEP_CNT_MSB (0x1C,0x1D) will updated immediately by value 4, interrupt STEP is generated as well.
The related interrupt status bit is STEP_INT (0x0A<4 >) and STEP_QUIT_INT (0x0A<3>). When the interrupt is generated, the value of STEP_INT/ STEP_QUIT_INT will be set to logic 1, and this will be cleared after the interrupt status register is read by user. STEP_EN/STEP_QUIT_EN (0x16<3>/0x16<2>) is the enable bit for the STEP_INT/STEP_QUIT_INT. Also, to get this interrupt on PIN_INT1 and/or PIN_INT2, we need to set INT1_STEP (0x1A<3>)/INT1_STEP_QUIT (0x19<2>) or INT2_STEP (0x1A<4>) /INT2_STEP_QUIT (0x1B<2>) to logic 1, to map the internal interrupt to the interrupt PINs.

7.4 TAP_INT

Tap detection allows the device to detect the events such as clicking or double clicking of a touch-pad. A tap event is detected if a pre-defined slope (absolute value of acceleration difference) of the acceleration of at least one axis is exceeded. The tap detection includes single tap (TAPS) and double tap (TAPD). A ‘Single tap’ is a single event within a certain time, followed by a certain quiet time. A ‘double tap’ consists of a first such event followed by a second event within a defined time frame.
Single tap interrupt can be enabled (disabled) by setting ‘1’ (‘0’) to bit (0x16) S_TAP_EN. The double tap detection can be enabled (disabled) by setting ‘1’ (‘0’) to (0x16) D_TAP_EN.
The status of single tap interrupt is stored in (0x0A) S_TAP_INT, the status of double tap interrupt is stored in (0x0A) D_TAP_INT.
The slope threshold for detecting a tap event is set by register (0x2B) TAP_TH. The meaning of an LSB of (0x2B) TAP_TH depends on the selected g-range: 1 LSB of the (0x2B) TAP_TH is 62.5mg in 2g-range, 125mg in 4g-range, 250mg in 8g-range.
In figure the timing for single tap and double tap is visualized:

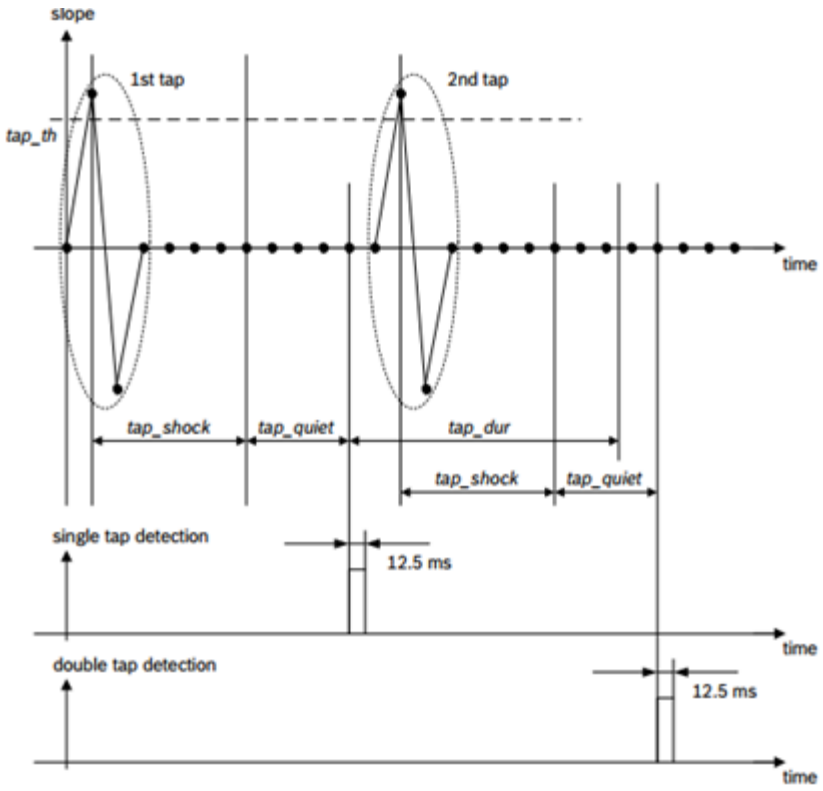


Figure 11. Timing of tap detction

The parameters (0x2A) TAP_SHOCK and (0x2A) TAP_QUIET are effect in both single tap and double tap detection, while (0x2A) TAP_DUR is effect in double tap detection only. Within the duration of (0x2A) TAP_SHOCK, any slope exceeding (0x2B) TAP_TH after the first event will be ignored. Contrary to this, within duration of (0x2A) TAP_QUIET, no slope exceeding (0x2B) TAP_TH must occur, otherwise the first event will be cancelled.
A single tap interrupt is generated after the combined duration of (0x2A) TAP_SHOCK and (0x2A) TAP_QUIET. The interrupt is cleared after a delay of 12.5ms.
A double tap interrupt is generated if an event fulfilling the conditions for a single tap occurs within the duration defined by (0x2A) TAP_DUR after the completion of the first tap event. The interrupt is cleared after a delay of 12.5ms.
For each of parameter (0x2A) TAP_SHOCK and (0x2A) TAP_QUIET two values are selectable. By writing '0' ('1') to bit (0x2A) TAP_SHOCK, the duration of (0x2A) TAP_SHOCK is set to 50ms (75ms). By writing '0' ('1') to bit (0x2A) TAP_QUIET, the duration of (0x2A) TAP_QUIET is set to 30ms (20ms).
The duration of (0x2A) TAP_DUR can be set by (0x2A) TAP_DUR bits:

TAP_DUR	Duration of TAP_DUR
000	50ms
001	100ms
010	150ms
011	200ms
100	250ms
101	375ms
110	500ms
111	700ms

The axis which triggered the interrupt is indicated by bits (0x0B) TAP_FIRST_X, (0x0B) TAP_FIRST_Y, and (0x0B) HIGH_FIRST_Z. The bit corresponding to the triggering axis contains a '1' while the other bits hold a '0'. These bits hold until new interrupt is triggered.
The sign of the triggering acceleration is stored in bit (0x0B) TAP_SIGN. If the (0x0C) HIGH_SIGN = '0' ('1'), the sign is positive (negative). This bit holds until new interrupt is triggered.

7.5 LOW-G_INT

The low-g interrupt is based on the comparison of acceleration data against a low-g threshold for the detection of free-fall.
The low-g interrupt is enabled (disabled) by writing logic '1' ('0') to bits (0x17) LOW_EN. There are two modes available, 'single' mode and 'sum' mode. In 'single' mode, the acceleration of each axis is compared with the threshold; in 'sum' mode, the sum of absolute value of all accelerations $|acc\_x| + |acc\_y| + |acc\_z|$ is compared with the threshold. The mode is selected by the contents of the (0x24) LOW_MODE bit: '0' means 'single' mode, '1' means 'sum' mode.
The low-g threshold is set through the (0x23) LOW_TH register. 1 LSB of (0x23) LOW_TH always corresponds to an acceleration of 7.81mg (increment is independent from g-range setting).
A hysteresis can be set with the (0x24) LOW_HYST bits. 1 LSB of (0x24) LOW_HYST always corresponds to an acceleration of 125mg (as well, increment is independent from g-range setting).
The low-g interrupt is generated if the absolute values of the acceleration of all axes ('and' relation, in case of 'single' mode) or their sum (in case of 'sum' mode) are lower than the threshold for at least the time defined by the (0x22) LOW_DUR register. The interrupt is reset if the absolute value of the acceleration of at least one axis ('or' relation, in case of 'single' mode) or the sum of absolute values (in case of 'sum' mode) is higher than the threshold plus the hysteresis for at least one data acquisition. The relation between the content of (0x25) LOW_DUR and the actual delay of the interrupt generation is delay = [(0x22) LOW_DUR+1]*2ms. The interrupt status is stored in bit (0x0B) LOW_INT.

7.6 HIGH-G_INT

The high-g interrupt is based on the comparison of acceleration data against a high-g threshold for the detection of shock or other high-acceleration events.
The high-g interrupt is enabled (disabled) per axis by writing logic '1' ('0') to bits (0x17) HIGH_EN_X, (0x17) HIGH_EN_Y, and (0x17) HIGH_EN_Z, respectively. The high-g threshold is set through the (0x26) HIGH_TH register. The meaning of an LSB of (0x26) HIGH_TH depends on the selected g-range: it corresponds to 7.81mg in 2g-range (15.63mg in 4g-range, 31.25mg in 8g-range).
A hysteresis can be set with the (0x24) HIGH_HYST bits. Analogously to the (0x26) HIGH_TH, the meaning of an LSB of (0x24) HIGH_HYST depends on the selected g-range: it corresponds to 125mg in 2g-range (250mg in 4g-range, 500mg in 8g-range).
The high-g interrupt is generated if the absolute value of the acceleration data of at least one of the enabled axes ('or' relation) is higher than the threshold for at least the time defined by the (0x25) HIGH_DUR register. The interrupt is reset if the absolute value of the acceleration of all enabled axes ('and' relation) is lower than the threshold minus the hysteresis. The relation between the content of (0x25) HIGH_DUR and the actual delay of the interrupt generation is delay = [(0x25) HIGH_DUR+1]*2ms.
The interrupt status is stored in bit (0x09) HIGH_INT. The axis which triggered the interrupt is indicated by bits (0x0C) HIGH_FIRST_X, (0x0C) HIGH_FIRST_Y, and (0x0C) HIGH_FIRST_Z. The bit corresponding to the triggering axis contains a '1' while the other bits hold a '0'. These bits hold until new interrupt is triggered.
The sign of the triggering acceleration is stored in bit (0x0C) HIGH_SIGN. If the (0x0C) HIGH_SIGN = '0' ('1'), the sign is positive (negative). This bit holds until new interrupt is triggered.

7.7 DRDY_INT

The width of the acceleration data is 10 bits, in two's complement representation. The data of each axis is split into 2 parts, the MSB part (one byte contains bit 11 to bit 4) and the LSB part (one byte contains bit 3 to bit 0). Reading data should start with LSB part. When user is reading the LSB byte of data, to ensure the integrity of the acceleration data, the content of MSB can be locked, by setting SHADOW_DIS (0x21<6>) to logic 0. This lock function can be disabled by setting SHADOW_DIS to logic 1. Without lock, the MSB and LSB content will be updated by new value immediately. The bit NEW_DATA in the LSB byte is the flag of the new data. If new data is updated, this NEW_DATA flag will be 1, and will be cleared when corresponding MSB or LSB is read by user. Also user should note that, even with SHADOW_DIS=0, the data of 3 axes are not guaranteed from the same time point. If user need all of the 3 axes data from the same time point, please use FIFO. Detailed information, user can refer to 6.8.
If SLEEP_DUR is set to be 0000, then the data can be filtered by low-pass filter, with bandwidth is set by BW (0x10<4:0>). If SLEEP_DUR is set to be other values, the data also can be averaged in different way (set by BW). In any conditions, the data stored in data registers are offset-compensated.

The device supports four different acceleration measurement ranges. The range is setting through RANGE (0x0F<3:0>), and the details as following:

RANGE	Acceleration range	Resolution
0001	2g	3.9mg/LSB
0010	4g	7.8mg/LSB
0100	8g	15.6mg/LSB
Others	Reserved	0.98mg/LSB

The interrupt for the new data serves for the synchronous data reading for the host. It is generated after storing a new value of z-axis acceleration data into data register. This interrupt will be cleared automatically when the next data conversion cycle starts, when SLEEP_DUR is not set to 0000b. When device is in full run (SLEEP_DUR=0000), the interrupt will be effective about 128us, and automatically cleared.
The interrupt mode for the new data is fixed to be non-latched.

7.8 FIFO_INT

The device has integrated FIFO memory, capable of storing up to 32 frames, with each frame contains three 10 bits words, for acceleration data of x, y, and z axis. All of the 3 axes acceleration are sampled at same point in time line.

The FIFO can be configured as three modes, FIFO mode, STREAM mode, and BYPASS mode.
FIFO mode.
In FIFO mode, the acceleration data of selected axes are stored in the buffer memory. If enabled, a watermark interrupt can be triggered when the buffer filled up to the defined level. The buffer will continuously be filled until the fill level reaches to 32. When the buffer is full, data collection stops, and the new data will be ignored. Also, FIFO_FULL interrupt will be triggered when enabled.
STREAM mode
In STREAM mode, the acceleration data of selected axes will be stored into the buffer until the buffer is full. The buffer's depth is 31 now. When the buffer is full, data collection continues, and the oldest data is discarded. If enabled, a watermark interrupt will be triggered when the fill level reached to the defined level. Also, when buffer is full, FIFO_FULL interrupt will be triggered if enabled. If any old data is discarded, the FIFO_OR (0x0E<7>) will be set to be logic 1.
BYPASS mode
In BYPASS mode, only the current acceleration data of selected axes can be read out from the FIFO. The FIFO acts like the STREAM mode with a depth of 1. Compare to reading directly from data register, this mode has the advantage of ensuring the package of xyz data are from same point of time line. The data registers are updated sequentially and have chance for the xyz data sampled in different time. Also, if any old data is discarded, the FIFO_OR will be set to be logic 1, similar as that in stream mode.
The FIFO mode can be configured by setting FIFO_MODE (0x3E<7:6>).

FIFO_MODE	Mode
00	BYPASS
01	FIFO
10	STREAM
11	FIFO

User can select the acceleration data of which axes to be stored in the FIFO. This configuration can be done by setting FIFO_CH (0x3E<1:0>), where '00b' for x-, y-, and z-axis, '01b' for x-axis only, '10b' for y-axis only, '11b' for z-axis only.
If all the 3 axes data are selected, the format of data read from 0x3F is as follows

XLSB	XMSB	YLSB	YMSB	ZLSB	ZMSB

These comprise one frame
If only one axis is enabled, the format of data read from 0x3F is as follows

YLSB	YMSB

These comprise one frame
If the frame is not read completely, the remaining parts of the frame will be discarded.
If the FIFO is read beyond the FIFO fill level, all zeroes will be read out.

FIFO_FRAME_COUNTER (0x0E<6:0>) reflects the current fill level of the buffer. If additional data frames are written into the buffer when the FIFO is full (in Stream mode or Bypass mode), then, FIFO_OR (0x0E<7>) is set to 1. This FIFO_OR can be considered as flag of discarding old data.
When a write access to one of the FIFO configuration registers (0x3E) or (0x31) occurs, the FIFO buffer will be cleared, the FIFO fill level indication register FIFO_FRAME_COUNTER (0x0E<6:0>) will be cleared, and the FIFO_OR (0x0E<7>) will be cleared.

As mentioned, FIFO controller contains two interrupts, FIFO_FULL interrupt, and watermark interrupt. These two interrupts are functional in all the FIFO operating modes.
The watermark interrupt is triggered when the fill level of buffer reached to the level that is defined by register FIFO_WM_TRIGGER (0x31<5:0>), if the interrupt is enabled by setting INT_FWM_EN (0x17<6>) to logic 1 and INT1_FWM (0x1A<1>) or INT2_FWM (0x1A<6>) is set.
The FIFO_FULL interrupt is triggered when the buffer has been fully filled. In FIFO mode, the fill level is 32, and in STREAM mode the fill level is 31, in BYPASS mode the fill level is 1. To enable the FIFO_FULL interrupt, INT_FFULL (0x17<5>) should be set to 1, and INT1_FFULL (0x1A<2>) or INT2_FFULL (0x1A<7>) should be set to 1.
The status of watermark interrupt and fifo full interrupt can be read through INT_STAT (0x0A).
After soft-reset, the watermark interrupt and FIFO full interrupt are disabled.

For the FIFO to recollect the data, user should reconfigure the register FIFO_MODE. (consult with app team)

7.9 Interrupt configuration

The device has the above 8 interrupt engines. Each of the interrupts can be enabled and configured independently. If the trigger condition of the enabled interrupt fulfilled, the corresponding interrupt status bit will be set to logic 1, and the mapped interrupt pin will be activated. The device has two interrupt PINs, INT1 and INT2. Each of the interrupts can be mapped to either PIN or both PINs.
The interrupt status registers update when a new data word is written into the data registers. If an interrupt is disabled, the related active interrupt status bit is disabled immediately.

The interrupt sequence is like the following
New data conversion, with or without filtering, judge the interrupt condition, new data written to data register, update interrupt status registers, trig associated interrupts, set mapped interrupt PINs, clear interrupts (depending on the interrupt mode), waiting for next data conversion.

Device supports 2 interrupt modes, non-latched, and latched mode. The interrupt modes are set through LATCH_INT (0x21<0>).
In non-latched mode, the interrupt status bit and the mapped interrupt pin are cleared as soon as the associated conditions are no more valid, or read operation to the INT_STAT (0x09~0x0b). Exceptions to this are the new data, orientation, and flat interrupts, which are automatically reset after a fixed time.
In latched mode, the clearings of the interrupt status and selected pin are determined by INT_RD_CLR (0x21<7>). If INT_RD_CLR=0, read operation to the INT_STAT will clear the interrupt and the selected pin. If INT_RD_CLR=1, any read operation to the device will clear the interrupt and the selected pin.
If the condition for trigging the interrupt still holds, the interrupt status will be set again with the next change of the data registers.

Mapping the interrupt pins can be set by INT_MAP (0x19~0x1B).
The electrical interrupt pins can be set INT_PIN_CONF (0x20<3:0>). The active logic level can be set to 1 or 0, and the interrupt pin can be set to open-drain or push-pull.

If the interrupt mode is configured as latched mode, the interrupt can also be cleared by I2C reading any of the interrupt status register (0x09 ~ 0x0c). (should confirm with application team, check 0x21<7>)

8 I²C COMMUNICATION PROTOCOL

8.1 I²C Timings

Below table and graph describe the I²C communication protocol times

Table 9. I2C Timings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL Clock	f_{scl}		0		400	kHz
SCL Low Period	t_{low}		1			μS
SCL High Period	t_{high}		1			μS
SDA Setup Time	t_{sudat}		0.1			μS
SDA Hold Time	t_{hddat}		0		0.9	μS
Start Hold Time	t_{hdsta}		0.6			μS
Start Setup Time	t_{susta}		0.6			μS
Stop Setup Time	t_{susto}		0.6			μS
New Transmission Time	t_{buf}		1.3			μS
Rise Time	t_r					μS
Fall Time	t_f					μS

Figure 12. I²C Timing Diagram

8.2 I²C R/W Operation

8.2.1 Abbreviation

Table 10. Abbreviation

SACK	Acknowledged by slave
MACK	Acknowledged by master
NACK	Not acknowledged by master
RW	Read/Write

8.2.2 Start/Stop/Ack

START: Data transmission begins with a high to transition on SDA while SCL is held high. Once I²C transmission starts, the bus is considered busy.
STOP: STOP condition is a low to high transition on SDA line while SCL is held high.
ACK: Each byte of data transferred must be acknowledged. The transmitter must release the SDA line during the acknowledge pulse while the receiver mush then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.
NACK: If the receiver doesn't pull down the SDA line during the high period of the acknowledge clock cycle, it's recognized as NACK by the transmitter.

8.2.3 I²C Write

I²C write sequence begins with start condition generated by master followed by 7 bits slave address and a write bit (R/W=0). The slave sends an acknowledge bit (ACK=0) and releases the bus. The master sends the one byte register address. The slave again acknowledges the transmission and waits for 8 bits data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol.

Table 11. I2C Write

START	Slave Address							R W	SACK	Register Address (0x11)								SACK	Data (0x80)								SACK	STOP
	0	0	1	0	0	1	0	0		0	0	0	1	0	0	0	1		1	0	0	0	0	0	0	0		

8.2.4 I²C Read

I²C write sequence consists of a one-byte I²C write phase followed by the I²C read phase. A start condition must be generated between two phase. The I²C write phase addresses the slave and sends the register address to be read. After slave acknowledges the transmission, the master generates again a start condition and sends the slave address together with a read bit (R/W=1). Then master releases the bus and waits for the data bytes to be read out from slave. After each data byte the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACK from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a STOP condition and terminate the transmission.
The register address is automatically incremented and more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified in the current I²C write command.

Table 12. I2C Read

START	Slave Address							R W	SACK	Register Address (0x00)								SACK										
	0	0	1	0	0	1	0	0		0	0	0	0	0	0	0	1											
START	Slave Address							R W	SACK	Data (0x00)								MACK	Data (0x01)									
	0	0	1	0	0	1	0	1		0	0	0	0	0	0	1	0		0	0	0	0	0	0	0	0		
MACK	Data (0x02)								MACK	…….								MACK	Data (0x07)								NACK	STOP
	0	0	0	0	0	0	1	0		…….									0	0	0	0	0	0	0	0		

9 REGISTERS

9.1 Register Map

The table below provides a list of the 8-bit registers embedded in the device and their respective function and addresses

Table 13. Register Map

Addr	Name	Description	B7	B6	B5	B4	B3	B2	B1	B0	Default	R/W
0x00	CHIP_ID	CHIP ID	For product version								0xB0	RW
0x01	DXL	LSB of X data	DX<1:0>							NEW_DATA_X	0x00	R

0x02	DXM	MSB of X data	DX<9:2>							0x00	R
0x03	DYL	LSB of Y data	DY<1:0>						NEW_DATA_Y	0x00	R
0x04	DYM	MSB of Y data	DY<9:2>							0x00	R
0x05	DZL	LSB of Y data	DZ<1:0>						NEW_DATA_Z	0x00	R
0x06	DZM	MSB of Y data	DZ<9:2>							0x00	R
0x07	STEP_CNT	LSB	STEP_CNT_LSB							0x00	RW
0x08		MSB	STEP_CNT_MSB							0x00	RW
0x09	INT_STAT									0xFF	R
0x0a			FOB_INT	ORIENT_INT	S_TAP_INT	D_TAP_INT	STEP_INT	STEP_QUIT_INT	STEP_UNSIMILAR		0x00	R
0x0b				FIFO_WM_INT	FIFO_FULL_INT	DATA_INT	LOW_INT	HIGH_INT			0x00	R
0x0c			TAP_SIGN	TAP_FIRST_Z	TAP_FIRST_Y	TAP_FIRST_X	HIGH_SIGN	HIGH_FIRST_Z	HIGH_FIRST_Y	HIGH_FIRST_X	0x00	R
0x0d			STEP_CNT_OVFL			FOB<1:0>		ORIENT<2:0>			0x00	R
0x0e	FIFO_STAT		FIFO_OR	FIFO_FRAME_COUNTER<6:0>							0x00	R
0x0f	RANGE						RANGE<3:0>				0x00	RW
0x10	BW				ODRH	BW<4:0>					0x00	RW
0x11	POWER		MODE_BIT	DSLP	PRESET<1:0>		SLEEP_DUR<3:0>				0x00	RW
0x12	STEP_CONF		STEP_START			STEP_SAMPLE_COUNT<4:0>					0x0C	RW
0x13			STEP_CLR	STEP_PRECISION<6:0>							0x00	RW
0x14			STEP_TIME_LOW								0x00	RW
0x15			STEP_TIME_UP								0xFF	RW
0x16	INT_EN		FOB_EN	ORIENT_EN	S_TAP_EN	D_TAP_EN	STEP_EN	STEP_QUIT_EN	STEP_UNSIMILAR_EN		0x00	RW
0x17				INT_FWM_EN	INT_FFULL_EN	DATA_EN	LOW_EN	HIGH_EN_Z	HIGH_EN_Y	HIGH_EN_X	0x00	RW
0x18				INT_SRC_STEP	INT_SRC_DATA	INT_SRC_TAP					0x00	RW
0x19	INT_MAP		INT1_FOB	INT1_ORIENT	INT1_S_TAP	INT1_D_TAP	INT1_STEP	INT1_STEP_QUIT	INT1_STEP_UNSIMIL		0x00	RW
0x1A				INT1_FWM	INT1_FFULL	INT1_DATA	INT1_LOW	INT1_HIGH			0x00	RW
0x1B			INT2_FOB	INT2_ORIENT	INT2_S_TAP	INT2_D_TAP	INT2_STEP	INT2_STEP_QUIT	INT2_STEP_UNSIMIL		0x00	RW
0x1C				INT2_FWM	INT2_FFULL	INT2_DATA	INT2_LOW	INT2_HIGH			0x00	RW
0x1D											0x00	RW
0x1E			PEAK_B<5:0>						STEP_MISMATCH_B<1:0>		0x00	RW
0x1F			VALLEY_B<5:0>								0x00	RW
0x20	INTPIN_CFG	Interrupt PIN configuration					INT2_OD	INT2_LVL	INT1_OD	INT1_LVL	0x05	RW
0x21	INT_CFG	Interrupt configuration	INT_RD_CLR	SHADOW_DIS	INT_PULSE					LATCH_INT	0x00	RW
0x22	LOW_HIGH_G		LOW_DUR								0x09	RW
0x23			LOW_TH								0x30	RW
0x24			HIGH_HYST<1:0>				LOW_MODE	LOW_HYST<1:0>			0x81	RW
0x25			HIGH_DUR								0x0F	RW
0x26			HIGH_TH								0xC0	RW
0x27	OS_CUST		OS_CUST_X								0x00	RW
0x28			OS_CUST_Y								0x00	RW
0x29			OS_CUST_Z								0x00	RW
0x2A	TAP		TAP_QUIET	TAP_SHOCK				TAP_DUR<2:0>			0x04	RW

0x2B					TAP_TH<4:0>							0x0A	RW
0x2C	4D6D		PL_Z_TH									0x00	RW
0x2D			UD_X_TH									0xA4	RW
0x2E			RL_Z_TH									0x00	RW
0x2F			RL_Y_TH									0xA4	RW
0x30			ORIENT_DB_DIS	FB_Z_TH<6:0>								0x00	RW
0x31	FIFO_WTMK	FIFO water mark level			FIFO_WTMK_LVL<5:0>							0x00	RW
0x32	ST_CFG		SELFTEST_BIT			SELFTEST_AMP/EN_PK_VLY	SINGLE_EN_STEP	SELFTESET_SIGN	SELFTEST_AXIS<1:0>			0x00	RW
0x33	NVM_CFG		UNLOCK_3F				NVM_LOAD	NVM_RDY	NVM_PROG			0x04	RW
0x34			VALLEY_A<5:0>									0x00	RW
0x35			PEAK_A<5:0>						STEP_MISMATCH_A<1:0>			0x00	RW
0x36	SR	Soft reset	SOFT_RESET: 0xB6, NVM_UNLOCK: 0xB3									0x00	RW
0x37	TRIM		OFFSET_X<10:8>			GAIN_Z<9:8>		OFFSET_Y<10:8>				NVM	RW
0x38			OFFSET_X<7:0>									NVM	RW
0x39			OFFSET_Y<7:0>									NVM	RW
0x3A			OFFSET_Z<7:0>									NVM	RW
0x3B			GAIN_X									NVM	RW
0x3C			GAIN_Y									NVM	RW
0x3D			GAIN_Z<7:0>									NVM	RW
0x3E	FIFO_CFG	FIFO configuration	FIFO_MODE<1:0>						FIFO_CH<1:0>			0x00	RW
0x3F	FIFO	FIFO register	FIFO_DATA									0x00	R

9.2 Register Definition

Register 0x00 (CHIP ID)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
Device ID								RW	

This register is used to identify the device

Register 0x01 ~ 0x02 (DXL, DXM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
DX<1:0>							NEWDATA_X	R	0x00
DX<9:2>								R	0x00

DX: 10bits acceleration data of x-channel. This data is in two's complement.
NEWDATA_X: 1, acceleration data of x-channel has been updated since last reading
0, acceleration data of x-channel has not been updated since last reading

Register 0x03 ~ 0x04 (DYL, DYM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
DY<1:0>							NEWDATA_Y	R	0x00
DY<9:2>								R	0x00

DY: 10bits acceleration data of y-channel. This data is in two's complement.
NEWDATA_Y: 1, acceleration data of y-channel has been updated since last reading
0, acceleration data of y-channel has not been updated since last reading

Register 0x05 ~ 0x06 (DZL, DZM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
DZ<1:0>							NEWDATA_Z	R	0x00
DZ<9:2>								R	0x00

DZ: 10bits acceleration data of z-channel. This data is in two's complement.
NEWDATA_Z: 1, acceleration data of z-channel has been updated since last reading
0, acceleration data of z-channel has not been updated since last reading

Register 0x07 ~ 0x08 (ID)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_CNT_LSB								R	0x00
	STEP_CNT_MSB							R	0x00

STEP_CNT_LSB The least significant 8 bits of step count
STEP_CNT_LSB: The most significant 8 bits of step count

Register 0x0a (INT_STAT0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FOB_INT	ORIENT_INT	S_TAP_INT	D_TAP_INT	STEP_INT	STEP_QUIT_INT	STEP_UNSIMILAR		R	0x00

FOB_INT: 1, front-back interrupt active
0, front-back interrupt inactive
ORIENT_INT: 1, orient interrupt active
0, orient interrupt inactive
S_TAP_INT: 1, single tap interrupt active
0, single tap interrupt inactive
D_TAP_INT: 1, double tap interrupt active
0, double tap interrupt inactive
STEP_INT: 1, step valid interrupt is active
0, step valid interrupt is inactive
STEP_QUIT_INT: 1, step quit interrupt is active
0, step quit interrupt is inactive
STEP_UNSIMILAR: 1, step unsimilar interrupt is active
0, step unsimilar interrupt is inactive

Register 0x0b (INT_STAT1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	FIFO_WM_INT	FIFO_FULL_INT	DATA_IINT T	LOW_INT	HIGH-INT			R	0x00

This register indicates interrupt status related to data ready, FIFO watermark, and FIFO full.

FIFO_WM_INT: 1, FIFO watermark interrupt active
0, FIFO watermark interrupt inactive
FIFO_FULL_INT: 1, FIFO full interrupt active
0, FIFO full interrupt inactive
DATA_INT: 1, data ready interrupt active
0, data ready interrupt inactive

LOW_INT: 1, low-g interrupt active
0, low-g interrupt inactive
HIGH_INT: 1, high-g interrupt active
0, high-g interrupt inactive

Register 0x0c (INT_STAT2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
TAP_SIGN	TAP_FIRST_Z	TAP_FIRST_Y	TAP_FIRST_X	HIGH_SIGN	HIGH_FIRST_Z	HIGH_FIRST_Y	HIGH_FIRST_X	R	0x00

TAP_SIGN: 1, sign of tap triggering is negative
0, sign of tap triggering signal is positive
TAP_FIRST_Z: 1, tap interrupt is triggered by Z axis
0, tap interrupt is not triggered by Z axis
TAP_FIRST_Y: 1, tap interrupt is triggered by Y axis
0, tap interrupt is not triggered by Y axis
TAP_FIRST_X: 1, tap interrupt is triggered by X axis
0, tap interrupt is not triggered by X axis
HIGH_SIGN: 1, sign of high-g triggering signal is negative
0, sign of high-g triggering signal is positive
HIGH_FIRST_Z: 1, high-g interrupt is triggered by Z axis
0, high-g interrupt is not triggered by Z axis
HIGH_FIRST_Y: 1, high-g interrupt is triggered by Y axis
0, high-g interrupt is not triggered by Y axis
HIGH_FIRST_X: 1, high-g interrupt is triggered by X axis
0, high-g interrupt is not triggered by X axis

Register 0x0d (INT_STAT3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_CNT_OVFL			FOB<1:0>		ORIENT<2:0>			R	0x00

STEP_CNT_OVFL: 1, step counter is over-flowed
0, step counter is not over-flowed

FOB<1:0>: 00, device is in unknown orientation
01, device is in front orientation
10, device is in back orientation
11, reserved
ORIENT<2:0>: 000, device is in unknown orientation
001, device is in left orientation
010, device is in right orientation
011, reserved
100, reserved
101, device is in down orientation
110, device is in up orientation
111, reserved

Register 0x0e (FIFO_STATE)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FIFO_OR	FIFO_FRAME_COUNT<6:0>							R	0x00

FIFO_OR: 1, FIFO over run occurred
0, FIFO over run not occurred
FIFO_FRAME_COUNT<6:0>:
Fill level of FIFO buffer. An empty FIFO corresponds to 0x00. The frame counter can be cleared by reading out all of the frames, or by writing register 0x3e (FIFO_CFG1) or 0x31.

Register 0x0f (RANGE)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
				RANGE<3:0>				RW	0x00

RANGE<3:0>: set the full scale of the accelerometer. Setting as following

RANGE<3:0>	Acceleration range	Resolution
0001	2g	3.9mg/LSB
0010	4g	7.8mg/LSB
0100	8g	15.6mg/LSB
Others	Reserved	0.98mg/LSB

Register 0x10 (BW)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
		ODRH	BW<4:0>					RW	0x00

ODRH: 1, higher output data rate, ODR = 4*F_BW
0, lower output data rate, ODR = 2*F_BW
BW<4:0>: bandwidth setting, as following

BW<4:0>	F_BW (Bandwidth)	ODR (0x10<5>=0)	ODR (0x10<5>=1)
xx000	3.9Hz	7.8Hz	15.6Hz
xx001	7.8Hz	15.6Hz	31.2Hz
xx010	15.6Hz	31.2Hz	62.5Hz
xx011	31.2Hz	62.5Hz	125Hz
xx100	62.5Hz	125Hz	250Hz
xx101	125Hz	250Hz	500Hz
xx110	250Hz	500Hz	1000Hz
xx111	500Hz	1000Hz	2000Hz

Even if unfiltered data is used, the ODR is still set by BW value.

Register 0x11 (POWER)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
MODE_BIT	DSLP	PRESET<1:0>		SLEEP_DUR<3:0>				RW	0x00

MODE_BIT: 1, set device into active mode
0, set device into standby mode

DSLP: 1, enable deep sleep. This action can lower down the power consumption more
0, disable deep sleep

PRESET<1:0>: Preset time setting. The preset time is reserved for CIC filter in digital
11, Tpreset=2048us
10, Tpreset=768us
01, Tpreset=96us
00, Tpreset=12us

SLEEP_DUR<3:0>: Set the sleep time, when device is in power cycling power saving.

SLEEP_DUR<3:0>	Sleep time Tsl
0000	No power cycling / full speed
0001~0101	0.5ms
0110	1ms
0111	2ms
1000	4ms
1001	6mS
1010	10mS
1011	25mS
1100	50mS
1101	100mS
1110	500ms
1111	1s

Register 0x12 (STEP_CONF0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_START			STEP_SAMPLE_COUNT<4:0>					RW	0x0C

STEP_START: start step counter, this bit should be set when using step counter

STEP_SAMPLE_COUNT<4:0>:
sample count setting for dynamic threshold calculation. The actual value is STEP_SAMPLE_COUNT<4:0>*4, default is 0xC, 48 sample count

Register 0x13 (STEP_CONF1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_CLR	STEP_PRECISION<6:0>							RW	0x00

STEP_CLR: clear step count in register 0x7 and 0x8

STEP_PRECISION<6:0>:
threshold for acceleration change of two successive sample which is used to update sample_new register in step counter, the actual g value is TEP_PRECISION<6:0>*3.9mg

Register 0x14 (STEP_CONF2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_TIME_LOW								RW	0x00

STEP_TIME_LOW: the short time window for a valid step, the actual time is STEP_TIME_LOW<7:0>*ODR

Register 0x15 (STEP_CONF3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_TIME_UP								RW	0x00

STEP_TIME_UP: time window for quitting step counter, the actual time is STEP_TIME_UP<7:0>*8*ODR

Register 0x16 (INT_EN0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FOB_EN	ORIENT_EN	S_TAP_EN	D_TAP_EN	STEP_EN	STEP_QUIT_EN	STEP_UNSIMILAR_EN		RW	0x00

FOB_EN: 1, enable front-and-back orientation interrupt
0, disable front-and-back orientation interrupt
ORIENT_EN: 1, enable 4D orientation interrupt
0, disable 4D orientation interrupt
S_TAP_EN: 1, enable single tap interrupt
0, disable single tap interrupt
D_TAP_EN: 1, enable double tap interrupt
0, disable double tap interrupt
STEP_EN: 1, enable step valid interrupt
0, disable step valid interrupt
STEP_QUIT_EN: 1, enable step quit interrupt
0, disable step quit interrupt
STEP_UNSIMILAR_EN:
1, enable step unsimilar interrupt
0, disable step unsimilar interrupt

Register 0x17 (INT_EN1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	INT_FWM_EN	INT_FFULL_EN	DATA_EN	LOW_EN	HIGH_EN_Z	HIGH_EN_Y	HIGH_EN_X	RW	0x00

INT_FWM_EN: 1, enable FIFO watermark interrupt
0, disable FIFO watermark interrupt
INT_FFULL_EN: 1, enable FIFO full interrupt
0, disable FIFO full interrupt
DATA_EN: 1, enable data ready interrupt
0, disable data ready interrupt
LOW_EN: 1, enable low-g interrupt
0, disable low-g interrupt
HIGH_EN_Z: 1, enable high-g interrupt on Z axis
0, disable high-g interrupt on Z axis
HIGH_EN_Y: 1, enable high-g interrupt on Y axis
0, disable high-g interrupt on Y axis
HIGH_EN_X: 1, enable high-g interrupt on X axis
0, disable high-g interrupt on X axis

Register 0x18 (INT_SRC)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	INT_SRC_STEP	INT_SRC_DATA	INT_SRC_TAP					RW	0x00

INT_SRC_STEP: 1, select unfiltered data for step counter
0, select filtered data for step counter
INT_SRC_DATA: 1, select unfiltered data for new data interrupt and FIFO
0, select filtered data for new data interrupt and FIFO
INT_SRC_TAP: 1, select unfiltered data for TAP interrupt
0, select filtered data for TAP interrupt

Register 0x19 (INT_MAP0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
INT1_FOB	INT1_ORIENT	INT1_S_TAP	INT1_D_TAP	INT1_STEP	INT1_STEP_QUIT	INT1_STEP_UNSIMILAR		RW	0x00

INT1_FOB: 1, map FOB interrupt to INT1 pin
0, not map FOB interrupt to INT1 pin
INT1_ORIENT: 1, map ORIENT interrupt to INT1 pin
0, not map ORIENT interrupt to INT1 pin
INT1_S_TAP: 1, map single tap interrupt to INT1 pin
0, not map single tap interrupt to INT1 pin
INT1_D_TAP: 1, map double tap interrupt to INT1 pin
0, not map double tap interrupt to INT1 pin
INT1_STEP: 1, map step valid interrupt to INT1 pin
0, not map step valid interrupt to INT1 pin
INT1_STEP_QUIT: 1, map step quit interrupt to INT1 pin
0, not map step quit interrupt to INT1 pin
INT1_STEP_UNSIMILAR:
1, map step unsimilar interrupt to INT1 pin
0, not map step unsimilar interrupt to INT1 pin

Register 0x1a (INT_MAP1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	INT1_FWM	INT1_FFULL	INT1_DATA	INT1_LOW	INT1_HIGHs			RW	0x00

INT1_FWM: 1, map FIFO watermark interrupt to INT1 pin
0, not map FIFO watermark interrupt to INT1 pin
INT1_FFULL: 1, map FIFO full interrupt to INT1 pin
0, not map FIFO full interrupt to INT1 pin
INT1_DATA: 1, map data ready interrupt to INT1 pin
0, not map data ready interrupt to INT1 pin
INT1_LOW: 1, map low-g interrupt to INT1 pin
0, not map low-g interrupt to INT1 pin
INT1_HIGH: 1, map high-g interrupt to INT1 pin
0, not map high-g interrupt to INT1 pin

Register 0x1B (INT_MAP2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
INT2_FOB	INT2_ORIENT	INT2_S_TAP	INT2_D_TAP	INT2_STEP	INT2_STEP_QUIT	INT2_STEP_UNSIMILAR		RW	0x00

INT2_FOB: 1, map FOB interrupt to INT2 pin
0, not map FOB interrupt to INT2 pin
INT2_ORIENT: 1, map ORIENT interrupt to INT2 pin
0, not map ORIENT interrupt to INT2 pin
INT2_S_TAP: 1, map single tap interrupt to INT2 pin
0, not map single tap interrupt to INT2 pin
INT2_D_TAP: 1, map double tap interrupt to INT2 pin
0, not map double tap interrupt to INT2 pin
INT2_STEP: 1, map step valid interrupt to INT2 pin
0, not map step valid interrupt to INT2 pin
INT2_STEP_QUIT: 1, map step quit interrupt to INT2 pin
0, not map step quit interrupt to INT2 pin
INT2_STEP_UNSIMILAR:
1, map step unsimilar interrupt to INT2 pin
0, not map step unsimilar interrupt to INT2 pin

Register 0x1c (INT_MAP3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	INT2_FWM	INT2_FULL	INT2_DATA	INT1_STEP	INT2_LOW	INT2_HIGH		RW	0x00

INT2_FWM: 1, map FIFO watermark interrupt to INT2 pin
0, not map FIFO watermark interrupt to INT2 pin
INT2_FULL: 1, map FIFO full interrupt to INT2 pin
0, not map FIFO full interrupt to INT2 pin
INT2_DATA: 1, map data ready interrupt to INT2 pin
0, not map data ready interrupt to INT2 pin
INT2_LOW: 1, map low-g interrupt to INT2 pin
0, not map low-g interrupt to INT2 pin
INT2_HIGH: 1, map high-g interrupt to INT2 pin
0, not map high-g interrupt to INT2 pin

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Register 0x1e (VALLEY_B)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
VALLEY_B<5:0>								RW	0x00

VALLEY_B<5:0>: valley value of one axis which is used for step valley match

Register 0x1f (PEAK_B)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
PEAK_B<5:0>						STEP_MISMATCH_B<1:0>		RW	0x00

PEAK_B<5:0>: peak value of one axis which is used for step peak match
STEP_MISMATCH_B<1:0>:
precision for step peak and valley match
00, match VALLEY_B<5:1> and PEAK_B<5:1>
01, match VALLEY_B<5:2> and PEAK_B<5:2>
10, match VALLEY_B<5:3> and PEAK_B<5:3>
11, match VALLEY_B<5:4> and PEAK_B<5:4>

Register 0x20 (INTPIN_CFG)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
				INT2_OD	INT2_LVL	INT1_OD	INT1_LVL	RW	0x05

INT2_OD: 1, open-drain for INT2 pin
0, push-pull for INT2 pin
INT2_LVL: 1, logic high as active level for INT2 pin
0, logic low as active level for INT2 pin

INT1_OD: 1, open-drain for INT1 pin
0, push-pull for INT1 pin
INT1_LVL: 1, logic high as active level for INT1 pin
0, logic low as active level for INT1 pin

Register 0x21 (INT_CFG)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
INT_RD_CLR	SHADOW_DIS	INT_PULSE					LATCH_INT	RW	0x00

INT_RD_CLR: 1, clear all the interrupts in latched-mode, when any read operation to this device
0, clear all the interrupts, only when read the register INT_STAT (0x0A~0x0B), no matter the interrupts in latched-mode, or in non-latched-mode
SHADOW_DIS: 1, disable the shadowing function for the acceleration data
0, enable the shadowing function for the acceleration data. When shadowing is enabled, the MSB of the acceleration data is locked, when corresponding LSB of the data is reading. This can ensure the integrity of the acceleration data during the reading. The MSB will be unlocked when the MSB is read.
INT_PULSE: 1, data ready interrupt is kept until next conversion starts, in power cycling
0, pulse of data ready interrupt is fixed to be 128us
LATCH_INT: 1, interrupt is in latch mode
0, interrupt is in non-latch mode

Register 0x22 (LOW_HIGH_G_0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
LOW_DUR								RW	0x09

LOW_DUR: low-g interrupt triggered delay, the actual time is (LOW_DUR<7:0>+1)*2ms; the default delay time is 20ms

Register 0x23 (LOW_HIGH_G_1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
LOW_TH								RW	0x30

LOW_TH: low-g interrupt threshold, the actual g value is (LOW_TH<7:0>)*7.8mg; the default value is 375mg

Register 0x24 (LOW_HIGH_G_2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
HIGH_HYST<1:0>					LOW_MODE	LOW_HYST<1:0>		RW	0x81

HIGH_HYST<1:0>: hysteresis of high-g interrupt , the actual g value is (HIGH_HYST<1:0>)*125mg(2g range), (HIGH_HYST<1:0>)*250mg (4g range),(HIGH_HYST<1:0>)*500mg(8g range)
LOW_MODE: low-g interrupt mode, 0: single-axis mode, 1: sum mode
LOW_HYST<1:0>: hysteresis of low-g interrupt , the actual g value is (LOW_HYST<1:0>)*125mg, independent of the selected g range

Register 0x25 (LOW_HIGH_G_3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
HIGH_DUR								RW	0x0F

HIGH_DUR: high-g interrupt triggered delay, the actual time is (HIGH_DUR<7:0>+1)*2ms; the default delay time is 32ms

Register 0x26 (LOW_HIGH_G_4)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
HIGH_TH								RW	0xC0

HIGH_TH: high-g interrupt threshold, the actual g value is (HIGH_TH<7:0>)*7.8mg(2g range), (HIGH_TH<7:0>)*15.6mg(4g range), (HIGH_TH<7:0>)*31.2mg(8g range)

Register 0x27 (OS_CUST_X)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OS_CUST_X								RW	0x00

OS_CUST_X: offset calibration of X axis for user, the LSB depends on full-scale of the device which is 3.9mg in 2g range, 7.8mg in 4g range, 15.6mg in 8g range

Register 0x28 (OS_CUST_Y)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OS_CUST_Y								RW	0x00

OS_CUST_Y: offset calibration of Y axis for user, the LSB depends on full-scale of the device which is 3.9mg in 2g range, 7.8mg in 4g range, 15.6mg in 8g range

Register 0x29 (OS_CUST_Z)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OS_CUST_Z								RW	0x00

OS_CUST_Z: offset calibration of Z axis for user, the LSB depends on full-scale of the device which is 3.9mg in 2g range, 7.8mg in 4g range, 15.6mg in 8g range

Register 0x2a (TAP_CONF0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
TAP_QUIET	TAP_SHOCK				TAP_DUR<2:0>			RW	0x04

TAP_QUIET: tap quiet time, 1: 30ms, 0: 20ms
TAP_SHOCK: tap shock time, 1: 50ms, 0: 75ms

TAP_DUR<2:0>: the time window of the second tap event for double tap

TAP_DUR<2:0>	Duration of TAP_DUR
000	50ms
001	100ms
010	150ms
011	200ms
100	250ms
101	375ms
110	500ms
111	700ms

Register 0x2b (TAP_CONF1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
			TAP_TH<4:0>					RW	0x00

TAP_TH<4:0>: threshold of single/double tap interrupt, the actual g value is TAP_TH<4:0>*62.5mg (2g range), TAP_TH<4:0>*125mg(4g range), TAP_TH<4:0>*250mg(8g range)

Register 0x2c (4D6D_CONF0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
UD_Z_TH								RW	0x00

UD_Z_TH: Up/down z axis threshold, the actual g value is UD_Z_TH<7:0>*3.91mg+0.1g, independent of the selected g range

Register 0x2d (4D6D_CONF1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
UD_X_TH								RW	0xA4

UD_X_TH: Up/down x axis threshold, the actual g value is UD_X_TH<7:0>*3.91mg, independent of the selected g range, the default value is 0.64g, corresponding to 40 degree

Register 0x2e (4D6D_CONF2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
RL_Z_TH								RW	0x00

RL_Z_TH: Right/left z axis threshold, the actual g value is RL_Z_TH<7:0>*3.91mg+0.1g, independent of the selected g range

Register 0x2f (4D6D_CONF3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
RL_Y_TH								RW	0xA4

RL_Y_TH: Up/down x axis threshold, the actual g value is RL_Y_TH<7:0>*3.91mg, independent of the selected g range, the default value is 0.64g, corresponding to 40 degree

Register 0x30 (4D6D_CONF4)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
ORIENT_DB_DIS	FB_Z_TH<6:0>							RW	0x00

ORIENT_DB_DIS: 1: disable orient denounce time
0: enable orient denounce time

FB_Z_TH<6:0>: Front/back z axis threshold, the actual g value is FB_Z_TH<7:0>*3.91mg+0.1g, independent of the selected g range

Register 0x31 (FIFO_WTMK)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
		FIFO_WTMK_LVL<5:0>						RW	0x00

FIFO_WTMK_LVL<5:0>:
defines FIFO water mark level. Interrupt will be generated, when the number of entries in the FIFO exceeds FIFO_WTMK_LVL<5:0>. When the value of this register is changed, the FIFO_FRAME_COUNTER is reset to 0.

Register 0x32 (ST_CONF)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
SELFTEST_BIT			SELFTEST_AMP/En_Peak_Valley	SingleEn_Step	SELFTEST_SIGN	SELFTEST_AXIS<1:0>		RW	0x00

SELFTEST_BIT: 1, self-test enabled. When self-test enabled, a delay of 3ms is necessary for the value settling.
0, normal

SELFTEST_AMP/En_Peak_Valley:
This bit is multiple used by SELFTEST_AMP and En_Peak_Valley,
When used as SELFTEST_AMP:
1, set high amplitude for self-test force
0, set low amplitude for self-test force
When used as En_Peak_Valley:
1, enable Peak and Valley match in step counter
0, disable Peak and Valley match in step counter

SingleEn_Step: 1, enable single axis mode in step counter
0, disable single axis mode in step counter

SELFTEST_SIGN: 1, set self-test excitation positive

0, set self-test excitation negative

SELFTEST_AXIS<1:0>:

These two bits are used to select axis for selftest or step counter
When SELFTEST_BIT (0x32<7>) is enabled:
00, x axis
01, y axis
10, z axis
11, z axis
When STEP_EN (0x16<3>) is enabled,
00, x axis
01, y axis
10, z axis
11, z axis
When STEP_EN (0x16<3>) and SingleEn_Step (0x32<3>) is enabled,
00, x axis
01, y axis
10, z axis
11, z axis

Register 0x34 (VALLEY_A)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
VALLEY_A<5:0>								RW	0x00

VALLEY_A<5:0>: valley value of one axis which is used for step valley match

Register 0x1f (PEAK_A)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
PEAK_A<5:0>						STEP_MISMATCH_A<1:0>		RW	0x00

PEAK_A<5:0>: peak value of one axis which is used for step peak match

STEP_MISMATCH_A<1:0>:

precision for step peak and valley match
00, match VALLEY_A<5:1> and PEAK_A<5:1>
01, match VALLEY_A<5:2> and PEAK_A<5:2>
10, match VALLEY_A<5:3> and PEAK_A<5:3>
11, match VALLEY_A<5:4> and PEAK_A<5:4>

Register 0x33 (NVM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
UNLOCK_3F				NVM_LOAD	NVM_RDY	NVM_PROG		RW	0x04

UNLOCK_3F: 1, unlock the burst-reading of FIFO. The burst-reading can access registers behind 0x3F. This option is reserved for internal test.
0, lock the burst-reading of FIFO. The register address will be locked at 0x3F, for normal use.

NVM_LOAD: 1, trigger loading register from NVM
0, not trigger loading register form NVM
This bit is cleared when NVM loading is done

NVM_RDY: 1, NVM is ready, loading or programing NVM is done
0, NVM is not ready, loading or programming NVM is in progress.
NVM_RDY is read-only to customer.

NVM_PROG: 1, trigger programing NVM
0, not trigger programming NVM
This bit is cleared when NVM programming is done

Register 0x36 (SR)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
SOFT_RESET								RW	0x00

SOFT_RESET: 0xB6, reset all of the registers
0xB3, unlock NVM for programming (not open to customer)
This register is cleared when reset or NVM programming is done

Register 0x37 (OFFSET_XY)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OFFSET_X<10:8>			GAIN_Z<9:8>		OFFSET_Y<10:8>			RW	NVM

OFFSET_X<10:8>: offset value of x-channel. This data is the trimming data for x channel in FT phase, together with OFFSET_X<7:0> in 0x38.
GAIN_Z<9:8>: sensitivity trimming bits for z channel, together with GAIN_Z<7:0> in 0x3D (total 10 bits).
OFFSET_Y<10:8>: offset value of y-channel. This data is the trimming data for y channel in FT phase, together with OFFSET_Y<7:0> in 0x39.

Register 0x38 (OFFSET_X)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OFFSET_X<7:0>								RW	NVM

OFFSET_X<7:0>: offset value of x-channel. This data is the trimming data for x channel in FT phase, together with OFFSET_X<10:8> in 0x37<7:5>.
The trimming LSB is 4mg, the full trimming range in digital domain is +-4g
User can perform read-modify-write access, to change the register value. However, when device is re-power-on, or soft-reset, this value will be updated to default again.

Register 0x39 (OFFSET_Y)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OFFSET_Y<7:0>								RW	NVM

OFFSET_Y<7:0>: offset value of y-channel. This data is the trimming data for y channel in FT phase, together with OFFSET_Y<10:8> in 0x37<2:0>. The trimming LSB is 4mg, the full trimming range in digital domain is +-4g
User can perform read-modify-write access, to change the register value. However, when device is re-power-on, or soft-reset, this value will be updated to default again.

Register 0x3a (OFFSET_Z)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OFFSET_Z<7:0>								RW	NVM

OFFSET_Z<7:0>: offset value of z-channel. This data is the trimming data for z channel in FT phase, together with OFFSET_Z<11:8> in 0x45<3:0>. The trimming LSB is 4mg, the full trimming range in digital domain is +-8g
User can perform read-modify-write access, to change the register value. However, when device is re-power-on, or soft-reset, this value will be updated to default again.

Register 0x3b (GAIN_X) not open to customer

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
GAIN_X								RW	NVM

GAIN_X: sensitivity trimming bits for x channel (total 8 bits).
Gain_total = (256 + GAIN_X) / 256
Gain rang is from 1 to 2, the worst gain accuracy is 1/256 ~= 0.4%

Register 0x3c (GAIN_Y) not open to customer

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
GAIN_Y								RW	NVM

GAIN_Y: sensitivity trimming bits for y channel (total 8 bits).
Gain_total = (256 + GAIN_Y) / 256
Gain rang is from 1 to 2, the worst gain accuracy is 1/256 ~= 0.4%

Register 0x3d (GAIN_Z) not open to customer

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
GAIN_Z<7:0>								RW	NVM

GAIN_Z: sensitivity trimming bits for z channel, together with GAIN_Z<9:8> in 0x37<4:3> (total 10 bits).
Gain_total = (128 + GAIN_Z) / 256
Gain rang is from 0.5 to 4.5, the worst gain accuracy is 1/128 ~= 0.8%

Register 0x3e (FIFO_CFG)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FIFO_MODE<1:0>						FIFO_CH<1:0>		RW	0x00

FIFO_MODE<1:0>: FIFO_MODE defines FIFO mode of the device. Settings as following

FIFO_MODE<1:0>	Mode
11	FIFO
10	STREAM
01	FIFO
00	BYPASS

FIFO_CH<1:0>: FIFO_CH defines which channel data be stored in FIFO buffer. Setting as following
11, only z axis data be stored in FIFO buffer
10, only y axis data be stored in FIFO buffer
01, only x axis data be stored in FIFO buffer
00, all axes data be stored in FIFO buffer

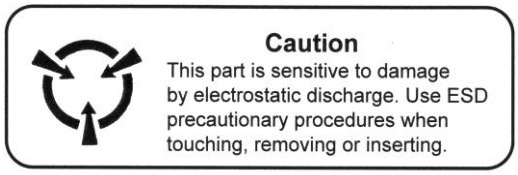
Register 0x3f (FIFO_DATA)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FIFO_DATA								R	0x00

FIFO_DATA: FIFO read out data. User can read out FIFO data through this register. Data format depends on the setting of FIFO_CH (0x3e<1:0>).
When the FIFO data is the LSB part of acceleration data, and if FIFO is empty, then FIFO_DATA<0> is 0. Otherwise if FIFO is not empty and the data is effective, FIFO_DATA<0> is 1 when reading LSB of acceleration.

ORDERING INFORMATION

Ordering Number	Temperature Range	Package	Packaging
QMA6981-TR	-40℃~85℃	LGA-12	Tape and Reel: 5k pieces/reel



CAUTION: ESDS CAT. 1B

FIND OUT MORE

For more information on QST's Accelerometer Sensors contact us at 86-21-50497300.

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ISO9001 : 2008

China Patents 201510000399.8, 201510000425.7, 201310426346.3, 201310426677.7, 201310426729.0, 201210585811.3 and 201210553014.7 apply to the technology described.

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