QN8007B/8007LB

High Performance Digital FM Transmitter for Portable Devices

General Description

The QN8007 is a high performance, low power, full-featured single-chip stereo FM transmitter designed for portable audio/video players, automotive accessories, cell phones, and GPS personal navigation devices. It integrates transmitting functions, clear channel scan, and antenna tuning to ease matching in real applications. Advanced digital architecture enables variable input gain programming; selectable pre-emphasis, precision low-spur MPX stereo encoding and pilot tone generation, low-noise PLL-based modulation, and an on-chip power amplifier with variable output level and RF band-pass filtering to ensure optimum transmit spectrum purity.

With its small footprint, minimal external component count and multiple clock frequency support, the QN8007 is easy to integrate into a variety of small form-factor low power portable applications. An integrated voltage regulator enables direct connection to a battery and provides high PSRR for superior noise suppression. A low-power Standby mode extends battery life. ESD protection is on all pins. The QN8007 is fabricated in highly reliable CMOS technology.

Key Features

- **Worldwide FM Band Transmit**
  - *76 MHz to 108 MHz full band tuning in 50/100/200 kHz step sizes*
  - *50/75µs pre-emphasis*
- **High Performance FM Transmitter (FMT)**
  - *66dB Stereo SNR, 0.03% THD*
  - *Maximum 121dBµV RF output level with 42dB adjustable range*
  - *Integrated Clear Channel Scan*
- **RDS/RBDS Transmit**
  - *Supports US and European data service, including TMC (Traffic Messaging Channel) (not available in QN8007L)*
- **Flexible Audio Interfaces**
  - *Digital audio interface supports I²S and a variety of PCM data formats with 4 different data rates*
  - *Programmable analog audio input/output*
  - *Integrated audio AGC and soft clipping*
- **Very Low Power Consumption**
  - *9.2 mA*
  - *Integrated voltage regulator, direct connect to battery*
  - *Power saving idle and standby modes*
  - *Low shutdown leakage current*
- **Ease of Integration**
  - *Small footprint, 4 x 4 x 0.85mm QFN24*
  - *Only 2 external passive components required*
  - *Adaptive antenna tuning*
  - *Low cellular and GPS band spurs*
  - *High Immunity to TDMA (GSM/GPRS) burst noise*
  - *Multiple crystal frequencies supported*
  - *2-wire and 3-wire control interfaces*
- **Robust Operation**
  - *-25^{0}C to +85^{0}C operation*
  - *ESD protection on all input and output pads*

Typical Applications

- Cell Phones / PDAs / Smart Phones
- Portable Audio & Media Players
- GPS Personal Navigation Devices
- Automotive and Accessories

CONTENTS

REVISION HISTORY

REVISION	CHANGE DESCRIPTION	DATE
1.0	Datasheet Release	06/12/08
2.0	B1 Register set incorporated, INT pin added to Figure 1.	8/26/08
2.01	1. Table 3 Vcc range:2.7~5.0 v, TYP:3.3 v; 2. In Section 4.1: Modify 124 to 121dBµVp. 3. In Section 4.4: Delete" When there is no audio signal for a pre-determined period, AGC will power down the transmitter. "	03/17/09
2.02	Modify Figure1, Figure 2 and the pictures in Section 6.3: Pin20, should be DIN not DIN/INT	05/12/09
2.03	Add the Register STATUS2(RO) Address 1Bh	06/02/09
2.04	Update the data in Table 4 and Table 6.	06/19/09
2.05	Modify the register PWROUT_CAL→ PAC_TARGET and the description	07/30/09
2.06	Update the registers in Section 7.	08/05/09
2.07	Modify t_{dtHD} MIN 100 ns→20 ns in table 8	09/09/09
2.08	Modify the description of register PAC_TARGET	10/12/09
2.09	1. Modify I^2C to 2-wire; 2. Add Reg 59h, Reg 5Ah. 3. Update the grammar and syntax. 4. Modify V_{ain} Max value: 1400 mV→2000 mV	11/19/09

STATEMENT:

Users are responsible for compliance with local regulatory requirements for low power unlicensed FM broadcast operation. Quintic is not responsible for any violations resulting from user's intentional or unintentional breach of regulatory requirements in personal or commercial use.

1 FUNCTIONAL BLOCK DIAGRAM

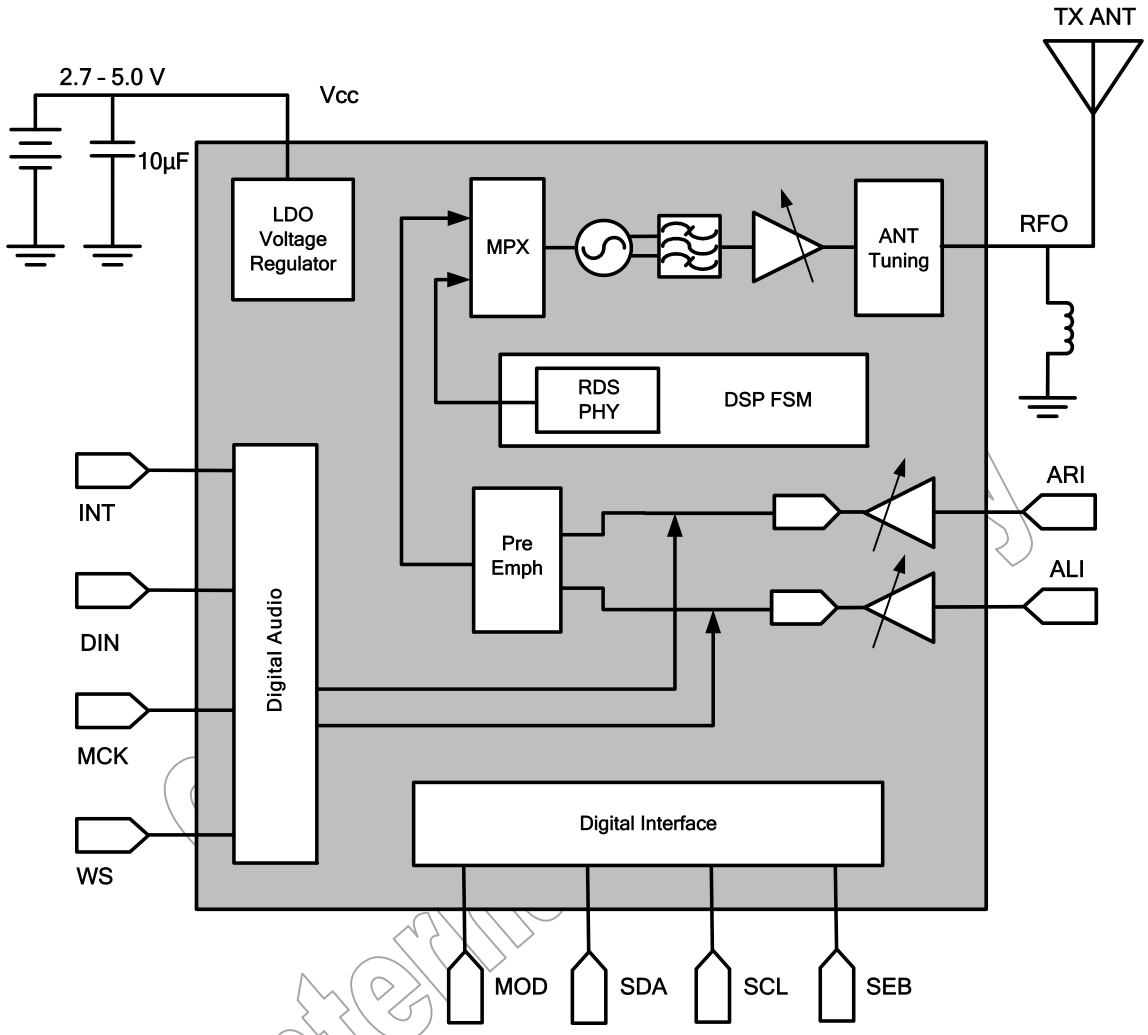


Figure 1: QN8007 Functional Blocks

2 PIN ASSIGNMENTS

(Top View)

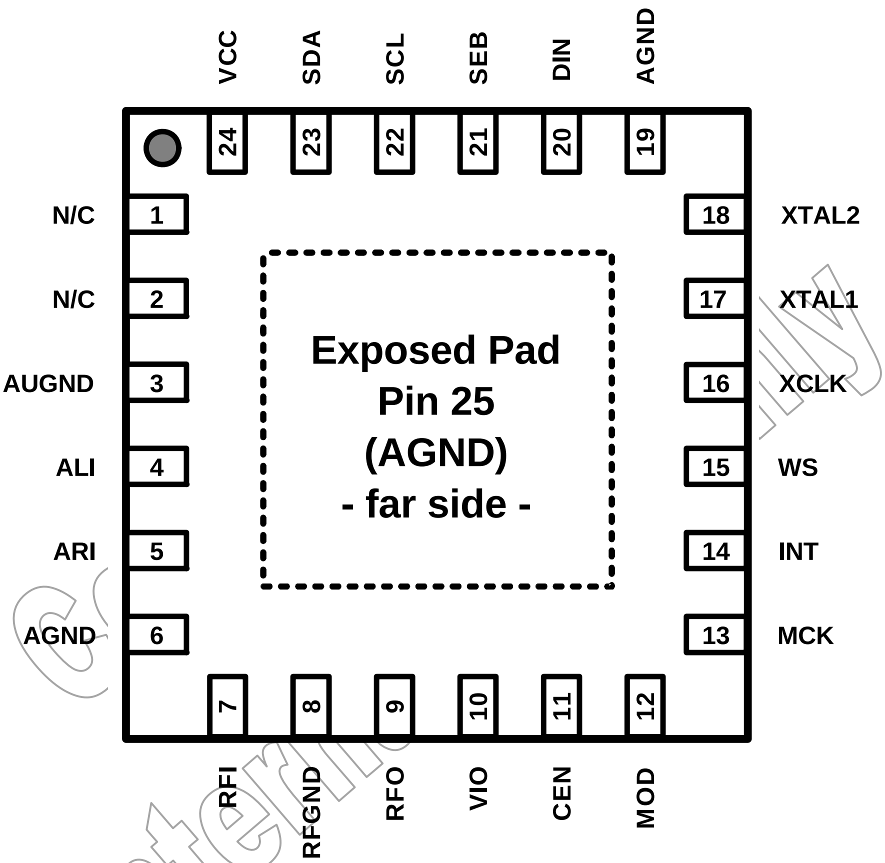


Figure 2: QN8007B Device Pin Out

Table 1: Pin Descriptions

PINS	NAME	DESCRIPTION
1	N/C	No connect
2	N/C	No connect
3	AUGND	Audio ground
4	ALI	Analog audio input – left channel
5	ARI	Analog audio input – right channel
6	AGND	Analog ground
7	RFI	Receiver RF input
8	RFGND	RF ground
9	RFO	Transmitter RF output – connect to matched antenna.
10	VIO	IO voltage – specifies voltage limit for all digital pins.
11	CEN	Chip enable: Chip power down if less than 0.6V, (see also MOD pin below) power up if voltage applied >min (0.7*VIO, 1.8V).
12	MOD	Bus mode: HIGH = 3-wire serial operation. LOW = 2-wire serial operation Note: Both MOD=0 and CEN=0 to disable chip.
13	MCK	Master clock – for digital audio interface.
14	INT	Interrupt
15	WS	Word select (I^2S mode only)
16	XCLK	External clock input (register 49h, bit 4 must be HIGH)
17	XTAL1	On-chip crystal driver port 1. If using an external clock source, connect this pin to ground.
18	XTAL2	On-chip crystal driver port 2. If using an external clock source, connect this pin to ground.
19	AGND	Analog ground
20	DIN	Data in (I^2S mode only)
21	SEB	Serves as the bus enable pin in 3-wire serial mode; serves as the address select pin in 2-wire serial mode, SEB = Low for default address, SEB = High for register controlled address.
22	SCL	Clock for 2-wire or 3-wire serial bus.
23	SDA	Bi-directional data line for 2- or 3-wire serial bus.
24	VCC	Voltage supply
25	PAD	Exposed pad, must be soldered to the ground on the PCB.

3 ELECTRICAL SPECIFICATIONS

Table 2: Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{bat}	Supply voltage	VCC to GND	-0.3	5	V
V_{IO}	Logic signals	CEN, SEB, SCL, SDA, MOD, to GND	-0.3	3.6	V
T_s	Storage temperature		-55	+150	^oC

Table 3: Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Vcc	Supply voltage	VCC to GND	2.7	3.3	5.0	V
T_A	Operating temperature		-25		+85	^oC
V_{ain}	L/R channel input signal level	Single ended peak to peak voltage		1000	2000	mV
V_{io}	Digital I/O voltage		1.6		3.6	V

Table 4: DC Characteristics

(Vcc = 2.7 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V, f carrier=88 MHz and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{TX}	Transmit mode supply current[1]	digital audio interface		6.8		mA
		analog audio interface	9.2		12.9	mA
I_{IDLE}	Idle mode supply current	Idle mode		3.5		mA
I_{STBY}	Standby mode supply current	Standby mode		350		µA
I_{PDN}	Power down leakage current	power down		5	15	µA
Interface						
V_{OH}	High level output voltage		$0.9*V_{IO}$			V
V_{OL}	Low level output voltage				$0.1*V_{IO}$	V
V_{IH}	High level input voltage		1.7 or $0.7*V_{IO}$			V
V_{IL}	Low level input voltage				0.6	V

Notes:
1. Max: RFO output level is 121dBuVp, Min: RFO=82 dBµVp.

Table 5: AC Characteristics

(Vcc = 2.7 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
F_{xtal}	Crystal or Clock frequency	Real-Time Clock	7.6 - 38.4[1]			MHz
F_{xtal_err}	Crystal frequency accuracy	Over temperature, and aging	-20		20	ppm

Notes:
1. See also XSEL [3:0] (register 03h, bits 3:0).

Table 6: Transmitter Characteristics

(Vcc = 2.7 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V, f carrier=88 MHz and T_A = 25°C).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
R_{audio_in}	Audio input impedance	At pin ALI and ARI	10		80	kΩ
C_{audio_in}	Audio input capacitance[1]	At pin ALI and ARI		2	5	pF
G_{audio_In}	Audio input gain	RIN[1:0] = 01	-1.5		15	dB
ΔG_{audio_In}	Audio gain step	For any gain setting	0.5	1	1.5	dB
τ_{emph}	Pre-emphasis time constant[1]	PETC = 1	71.3	75	78.7	µs
		PETC = 0	47.5	50	52.5	
SNR_{audio_tx}	Tx audio SNR[3]	MONO, Δf = 22.5 kHz		65		dB
		STEREO, Δf = 67.5 kHz, Δf_{pilot} = 6.75 kHz		66		
THD_{audio_tx}	Tx audio THD[3]	STEREO, Δf = 67.5 kHz, Δf_{pilot} = 6.75 kHz		0.03	0.1	%
α_{LR_tx}	L/R separation [2, 3]		40	45		dB
B_{LR_tx}	L/R channel imbalance [1, 2]	L and R channel gain imbalance at 1 kHz offset from DC			1	dB
M_{pilot}	19 kHz pilot modulation [2, 3, 6]	Relative to 75 kHz deviation	7	9.0	15	%
SUP_{sub}	38 kHz sub-carrier [2, 3] suppression		70			dB
C_{tune}	Output capacitance tuning range		5		30	pF
P_{out}	RF output voltage swing[4]	RF Channel frequency = 88 MHz	82		121	dBµV
ΔG_{RF_Out}	Power gain step	Over process, temperature		1.5		dB
ΔP_{out}	Power gain flatness	Over 76 MHz ~ 108 MHz	-2		2	dB
P_{mask}	RF output spectrum mask[5]	120 kHz to 240 kHz offset		-50	-45	dBc
		240 kHz to 600 kHz offset		-55	-45	
		>600 kHz offset			-45	
F_{rf}	RF channel frequency		76		108	MHz
F_{ch}	Channel frequency step		50	100	200	kHz
F_{err}	Channel center frequency accuracy		-2		2	kHz
F_{perr}	Pilot Tone frequency accuracy[1]		-2		2	Hz
F_{pk}	Modulation peak frequency deviation			75		kHz

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT

Notes:
1. Guaranteed by design.
2. Stereo (ST_MO_TX = 0).
3. 1000mVp-p, 1 kHz tone at ALI pin, no input signal at ARI pin.
4. Into matched antenna (see application note for details).
5. Within operating band 76 MHz to 108 MHz.
6. Value set with GAIN_TXPLT [5:0] (reg. 0Fh, bits 5:0). The user must conform to local regulatory requirements for low-power unlicensed FM broadcast operation when setting this value.

Table 7: Timing Characteristics

(Vcc = 2.7 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
τ_{pup}	Chip power-up time [1]	From rising edge of CEN to PLL settled and transmitter ready for transmission.			0.6	Sec
τ_{astby}	Auto Standby time [2]	TMOUT [1:0] = 00		1		Min
		TMOUT [1:0] = 01		3		
		TMOUT [1:0] = 10		5		
		TMOUT [1:0] = 11		Never		
τ_{chsw}	Channel switching time[1]	From any channel to any channel.			0.1	Sec
Transmitter Timing						
τ_{wkup}	Wake-up time from standby to transmit			25	200	msec
τ_{CCS}	Clear channel scan time	Per channel.		5		msec

Notes:
1. Guaranteed by design.
2. Chip automatically goes from idle to standby mode; TMOUT = 11 equivalent to auto standby disabled.

Table 8: 2-Wire Interface Timing Characteristics

(Vcc = 2.7 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	2-wire clock frequency				400	kHz
t_{LOW}	Clock Low time		1.3			µs
t_{HI}	Clock High time		0.8			µs
t_{ST}	SCL input to SDA falling edge start [1,3]		0.6			µs
t_{STHD}	SDA falling edge to SCL falling edge start[3]		0.6			µs
t_{rc}	SCL rising edge[3]	Level from 30% to 70%			300	ns
t_{fc}	SCL falling edge[3]	Level from 70% to 30%			300	ns
t_{dtHD}	SCL falling edge to next SDA rising edge[3]		20			ns
t_{dtc}	SDA rising edge to next SCL rising edge[3]				900	ns
t_{stp}	SCL rising edge to SDA rising edge [2,3]		0.6			µs
t_w	Duration before restart[3]		1.3			µs
C_b	SCL, SDA capacitive loading[3]			10		pF

Notes:
1. Start signaling of 2-wire interface.
2. Stop signaling of 2-wire interface.
3. Guaranteed by design.

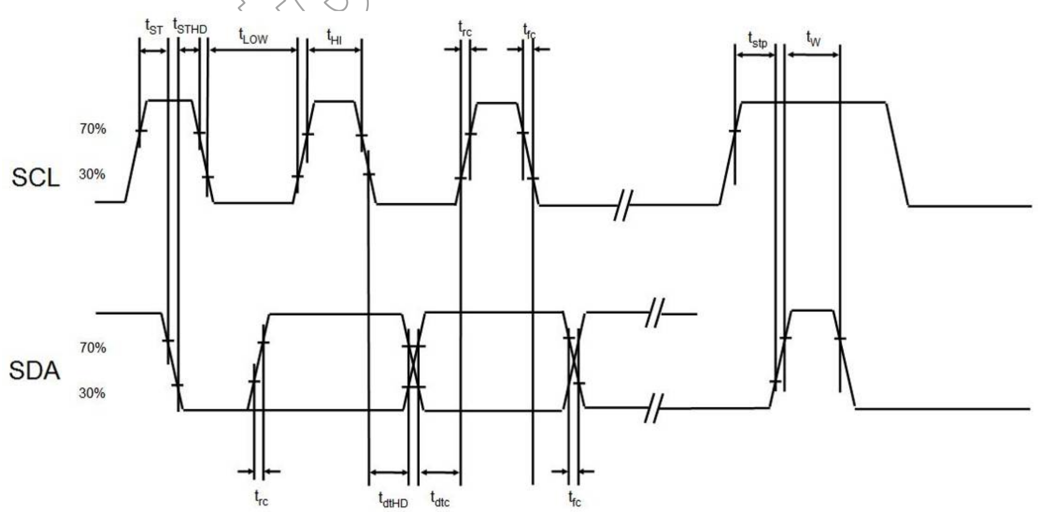


Figure 3: 2-wire Serial Control Interface Timing Diagram

Table 9: 3-Wire Interface Timing Characteristics

(Vcc = 2.7 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK}	Bus clock frequency				2.5	MHz
t_{HI}	SCL high time		50			ns
t_{LOW}	SCL low time		25			ns
ts	SEB and SDA falling edge to clock rising edge[1]		20			ns
t_h	Data holding time[1]		10			ns
t_{tr}	SCL rising edge to SDA output valid[1]	Only in read mode.	2		50	ns
t_{ed}	SCL rising edge to SDA output high Z[1]		2		25	ns

Notes:
1. Guaranteed by design.

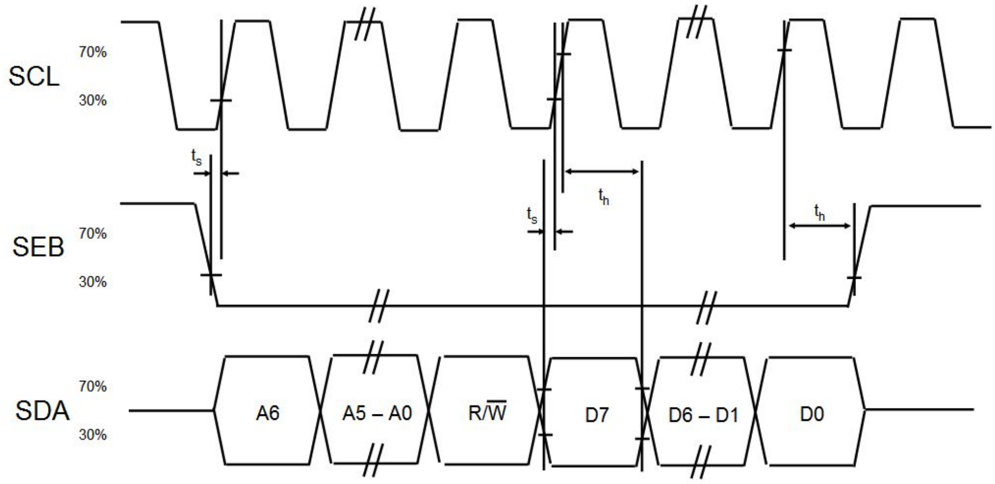


Figure 4: 3-Wire Serial Control Interface Write Timing Diagram

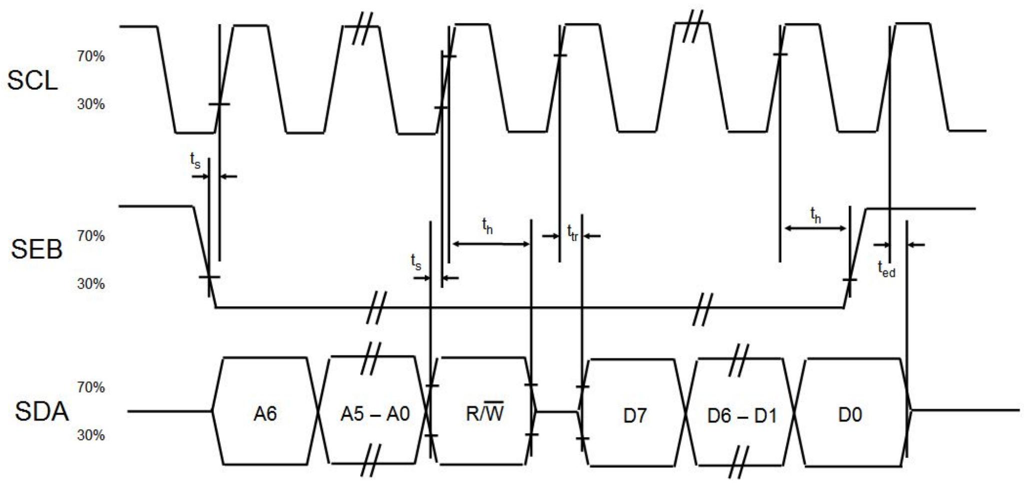


Figure 5: 3-Wire Serial Control Interface Read Timing Diagram

Table 10: Digital Audio Interface Timing Characteristics

Master Clock:

(Vcc = 2.7 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK_M}	Bus clock frequency				3.072	MHz
τ_{rise_M}	Rise-time				0.5	ns
τ_{fall_M}	Fall-time				0.5	ns
F_{err_M}	Frequency accuracy	According to PLL.			100	ppm

Slave Clock:

(Vcc = 2.7 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK_S}	Bus clock frequency				10	MHz
τ_{rise_S}	Rise-time				1.5	ns
τ_{fall_S}	Fall-time				1.5	ns
F_{err_S}	Frequency accuracy				100	ppm

3.1 I²S Interface Timing

Note: The term 'receiver' as described below is from the QN8007's point of view.

Either the QN8007 or the external device can act as the system master by providing the necessary clock signals. The slave will usually derive its internal clock signal from an external clock input. This means, taking into account the propagation delay between the master clock and the data and/or word-select signals, that the total delay is simply the sum of:

- The delay between the external (master) clock and slave's internal clock;
- The delay between the internal clock and the data and/or word-select signals.

For data and word-select inputs, the external to internal clock delay is of no consequence because it only lengthens the effective set-up time (see Figure 6:). The major part of the time margin is to accommodate the difference between the propagation delay of the transmitter, and the time required to set up the receiver. All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device. This means that higher data rates can be used in the future.

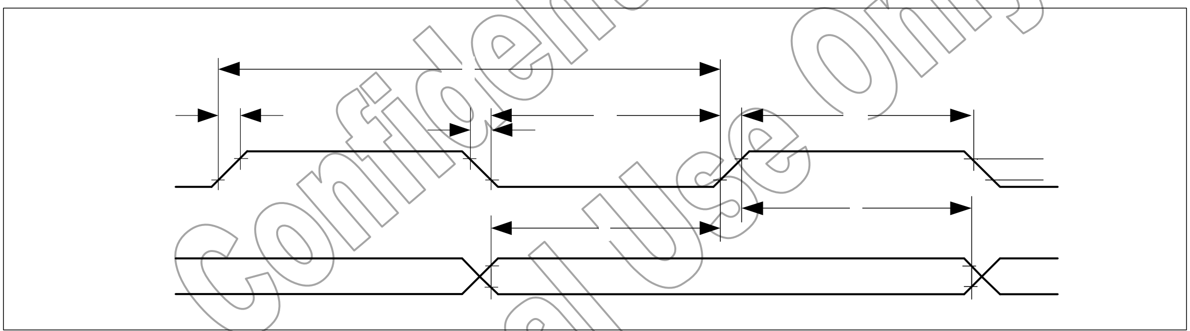


Figure 6: Timing for QN8007 as I²S Slave and Receiver

Table 11: Timing for QN8007 as I²S Slave and Receiver

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T	I²S clock frequency		100			ns
t_{LC}	Clock low time		10			ns
t_{HC}	Clock high time		10			ns
t_s	WS and SD setup time		10			ns
t_h	WS and SD hold time		5			ns
t_{RC}	Clock rise-time				5	ns
t_{FC}	Clock fall-time				5	ns

T

t_{RC} t_{FC}

MCK

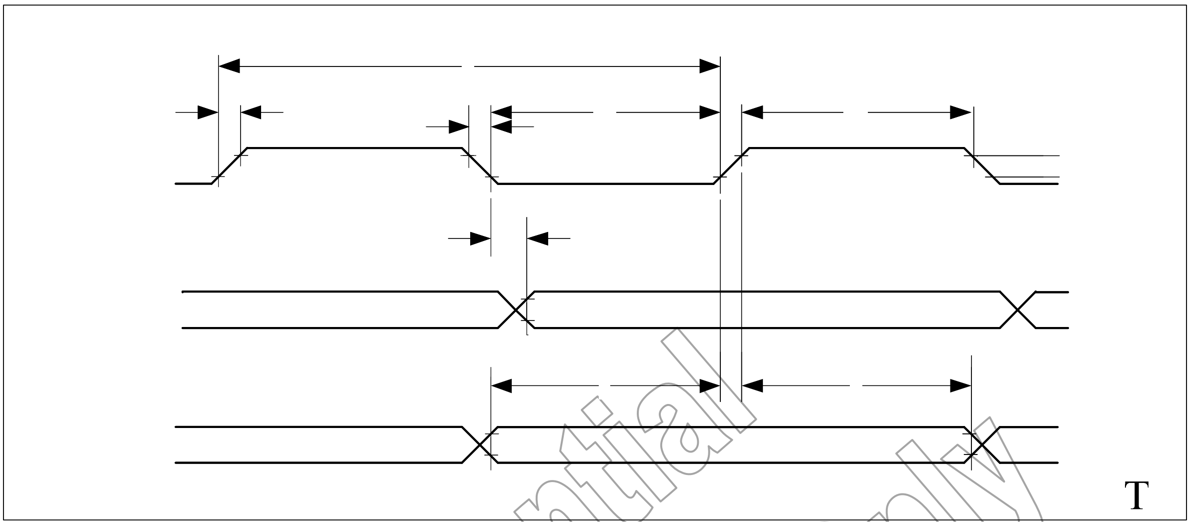


Figure 7: Timing for QN8007 as I²S Master and Receiver

Table 12: Timing for QN8007 as I²S Master and Receiver

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T	I²S clock period		330			ns
t_{LC}	Clock low time		120			ns
t_{HC}	Clock high time		120			ns
t_s	SD setup time		10			ns
t_h	SD hold time		5			ns
t_{dtr}	WS delay time				10	ns
t_{RC}	Clock rise-time				5	ns
t_{FC}	Clock fall-time				5	ns

4 FUNCTIONAL DESCRIPTION

The QN8007 is a high performance, low power, single chip FM transmitter IC that supports worldwide FM broadcast band operation. It has idle and standby modes for saving power. RDS/RBDS data service is also supported.

4.1 Transmit Mode

The QN8007 transmitter uses a highly digitized architecture. The input left and right analog audio signals are first adjusted by two automatic gain controlled (AGC) amplifiers, and then digitized by two high resolution ADCs into the digital domain. If a digital audio interface is used, the analog input circuits and ADCs will be bypassed. Pre-emphasis, soft clipping and MPX encoding are then performed. If RDS mode is enabled, the RDS signal will also be mixed with the MPX signal and the combined output will be fed into a high performance digital FM modulator which generates FM signal at RF carrier frequency. The FM signal is then filtered and amplified by the PA.

The QN8007 can deliver up to 121 dBμV output signal to an external antenna and/or matching network. An RF VGA provides a 42 dB of output power control range in 1.5dB steps and can be programmed through the serial control bus. Output power control and in-band power flatness can be easily achieved by a calibration circuit. This wide range of control allows for various antenna configurations such as loop, monopole, or meandering traces on PCB. An integrated RF bandpass filter ensures optimal output spectral purity.

4.2 Idle and Standby Mode

The QN8007 features low power IDLE and STANDBY modes for fast turn around and power saving. After power up, the QN8007 will enter IDLE mode automatically. If there is no transmitting requirement in a pre-determined time period, the QN8007 will enter STANDBY mode automatically. The auto-standby function can be enabled or disabled through the serial control interface.

4.3 Audio Interface

The QN8007 supports both analog and digital audio interfaces providing maximum flexibility in real applications.

Analog Audio Interface

The QN8007 has a highly flexible analog audio interface. For audio input, the signal is AC coupled with a 3dB corner frequency less than 50Hz. It has 4 different input impedances and 18dB adjustable gain range (in 1.5dB step) to optimize the SNR and linearity. The gain setting can be controlled automatically by integrated AGC or manually set through serial interface.

The single ended audio output level is 1V peak to peak and will be AC coupled to external audio driver.

Digital Audio Interface

With digital audio, the interface operates in slave mode and supports MSB-Justified, LSB-Justified, I^2S, DSP1, and DSP2. The three interface lines are MCK, DIN, and WS. MCK and WS can be tri-stated to allow for multiplexing.

4.4 Audio Processing

The QN8007 supports audio AGC, programmable pre-emphasis, and soft clipping. The AGC state machine will detect the signal level and control the VGA gain to optimize both SNR and THD. A saturation indicator is also integrated which will be asserted when the input signal is out of the range of AGC. A soft clipping feature provides graceful performance degradation when the signal level is higher than a pre-determined level.

Stereo signal is generated by the MPX circuit. It combines the left and right channel signals in the following way:

$$m(t) = \left[L(t) + R(t)\right] + \left[L(t) - R(t)\right]\sin(4\pi ft + 2\theta_0) + \alpha\sin(2\pi ft + \theta_0) + d(t)\sin(6\pi ft + 3\theta_0)$$

Here, L(t) and R(t) correspond to the audio signals on left and right channels respectively, f = 19 kHz, θ is the initial phase of pilot tone and α is the magnitude of pilot tone, and d(t) is RDS signal. In mono mode, only the L+R portion of audio signal is transmitted. The 19 kHz pilot tone is generated by the MPX circuit which contributes 9% of peak modulation, and RDS signal will contribute 2.1% of peak modulation.

A pre-emphasis function is also integrated with both 75µs and 50µs time constants. The time constant can be programmed through the serial control interface.

4.5 Channel Setting

The QN8007 supports both clear channel scan and manual channel setting.

Manual Channel Setting

By programming channel index CH[9:0], the RF channel can be set to any frequency between 76 MHz ~ 108 MHz in 50 kHz steps. The channel index and RF frequency have the following relationship:

F_{RF} = *(76 + 0.05* x *Channel Index), where* F_{RF} is the RF frequency in MHz.

The QN8007 has an integrated crystal oscillator and supports various crystal frequencies. Alternatively, the QN8007 can be driven externally by various clock frequencies.

Clear Channel Scan

The QN8007 can automatically find the clearest channel and return the channel information for FM transmission. The start, stop and frequency step of searching as well as upward or downward searching can be programmed through serial interface.

4.6 RDS/RBDS

The QN8007 supports RDS/RBBS data transmitting, including station ID, Meta data, TMC information, etc. The integrated RDS processor performs all symbol encoding/decoding, block synchronization, error detection and correction functions. RDS/RBDS data communicates with an external MCU through the serial control interface.

The INT pin is used for the interrupt signal as shown in Figure 8. Ping-pong buffers are used so that the user can write into one buffer while the RDS data in the other buffer is being transmitted. When the internal RDS buffer (8 bytes) is full, an Interrupt signal is generated. The user should wait for the Interrupt signal (INT) before toggling the RDSTXRDY bit in the SYSTEM2 register (reg. 01h [2]). Alternatively, the user can also check the RDS buffer space by reading the RDS_RXTXUPD bit in the STATUS2 register (reg. 1Bh [7]).

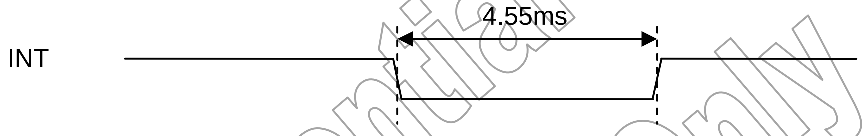


Figure 8: Interrupt Output

RDS/RBDS is not available in the QN8007L.

5 CONTROL INTERFACE PROTOCOL

The QN8007 supports 2- wire and 3-wire serial interfaces. The interface selection is controlled by the MOD pin which determines whether a 2- wire or a 3-wire serial interface will be used. MOD = HIGH selects a 3-wire bus and LOW selects a 2-wire bus.

5.1 2-Wire Serial Control Interface

The 2-wire bus is a simple bi-directional bus interface. The bus requires only serial data (SDA) and serial clock (SCL) signals. The bus is 8-bit oriented. Each device is recognized with a unique address. Each register is also recognized with a unique address. A third line (SEB) is used to choose the device address configuration. SEB = LOW selects the default address (0101011), SEB = HIGH selects register defined addressing. The L2 bus operates with a maximum frequency of 400 kHz. Each data put on the SDA must be 8 bits long (Byte) from MSB to LSB and each byte sent should be acknowledged by an "ACK" bit. In case a byte is not acknowledged, the transmitter should generate a stop condition or restart the transmission. If a stop condition is created before the whole transmission is completed, the remaining bytes will keep their old setting. In case a byte is not completely transferred, it will be discarded.

Data transfer to and from the QN8007 can begin when a start condition is created. This is the case if a transition from HIGH to LOW on the SDA line occurs while the SCL is HIGH. The first byte transferred represents the address of the IC plus the data direction. The default IC address is 0101011. A LOW LSB of this byte indicates data transmission (WRITE) while a HIGH LSB indicates data request (READ). This means that the first byte to be transmitted to the QN8007 should be "56" for a WRITE operation or "57" for a READ operation.

The second byte is the starting register address (N) for write/read operation. The following bytes are register data for address N, N+1, N+2, etc. There is no limit on the number of bytes in each transmission. A transmission can be terminated by generating a stop condition, which is SDA transition from LOW to HIGH while SCL is HIGH. For write operation, master stops transmission after the last byte. For read operation, master doesn't send ACK after receiving the last read back byte; then stops the transmission.

The following timing diagram is for both write and read.

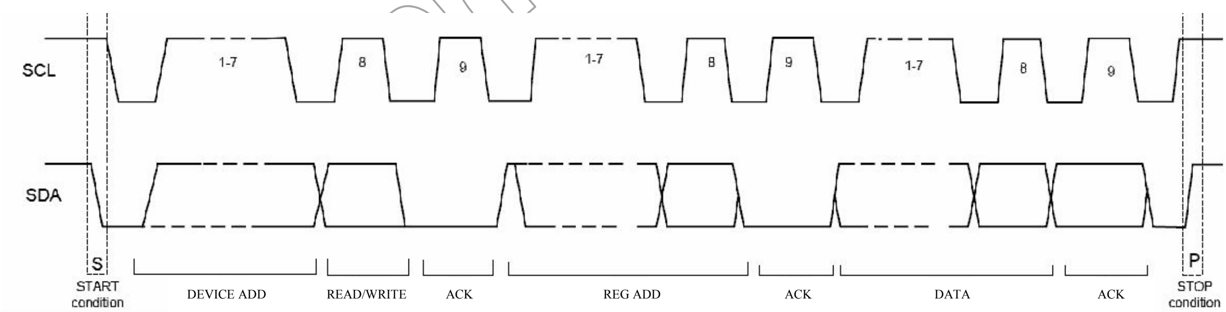


Figure 9: 2-Wire Serial Control Interface Protocol

5.2 3-Wire Serial Control Interface

For 3-wire serial operation, a transfer begins when the SEB pin is set LOW on a rising SCL edge. The control word is latched internally on rising SCL edges and is 8 bits in length, comprised of a 7-bit register address A6:A0, and a read/write bit (read = 1, write = 0). The ordering of the control word is A6:A0, R/W as shown in Figure 11.

For write operations, the serial control word is followed by an 8-bit data word and is latched internally on rising SCL edges. For read operations, a bus turn-around of half a cycle is followed by an 8-bit data word shifted out on rising SCL edges. The transfer ends on the rising SCL edge after SEB is set HIGH. After the 16th data bit, a full clock with both rising and falling edges is needed to shift in the control word.

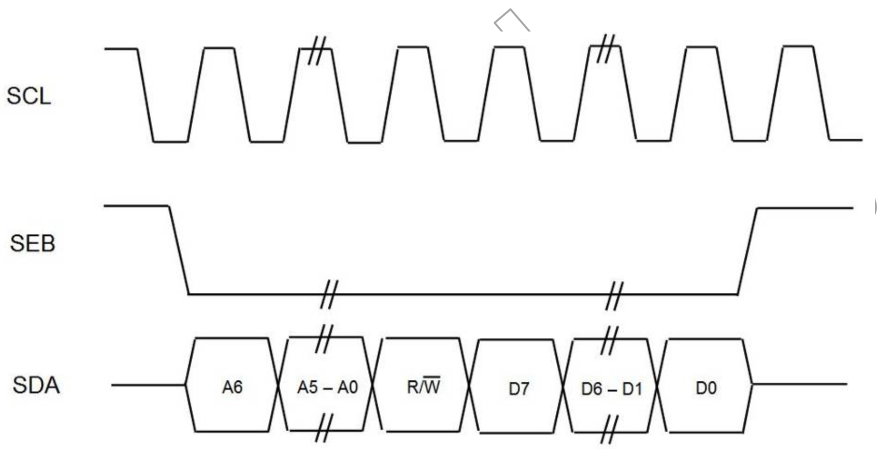


Figure 10: 3-Wire Serial Control Interface Write Protocol

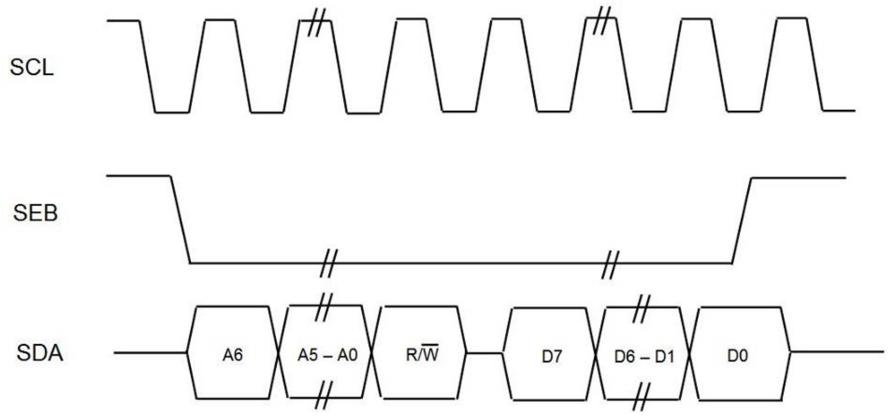


Figure 11: 3-Wire Serial Control Interface Read Protocol

6 DIGITAL AUDIO INTERFACE PROTOCOL

6.1 Introduction

The QN8007 uses an I^2S interface to transfer audio data from the external source.

- Master or Slave modes are supported.
- Multiple data widths are supported: 8, 16, 24, and 32 bits.
- Multiple data alignments are supported: I^2S, DSP1, DSP2, MSB-Justified, and LSB-Justified modes.
- The term 'transmitter' as described below is from the QN8007's point of view.

6.2 I^2S BUS Signal Description

A 3-line serial bus is used consisting of a line for two time-multiplexed data channels, a word select line, and a clock line. The following figure shows how to use these three signals in the QN8007.

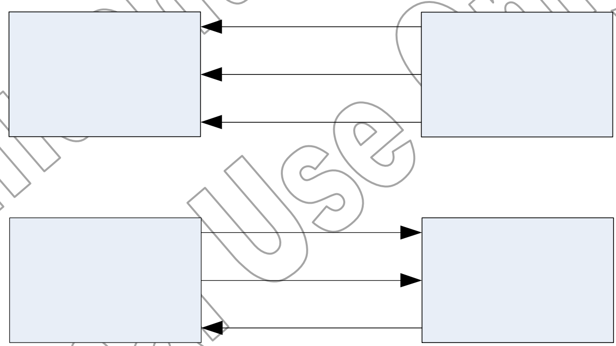


Figure 12: Top Level Block Diagram of I^2S

In Master mode, the serial clock signal SCK and the word selection signal WS are generated by the QN8007 and are output to the external device. In Slave mode, those two signals are input signals from the external device.

The QN8007 receives the serial data from the external device by the SD signal.

QN8007 as Slave and Receiver

QN8007

QN8007 as

6.3 I²S Interface Timing Description

The word select line indicates the channel being transmitted:

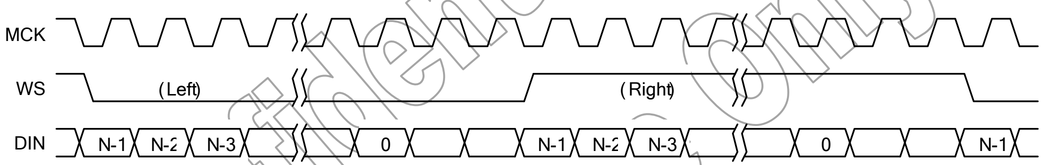
- WS = 0; channel 1 (left);
- WS = 1; channel 2 (right).

WS sent by the transmitter is synchronized by the trailing (HIGH-to-LOW) edge of the serial clock signal and is latched into the receiver on the leading (LOW-to-HIGH) edge of the serial clock signal.

The serial data signal SD has the same timing requirement as the WS signal. It is sent on the trailing edge of the clock signal by the transmitter, and received on the leading edge of the clock signal by the receiver. The serial data is transmitted in two's complement with the MSB first. The MSB is transmitted first because the transmitter and the receiver may have different word lengths. There are four data word lengths supported by the QN8007; 8, 16, 24 and 32.

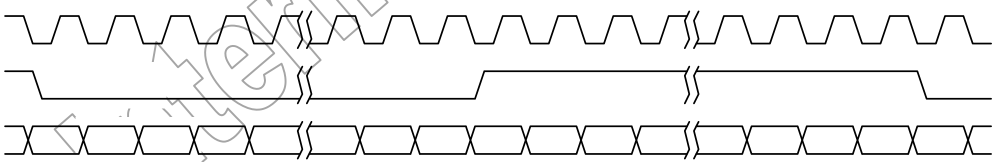
There are five data alignment modes supported by QN8007. The detailed timing descriptions are shown as below.

6.3.1 MSB-Justified (Format 0)



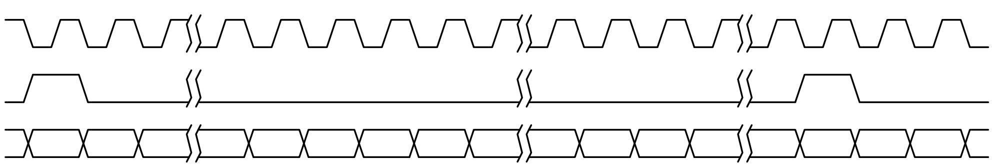
The transmitter sends the MSB (N-1) bit of the next word when the WS changes and sends the second MSB bit in the next clock period. Each bit is sent by the transmitter in one clock period until the LSB (0) bit is sent. The N indicates the word length that can be 8, 16, 24, and 32.

6.3.2 I²S (Format 1)



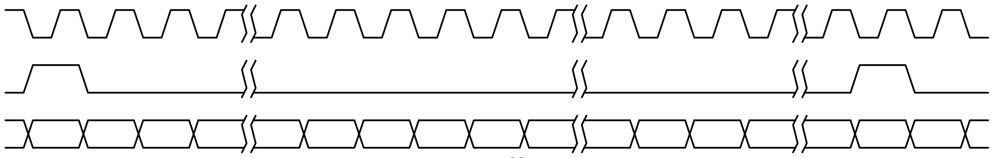
The transmitter sends the MSB(N-1) bit of the next word one clock period after the WS changes and sends the second MSB bit in the next clock period. Each bit is sent by the transmitter in one clock period until the LSB (0) bit is sent. In the case that the number of cycles equal the number of bits to be sent, the LSB (0) bit could be sent after the next WS change. The N indicates the word length that can be 8, 16, 24, and 32.

6.3.3 DSP1 (Format 2)



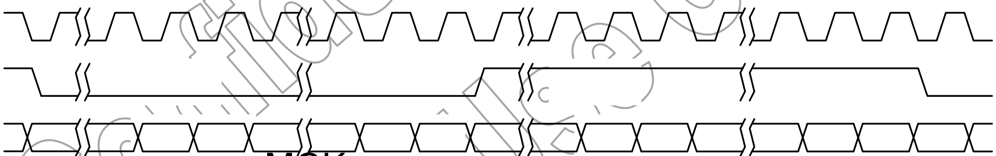
The transmitter sends the MSB (N-1) bit of the next word when the WS pulse occurs and sends the second MSB bit in the next clock period. Each bit is sent by the transmitter in one clock period until the LSB (0) bit is sent. Following the first LSB, transmitter sends the MSB (N-1) bit of a new word and then keeps sending data until the data transmission is finished. The N indicates the word length that can be 8, 16, 24, and 32.

6.3.4 DSP2 (Format 3)



The transmitter sends the MSB(N-1) bit of the next word one clock period after the WS pulse occurs and sends the second MSB bit in the next clock period. Each bit is sent by the transmitter in one clock period until the LSB (0) bit is sent. Following the first LSB, transmitter sends the MSB(N-1) bit of a new word and then keeps sending data until the data transmission is finished. The N indicates the word length that can be 8, 16, 24, and 32.

6.3.5 LSB-Justified (Format 4)



The transmitter sends the MSB (N-1) bit of the next word in the (N-1)th clock period back-counting from the next WS changes. The second MSB bit is sent in the next clock period. Finally, the LSB(0) bit is sent in the clock period that is just before the next WS changes in one clock period. The N indicates the word length that can be 8, 16, 24, and 32.

MCK
WS
(Left)
DIN
N-1
N-2
1

7 USER CONTROL REGISTERS

-------- THIS IS A PREVIEW LIST. Number and content of registers subject to change without notice --------

There are 28 user accessible control registers. All registers not listed below are for manufacturing use only.

Table 13: Summary of User Control Registers

REGISTER	NAME	USER CONTROL FUNCTIONS
00h	SYSTEM1	Sets device modes.
01h	SYSTEM2	Sets device modes, resets.
02h	DEV_ADD	Sets device address.
03h	ANACTL1	Analog control functions.
04h	REG_VGA	TX mode input impedance, crystal cap load setting.
05h	CID1	Device ID numbers.
06h	CID2	Device ID numbers.
07h	I^2S	Sets I^2S parameters.
08h	CH	Lower 8 bits of 10-bit channel index.
09h	CH_START	Lower 8 bits of 10-bit channel scan start channel index.
0Ah	CH_STOP	Lower 8 bits of 10-bit channel scan stop channel index.
0Bh	CH_STEP	Channel scan frequency step. Highest 2 bits of channel indexes.
0Ch	PAC_TARGET	Output power calibration control.
0Dh	TXAGC GAIN	Sets TX parameters.
0Eh	TX_FDEV	Specify total TX frequency deviation.
0Fh	GAIN_TXPLT	Gain of TX pilot frequency deviation, I^2S buffer clear.
10h	RDSD0	RDS data byte 0.
11h	RDSD1	RDS data byte 1.
12h	RDSD2	RDS data byte 2.
13h	RDSD3	RDS data byte 3.
14h	RDSD4	RDS data byte 4.
15h	RDSD5	RDS data byte 5.
16h	RDSD6	RDS data byte 6.
17h	RDSD7	RDS data byte 7.
18h	RDSFDEV	Specify RDS frequency deviation, RDS mode selection.
19h	CCA	Sets CCA parameters.
1Ah	STATUS1	Device status indicators.
1Bh	STATUS2	Device status indicators.
49h	REG_XLT3	XCLK pin control.
59h	PAC_CAL	PA tuning cap calibration.
5Ah	PAG_CAL	PA gain calibration.

Register Bit R/W Status:

RO - Read Only: You can not program these bits.
WO - Write Only: You can write and read these bits; the value you read back will be the same as written.
R/W - Read/Write: You can write and read these bits; the value you read back can be different from the value written. Typically, the value is set by the chip itself. This could be a calibration result, AGC FSM result, etc.

<u>Word</u>: SYSTEM1 <u>Address</u>: 00h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rsvd	txreq	chsc	stnby	rsvd	txi2s	rdsen	cca_ch_dis
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7	rsvd	0	Reserved	
6	TXREQ	0	Transmission request:	
			0	Non TX mode. Either idle or standby mode.
			1	Enter Transmit mode.
5	CHSC	0	Channel Scan mode enable: Combined with TXREQ, the chip scans for an empty channel for transmission. After completing channel scanning, this bit will be cleared automatically. For CCS (TX Scan), the clearest channel (channel with weakest RSSI) will be selected (if TXCCAA is not equal zero, another prior condition should be met, see description of CCA register at 19h).To use the scanned channel, set CCA_CH_DIS to 0. (CCA_CH_DIS can be set to 0 at the same time CHSC=1).	
			0	Normal operation.
			1	Channel Scan mode operation.
4	STNBY	0	Request immediately to enter Standby mode if the chip is in IDLE and no TXREQ is received.	
			0	Non standby mode. Either idle, or TX mode.
			1	Enter standby mode.
3	rsvd	0	Reserved	
2	TXI2S	0	I^2S enable:	
			0	Use analog input for TX audio.
			1	Use I^2S digital signal for TX audio.
1	RDSEN	0	RDS enable:	
			0	RDS disable.
			1	RDS enable.
0	CCA_CH_DIS	1	CH (channel index) selection method: See description for CH register at 08h and 0Bh for more information.	
			0	CH is determined by internal CCA (channel scan).

			1	CH is determined by the content in CH[9:0].

Note: TXREQ has highest priority, and STNBY has the lowest priority.

Word: SYSTEM2 Address: 01h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
swrst	recal	rsvd	st_mo_tx	tc	rdstxrdy	tmout[1]	tmout[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7	SWRST	0	Reset all registers to default values:	
			0	Keep the current value.
			1	Reset to default values.
6	RECAL	0	Reset the state to initial states and recalibrate all blocks:	
			0	FSM runs normally.
			1	Reset the FSM. After this bit is de-asserted, FSM will go through all the power up and calibration sequence.
5	rsvd	0	Reserved	
4	ST_MO_TX	0	TX stereo and mono mode selection:	
			0	Stereo
			1	Mono
3	TC	1	Pre-emphasis time constant: (µs)	
			0	50
			1	75
2	RDSTXRDY	0	RDS transmit ready: Toggle this bit to transmit all 8 bytes in RDS0~RDS7. The chip will internally fetch these bytes after completing transmit of the current group.	
1:0	TMOUT[1:0]	01	Time out setting for IDLE to standby state transition: (min)	
			0 0	1
			0 1	3
			1 0	5
			1 1	infinity (never)

Word: DEV_ADD **Address: 02h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rsvd	dadd[6]	dadd [5]	dadd [4]	dadd [3]	dadd [2]	dadd [1]	dadd [0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7	rsvd	0	Reserved	
6:0	DADD[6:0]	010 1010	Programmed device address when SEB=1: If SEB=0, the default device address (0101011) is used. After power up, if SEB=1, the device address is decided by this register (default 010 1010).	
			SEB	Device address:
			0	0101011
			1	DADDR[6:0]

Word: ANACTL1 **Address: 03h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
mute_en	i2s_sckinv	rstb_bb	ant_sel	xsel[3]	xsel[2]	xsel[1]	xsel[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7	MUTE_EN	0	TX audio mute enable:	
			0	Un-mute
			1	Mute
6	I2S_SCKINV	0	I^2S MCK invert:	
			0	Non inverted
			1	Inverted
5	RSTB_BB	1	Reset signal of baseband data-path: (Low active)	
			0	Reset
			1	No action
4	ANT_SEL	0	Select the antenna for TX channel scan mode:	
			0	Use the receiver antenna from RFI.
			1	Use the transmitter antenna on RFO.
3:0	XSEL[3:0]	1011	Crystal Frequency Selection (MHz):	
			0000	11.2896
			0001	12

			0010	12.288
			0011	13
			0100	16.367
			0101	18.414
			0110	19.2
			0111	Reserved
			1000	22.5792
			1001	24
			1010	24.576
			1011	26 (default)
			1100	32.734
			1101	36.828
			1110	38.4
			1111	7.6

Word: REG_VGA   **Address: 04h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rin[1]	rin[0]	xcsel[5]	xcsel[4]	xcsel[3]	xcsel[2]	xcsel[1]	xcsel[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7:6	RIN[1:0]	01	TX mode input impedance for both L/R channels: (kΩ)	
			0 0	10
			0 1	20
			1 0	40
			1 1	80
5:0	XCSEL[5:0]	10 0000	Crystal cap load setting: The loading cap on each side is: 10+XCSEL*0.32 pF, i.e. it ranges from 10pF to 30pF. Default is 20 pF.	

Word: CID1 **Address**: 05h (RO)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rsvd	rsvd	rsvd	cid1[2]	cid1[1]	cid1[0]	cid2[1]	cid2[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description	
7:5	Rsvd	rrr	reserved	
4:2	CID1[2:0]	rrr	Chip ID for product family:	
		000	000	FM
			001-111	Reserved
1:0	CID2[1:0]	rr	Chip ID for minor revision:	
		01	00	1
			01	2
			10	3
			11	4

Word: CID2 **Address**: 06h (RO)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
cid3[3]	cid3[2]	cid3[1]	cid3[0]	cid4[3]	cid4[2]	cid4[1]	cid4[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description	
7:4	CID3[3:0]	rrrr	Chip ID for product ID:	
		0001	0000	Reserved
			0001	Transmitter – QN8007
			0010	Reserved
			0011	Reserved
			0100	Reserved
			0101	Transmitter – QN8007L
			0110-1111	Reserved
3:0	CID4[3:0]	rrrr	Chip ID for major revision is 1+CID4:	
		0000	0000	1
			0001	2

			0010	3
			0011	4
			0100-1111	Reserved

Word: I²S **Address: 07h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
i2sbw[1]	i2sbw[0]	i2sdrate[1]	i2sdrate[0]	i2smode	i2sfmt[2]	i2sfmt[1]	i2sfmt[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7:6	I2SBW[1:0]	01	I²S bit width:	
			00	8-bit
			01	16-bit
			10	24-bit
			11	32-bit
5:4	I2SDRATE[1:0]	11	I²S data rate:	
			00	32kbps
			01	40kbps
			10	44.1kbps
			11	48kbps
3	I2SMODE	0	I²S mode:	
			0	Slave
			1	Master
2:0	I2SFMT[2:0]	001	I²S format:	
			000	MSB justified mode
			001	I²S mode
			010	DSP1 mode
			011	DSP2 mode
			100	LSB justified mode
			101-111	Reserved

Word: CH **Address**: 08h (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
ch[7]	ch[6]	ch[5]	ch[4]	ch[3]	ch[2]	ch[1]	ch[0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description
7:0	CH[7:0]	1010 0000	Lower 8 bits of 10-bit Channel index: Channel used for TX has two origins, one is from this register and CH[9:8] at 0Bh which can be written by the user, another is from CCA/CCS. CCA/CCS selected channels are stored in an internal register, which is physically different from the CH register, but it can be read out through register CH and be used for TX when CCA_CH_DIS (reg. 00h bit [0]) = 0.

Word: CH_START **Address**: 09h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
ch_sta[7]	ch_sta[6]	ch_sta[5]	ch_sta[4]	ch_sta[3]	ch_sta[2]	ch_sta[1]	ch_sta[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	CH_STA[7:0]	0000 0000	Lower 8 bits of 10-bit CCA (channel scan) start channel index.

Word: CH_STOP **Address**: 0Ah

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
ch_stp[7]	ch_stp[6]	ch_stp[5]	ch_stp[4]	ch_stp[3]	ch_stp[2]	ch_stp[1]	ch_stp[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	CH_STP[7:0]	1000 0000	Lower 8 bits of 10-bit CCA (channel scan) stop channel index.

Word: CH_STEP **Address**: 0Bh

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
fstep[1]	fstep[0]	ch_stp[9]	ch_stp[8]	ch_sta[9]	ch_sta[8]	ch[9]	ch[8]
wo	wo	wo	wo	wo	wo	rw	rw

Bit	Symbol	Default	Description	
7:6	FSTEP[1:0]	01	CCA (channel scan) frequency step:	
			00	50 kHz
			01	100 kHz
			10	200 kHz
			11	Reserved
5:4	CH_STP[9:8]	10	Highest 2 bits of 10-bit CCA(channel scan) stop channel index: Stop freq is (76+CH_STP*0.05) MHz.	
3:2	CH_STA[9:8]	00	Highest 2 bits of 10-bit CCA(channel scan) start channel index: Start freq is (76+CH_STA*0.05) MHz.	
1:0	CH[9:8]	00	Highest 2 bits of 10-bit channel index: Channel freq is (76+CH*0.05) MHz.	

Word: PAC_TARGET **Address**: 0Ch

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
pac_target [7]	pac_target [6]	pac_target [5]	pac_target [4]	pac_target [3]	pac_target [2]	pac_target [1]	pac_target [0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	PAC_TARGET [7:0]	1111 1111	PA calibration target value. PA output target is (0.37*PAC_TARGET+68) dBuV. Valid values are 31-131 dBuV.

Word: TXAGC GAIN **Address**: 0Dh (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tx_sftclpen	tagc_gain_sel	rsvd	txagc_gdb	txagc_gvga [3]	txagc_gvga [2]	txagc_gvga [1]	txagc_gvga [0]
wo	wo	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description	
7	TX_SFTCLPEN	0	TX soft clipping enable:	
			0	Disable
			1	Enabled
6	TAGC_GAIN_SEL	0	TX AGC Gain selection method:	
			0	Both the TX digital gain TXAGC_GDB and the TX input buffer gain TXAGC_GVGA [3:0] are determined by TX AGC FSM on chip.
			1	Both the TX digital gain and the TX input buffer gain are determined by the contents of TXAGC_GDB and TXAGC_GVGA [3:0] respectively.
5	rsvd	0	Reserved	
4	TXAGC_GDB	0	TX digital gain:	
			0	0 dB
			1	1 dB
3:0	TXAGC_GVGA [3:0]	0001	TX input buffer gain: (dB)	

VGAG [3:0]	RIN[1:0] 00	01	10	11
0000	4.5	-1.5	-7.5	-13.5
0001	6	0	-6	-12
0010	7.5	1.5	-4.5	-10.5
0011	9	3	-3	-9
0100	10.5	4.5	-1.5	-7.5
0101	12	6	0	-6
0110	13.5	7.5	1.5	-4.5
0111	15	9	3	-3
1000	16.5	10.5	4.5	-1.5
1001	18	12	6	0
1010	19.5	13.5	7.5	1.5
1011	21	15	9	3
11XX	Reserved			

Word: TX_FDEV **Address**: 0Eh

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tx_fdev[7]	tx_fdev[6]	tx_fdev[5]	tx_fdev[4]	tx_fdev[3]	tx_fdev[2]	tx_fdev[1]	tx_fdev[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7:0	TX_FDEV[7:0]	0110 1100	Specify total TX frequency deviation: TX frequency deviation = 0.69 kHz*TX_FEDV.	
			TX_FDEV[7:0]	Value
			0000 0000 - 1111 1111	0 ~ 255

Word: GAIN_TXPLT **Address**: 0Fh

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
i2sundfl_ clr	i2sovfl_ clr	gain_txpl [3]	gain_txplt [2]	gain_txplt [1]	gain_txplt [0]	rds_int_en	cca_int_en
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7	I2SUNDFL_ CLR	0	I^{2}S buffer underflow clear: User has to de-assert this bit after clearing.	
			0	No action
			1	Clear
6	I2SOVFL_ CLR	0	I^{2}S buffer overflow clear: User has to de-assert this bit after clearing.	
			0	No action
			1	Clear
5:2	GAIN_TXPLT [3:0]	10 01	Gain of TX pilot to adjust pilot frequency deviation: Refer to peak frequency deviation of MPX signal when audio input is full scale.	
			0111	7% * 75kHz
			1000	8% * 75kHz
			1001	9% * 75kHz
			1010	10% * 75kHz
1	RDS_INT_EN	0	RDS TX Interrupt Enable: When RDS_INT_EN=1, a 4.5ms low pulse will be output from DOUT/INT when a new group of data in RDSD0~RDSD7 is loaded into the internal transmitting buffer after user toggles RDSTXRDY.	
			0	Disable
			1	Enable

0	CCA_INT_EN	0	TX CCA Interrupt Enable: When CCA_INT_EN=1, a 4.5ms low pulse will be output from DOUT/INT (TX mode) when TXCCA is finished.	
			0	Disable
			1	Enable

Word: RDSD0 Address: 10h (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd0[7]	rdsd0[6]	rdsd0[5]	rdsd0[4]	rdsd0[3]	rdsd0[2]	rdsd0[1]	rdsd0[0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description
7:0	RDSD0[7:0]	0000 0000	RDS data byte 0: Data written into RDSD0~RDSD7 cannot be read out unless RDSTXRDY is toggled to allow the data to be loaded into the internal transmitting buffer.

Word: RDSD1 Address: 11h (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd1[7]	rdsd1[6]	rdsd1[5]	rdsd1[4]	rdsd1[3]	rdsd1[2]	rdsd1[1]	rdsd1[0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description
7:0	RDSD1[7:0]	0000 0000	RDS data byte 1

Word: RDSD2 Address: 12h (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd2[7]	rdsd2[6]	rdsd2[5]	rdsd2[4]	rdsd2[3]	rdsd2[2]	rdsd2[1]	rdsd2[0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description
7:0	RDSD2[7:0]	0000 0000	RDS data byte 2

Word: RDSD3 Address: 13h (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd3[7]	rdsd3[6]	rdsd3[5]	rdsd3[4]	rdsd3[3]	rdsd3[2]	rdsd3[1]	rdsd3[0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description
7:0	RDSD3[7:0]	0000 0000	RDS data byte 3

Word: RDSD4 Address: 14h (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd4[7]	rdsd4[6]	rdsd4[5]	rdsd4[4]	rdsd4[3]	rdsd4[2]	rdsd4[1]	rdsd4[0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description
7:0	RDSD4[7:0]	0000 0000	RDS data byte 4

Word: RDSD5 Address: 15h (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd5[7]	rdsd5[6]	rdsd5[5]	rdsd5[4]	rdsd5[3]	rdsd5[2]	rdsd5[1]	rdsd5[0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description
7:0	RDSD5[7:0]	0000 0000	RDS data byte 5

Word: RDSD6 Address: 16h (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd6[7]	rdsd6[6]	rdsd6[5]	rdsd6[4]	rdsd6[3]	rdsd6[2]	rdsd6[1]	rdsd6[0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description
7:0	RDSD6[7:0]	0000 0000	RDS data byte 6

Word: RDSD7 Address: 17h (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd7[7]	rdsd7[6]	rdsd7[5]	rdsd7[4]	rdsd7[3]	rdsd7[2]	rdsd7[1]	rdsd7[0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description
7:0	RDSD7[7:0]	0000 0000	RDS data byte 7: Writing to this byte will cause the entire group (8 bytes) to be updated into the internal transmitting buffer.

Word: RDSFDEV   **Address**: 18h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rsvd	rdsfdev[6]	rdsfdev[5]	rdsfdev[4]	rdsfdev[3]	rdsfdev[2]	rdsfdev[1]	rdsfdev[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7	rsvd	1	Reserved
6:0	RDSFDEV[6:0]	000 0110	Specify RDS frequency deviation: RDS frequency deviation = 0.35 kHz*RDSFDEV. RDSFDEV[6:0] | Value 000 0000 - 111 1111 | 0 ~ 127

Word: CCA   **Address**: 19h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
txccaa[2]	txccaa[1]	txccaa[0]	rsvd	rsvd	rsvd	rsvd	rsvd
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:5	TXCCAA[2:0]	010	Scaling factor to determine in-band noise power to out of band noise power ratio. Value 0 ~ 7 directly written in, default is 2. When TXCCAA is not zero, valid channels must satisfy the condition "in-band power > TXCCAA * out-of-band power", which usually is set to select channels without adjacent channel interference. When TXCCAA=0, this condition is omitted.
4:0	rsvd	0 1001	Reserved

Word: STATUS1 **Address**: 1Ah (RO)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rsvd	rsvd	i2sovfl	i2sundfl	insat	rsvd	rsvd	rsvd
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description	
7:6	rsvd	rr	Reserved	
5	I2SOVFL	r	I^{2}S overflow indicator:	
			0	No overflow
			1	Overflow
4	I2SUNDFL	r	I^{2}S underflow indicator:	
			0	No underflow
			1	Underflow
3	INSAT	r	Input level saturation flag:	
			0	No saturation
			1	Input level too high, Channel saturates.
2:0	rsvd	rr	Reserved	

Word: STATUS2 **Address**: 1Bh (RO)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rds_rxtxupd	rsvd	rsvd	rsvd	rsvd	rsvd	rsvd	rsvd
ro	ro	ro	ro	ro	ro	ro	ro

Bit	value	Symbol	Description	
7	r	RDS_RXTXUPD	RDS RX: RDS received group updated. Each time a new group is received, this bit will be toggled. RDS TX: If user want the chip transmitting all the 8 bytes in RDS0~RDS7, user should toggle the register bit RDSTXRDY. Then the chip internally will fetch these bytes after completing transmitting of current group. Once the chip internally fetched these bytes, it will toggle this bit. If RDS_INT_EN=1, then at the same time this bit is toggled, interrupt output will out put a 4.5 ms low pulse.	
			RDS_RXTXUPD	Status

			0->1 or 1->0	A new set (8 Byte) of data is received
			0->0 or 1->1	New data is in receiving
6:0	rsvd	rr	Reserved	

Word: XLT3 **Address**: 49h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rsvd	rsvd	rsvd	xtlbyp	rsvd	rsvd	rsvd	rsvd
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7:5	rsvd	rrr	Reserved	
4	XTLBYP	0	Direct inject crystal oscillation from external XCLK pin.	
			0	Use internal crystal oscillator.
			1	Inject external clock from pin XCLK.
3:0	rsvd	rrrr	Reserved	

Word: PAC_CAL **Address**: 59h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
pac_req	pac_dis	pacap[5]	pacap[4]	pacap[3]	pacap[2]	pacap[1]	pacap[0]
wo	wo	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description	
7	PAC_REQ	0	Manually request PA tuning cap and gain calibration	
			PAC_REQ	Calibration request
			1	Reset the calibration
			0	At the 1->0 transition, calibration starts
6	PAC_DIS	0	Disable PA tuning cap calibration and use PACAP as circuit setting	
			PAC_DIS	Status of calibration
			0	Use calibrated value
			1	No calibration and use user-set value

5:0	PACAP[5:0]	000000	User-set PA Tuning cap. Each LSB is 0.3pF. The read back value is the calibration result.

Word: PAG_CAL Address: 5Ah

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rsvd	pag_dis	paipow[1]	paipow[0]	pagain[3]	pagain[2]	pagain[1]	pagain[0]
wo	wo	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description	
7	rsvd	r	Reserved.	
6	PAG_DIS	0	Disable PA output power calibration and use IPOW, PAGAIN as circuit setting	
			PAG_DIS	Status of calibration
			0	Use calibrated value
			1	No calibration and use user-set value
5:4	IPOW[1:0]	00	Set PA current. The read back value is the calibration result.	
			IPOW[1:0]	Current consumption in PA
			00	4mA
			01	2mA
			10	1mA
			11	0.5mA
3:0	PAGAIN[3:0]	1111	Set PAGAIn setting. The read back value is the calibration result. Transmitter output voltage on the RFO pin (dBuV) is 124dBuV-1.5dB*PAGAIN [3:0].	
			POUT[3:0]	Power w matching
			0	124
			1	122.5
			10	121
			11	119.5
			100	118
			101	116.5
			110	115

			111	113.5
			1000	112
			1001	110.5
			1010	109
			1011	107.5
			1100	106
			1101	104.5
			1110	103
			1111	101.5

8 PACKAGE DESCRIPTION

24-Lead plastic Quad Flat, No Lead Package (ML) – 4x4 mm Body [QFN]

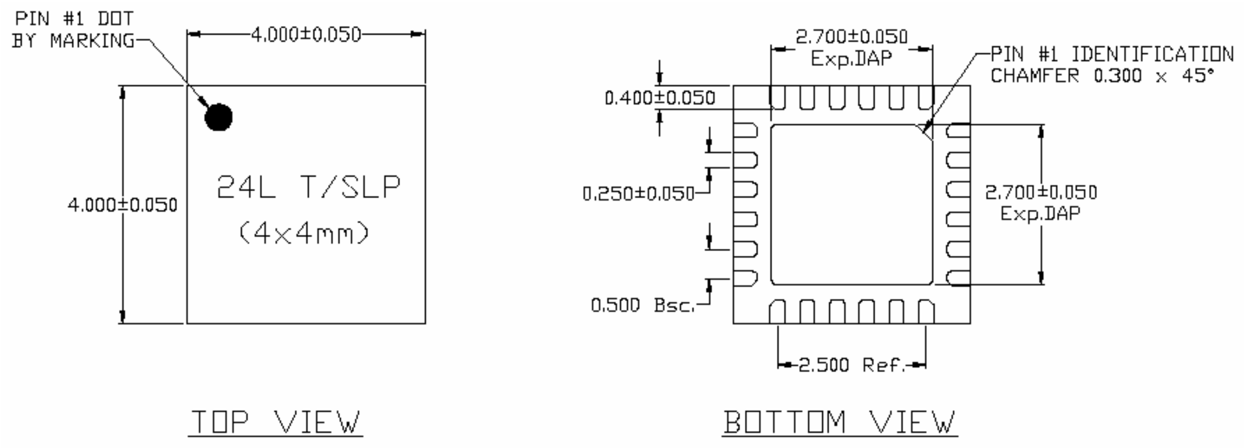


Figure 13: QN8007B/8007BL Device

Units	Millimeters		
Dimension Limits	**MIN**	**NOM**	**MAX**
Number of pins	24		
Pitch	0.50 BSC		
Overall Height (SLP)	0.80	0.85	0.90
Standoff	0.00		0.05
Contact Thickness	0.203 REF		
Overall Width	4.00 BSC		
Exposed Pad Width	2.65	2.70	2.75
Overall Length	4.00 BSC		
Exposed Pad Length	2.65	2.70	2.75
Contact Width	0.20	0.25	0.30
Contact Length	0.35	0.40	0.45
Contact-to-Exposed Pad	-	0.25	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerance per ASME Y 14.5M.
   BSC: Basic Dimension. The theoretically exact value is shown without tolerance.
   REF: Reference Dimension, usually without tolerance, for information purpose only.

Carrier Tape Dimensions

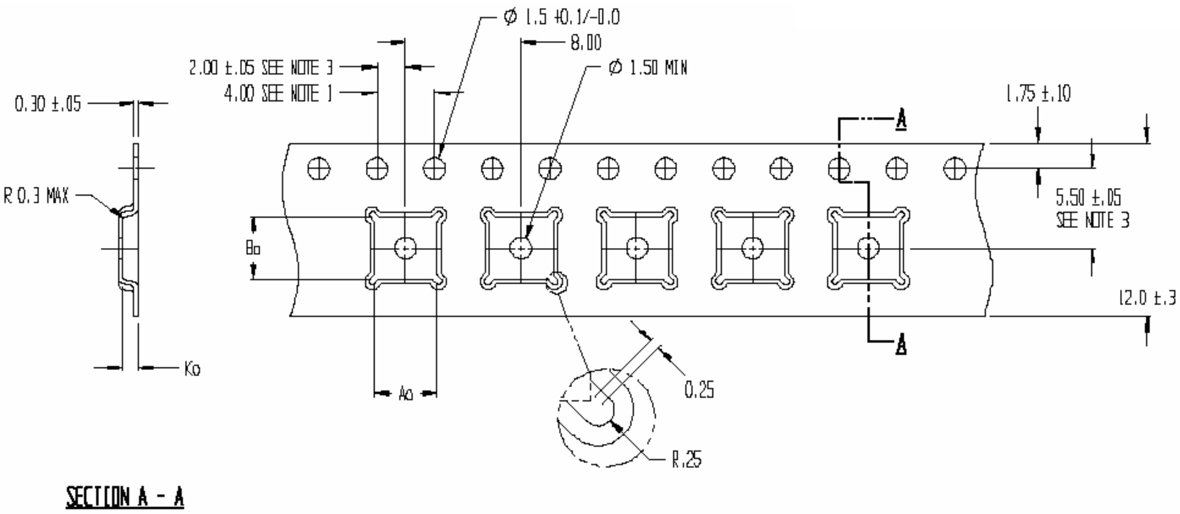


Figure 14: QN8007B/8007BL Carrier Tape Dimensions

NOTES:

1. 10 sprocket hole pitch cumulative tolerance ±0.2.
2. Camber in compliance with EIA-481.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
4. $A_0 = 4.35$
   $B_0 = 4.35$
   $K_0 = 1.10$
5. Reels are shipped in one of two sizes: 2,500 or 5,000 pieces per reel.

9 SOLDER REFLOW PROFILE

9.1 Package Peak Reflow Temperature

QN800X is assembled in a lead-free QFN24 package. Since the geometrical size of QN800X is 4 mm × 4 mm × 0.85 mm, the volume and thickness is in the category of volume<350 mm^3 and thickness<1.6 mm in Table 4-2 of IPC/JEDEC J-STD-020C. The peak reflow temperature is:

$$T_p = 260^{o}C$$

The temperature tolerance is +0^{o}C and -5^{o}C. Temperature is measured at the top of the package.

9.2 Classification Reflow Profiles

Profile Feature		Specification*
Average Ramp-Up Rate (tsmax to tP)		3°C/second max.
Pre-heat:	Temperature Min (Tsmin)	150°C
	Temperature Max (Tsmax)	200°C
	Time (ts)	60-180 seconds
Time maintained above:	Temperature (T_L)	217°C
	Time (t_L)	60-150 seconds
Peak/Classification Temperature (Tp)		260°C
Time within 5°C of Actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate		6°C/second max.
Time 25°C to Peak Temperature		8 minutes max.

*Note: All temperatures are measured at the top of the package.

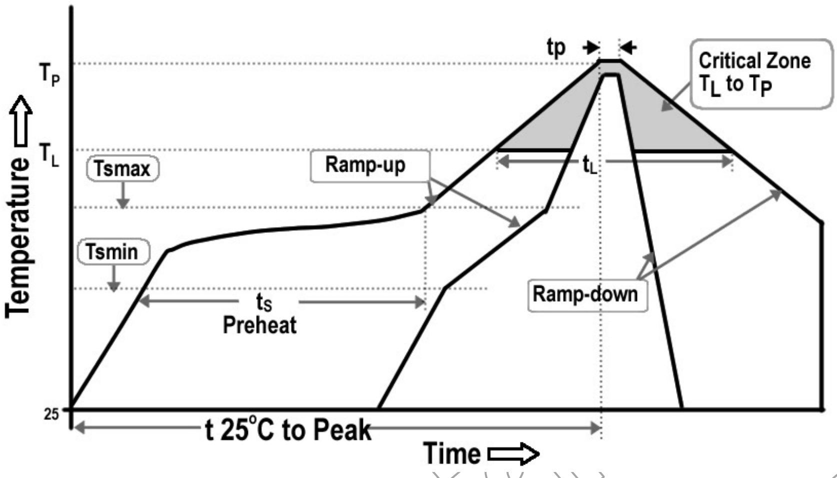


Figure 15: Reflow Temperature Profile

9.3 Maximum Reflow Times

All package reliability tests were performed and passed with a pre-condition procedure that repeat a reflow profile, which conforms to the requirements in Section 9.2, **three (3)** times.

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