QPA0016

13.75 – 14.5 GHz 15 Watt GaN Power Amplifier

Product Overview

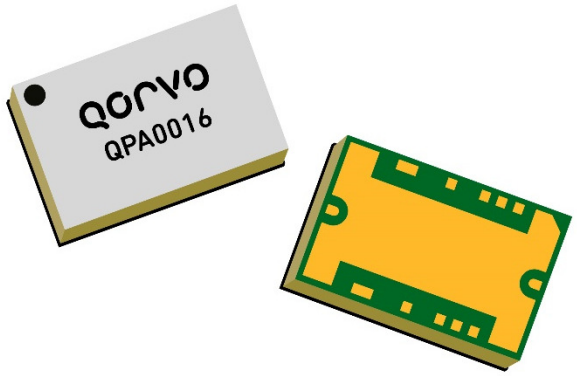
Qorvo's QPA0016 is a high power, packaged Ku-Band MMIC amplifier fabricated using Qorvo's production 0.15 um GaN-on-SiC process (QGaN15). The QPA0016 targets the 13.75-14.5 GHz Satcom band while providing 5-Watts of linear power with third-order intermodulation distortion products of 25 dBc. Furthermore, the QPA0016 can deliver output powers up to 15-Watts with 35 dB of small-signal gain and 32% power-added efficiency. The operating frequency can extend to 12.75-15.35 GHz if desired.

To simplify system integration, the QPA0016 is fully matched to 50 ohms with DC grounded I/O ports for optimum ESD performance. Also, there are on-chip blocking capacitors following the DC grounds on the input and output ports.

The QPA0016 is ideal for supporting communications and radar applications in both commercial and military markets.

The QPA0016 is 100% DC and RF tested to ensure compliance to electrical specifications.

Lead-free and RoHS compliant

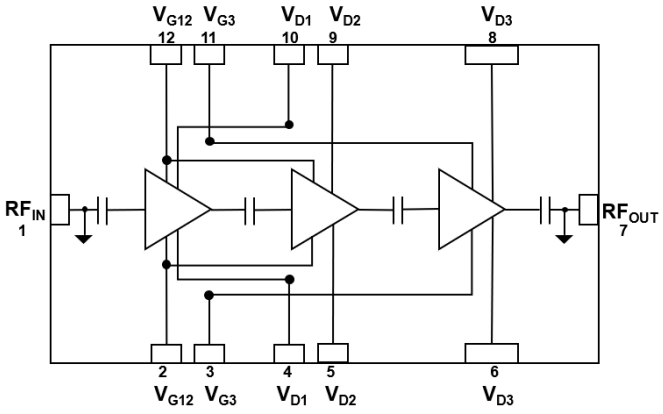


Key Features

- Frequency Range: 13.75 – 14.5 GHz
- Extended Frequency Range: 12.75 – 15.35 GHz
- Linear P_{OUT}: 37 dBm
- P_{OUT} (P_{IN} = 14 dBm): 42 dBm
- PAE (P_{IN} = 14 dBm): 32 %
- IM3 (P_{OUT_TOTAL} = 37 dBm): -25 dBc
- Small Signal Gain: 35 dB
- Bias: V_D = 24 V, I_{DQ} = 259 mA, V_G = -2.3 V typ. range
- Package Dimensions: 7.50 x 5.00 x 2.45 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Satellite Communications
- Datalinks

Ordering Information

Part No.	Description
QPA0016	15 Watt GaN PA Package
QPA0016TR7	200 pieces on a 7” reel (standard)
QPA0016EVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-4 V to 0 V
Drain Current (I_{D12}),1-sided feed	885 mA
Drain Current (I_{D3}), 1-sided feed	2400 mA
Drain Current Total (I_D),1-sided feed	3285 mA
Gate Current (I_G)	See p. 26
Power Dissipation (P_{DISS}), CW, T_{BASE} = 85 °C	45 W
Input Power (P_{IN}), 50 Ω, CW, V_D = 24 V, I_{DQ} = 259 mA, T_{BASE} = 85 °C	21 dBm
Input Power (P_{IN}), 3:1 VSWR, CW, V_D = 24 V, I_{DQ} = 259 mA, T_{BASE} = 85 °C	18 dBm
Mounting Temperature (30 seconds)	260 ºC
Storage Temperature	-55 to +150 ºC

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter		Min	Typ.	Max	Unit
Drain Voltage (V_D) – CW			24		V
Drain Current, Quiescent (I_{D12})			131		mA
Drain Current, Quiescent (I_{D3})			128		mA
Drain Current Total, Quiescent (I_{DQ} = I_{D12} + I_{D3})			259		mA
Drain Current Total, RF (I_{D_Drive})		See plot page 5, 6, 10, 13, 16			mA
Gate Voltage Typ. Range (V_G)		–1.6 to -3			V
Gate Current, RF (I_{G_Drive})		See plot page 6			mA
P_{IN}(1)	T_{BASE} = -40 °C		12		dBm
	T_{BASE} = +25 °C		14		
	T_{BASE} = +85 °C		18		
Operating Temp. (T_{BASE}) (2)		–40		+85	ºC

1. Compression is varied due to thermal, see p. 7, 8
2. T_{BASE} is back side of QPA0016 (see p. 29, offset temperature based on Qorvo's EVB design for reference).

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

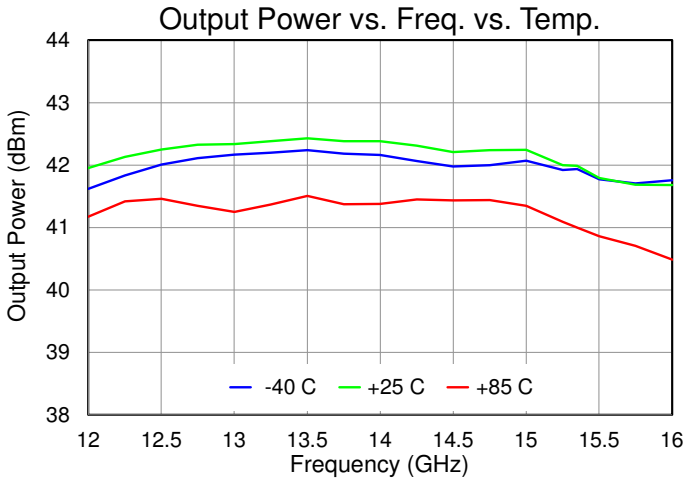
Parameter	Conditions (1) (2)	Min	Typ.	Max	Units
Operational Frequency Range		13.75 (3)		14.5 (3)	GHz
Linear Output Power			37		dBm
Output Power, P_{OUT}	P_{IN} = 14 dBm		42		dBm
Power Added Efficiency, PAE	P_{IN} = 14 dBm		32		%
3RD Intermodulation Products, IM3	P_{OUT_TOTAL} = 37 dBm ($P_{OUT/TONE}$ = 34 dBm)		-25		dBc
5TH Intermodulation Products, IM5			-40		
Small Signal Gain, S21	P_{IN} = -30 dBm		35		dB
Input Return Loss, IRL			15		
Output Return Loss, ORL			6		
P_{SAT} Temperature Coefficient	T_{DIFF} = 25 ºC to 85 ºC; P_{IN} = 14 dBm		-0.05		dBm/ºC
S21 Temperature Coefficient	T_{DIFF} = 25 ºC to 85 ºC		-0.10		dB/ºC

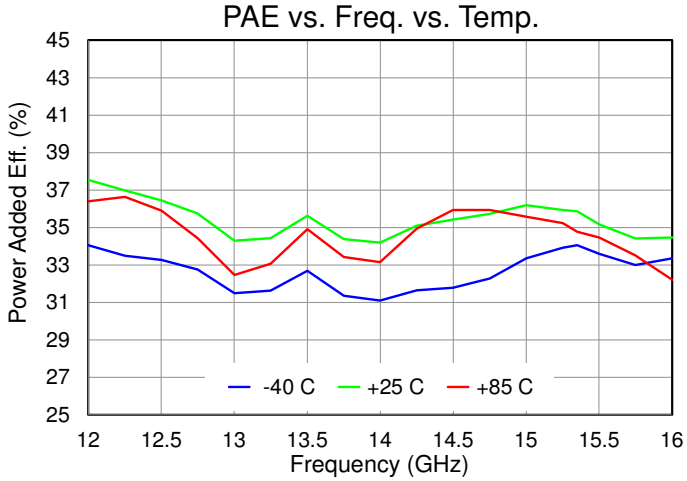
Notes:

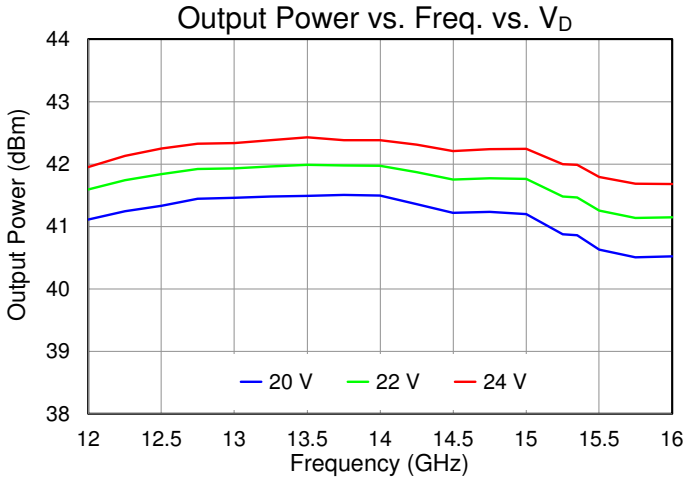
1. Test conditions unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), V_G = -2.3 V +/- 0.7V typical, T_{BASE} = +25ºC, Z_0 = 50 Ω (reference planes are at QPA0016).
2. T_{BASE} is back side of QPA0016 (see page 28, offset temperature based on Qorvo's EVB design for reference).
3. Extended frequency range: 12.75 – 15.35 GHz

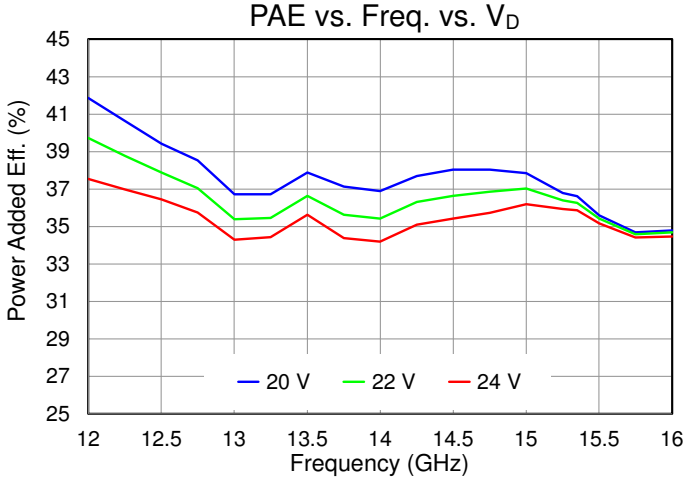
Performance Plots – Large Signal (CW)

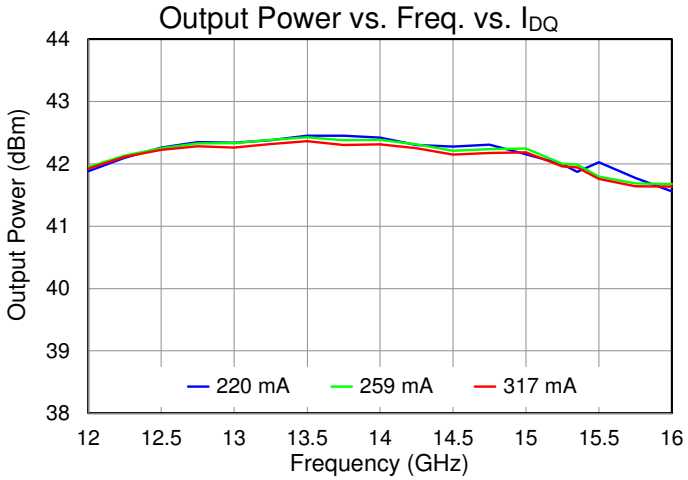
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), P_{IN} = 14 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

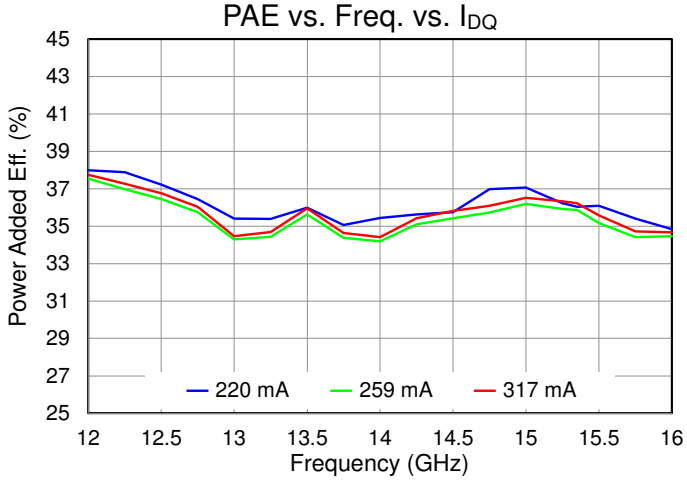












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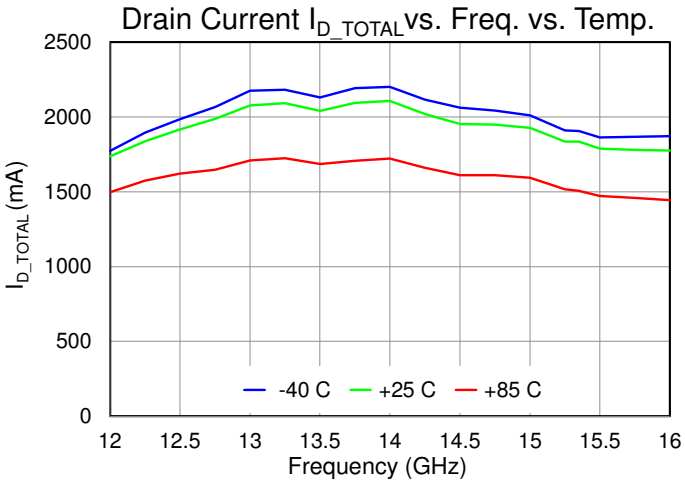

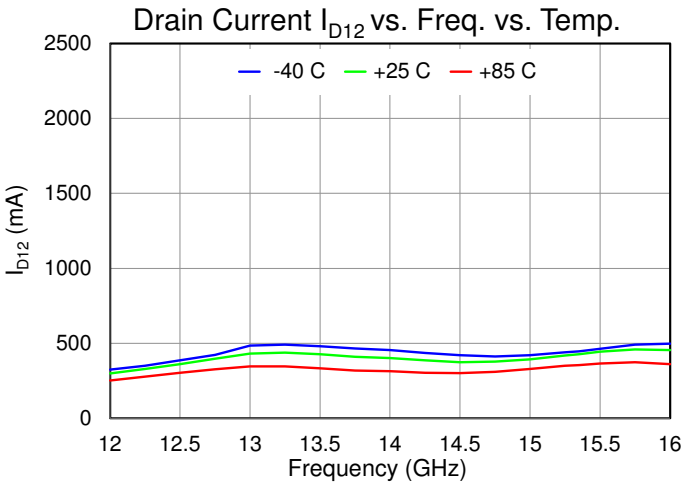

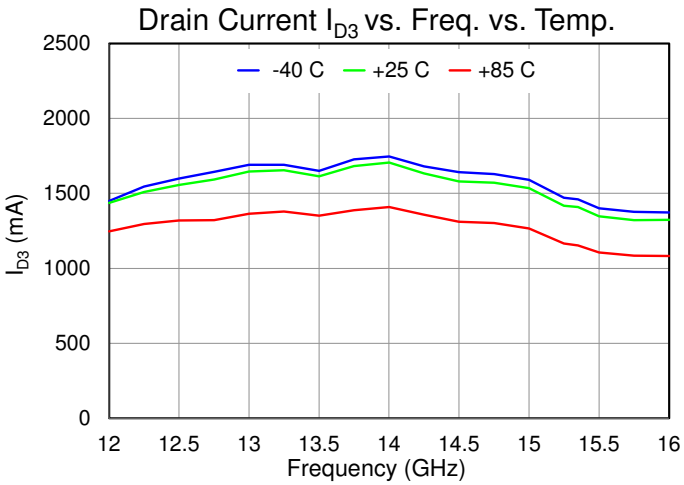

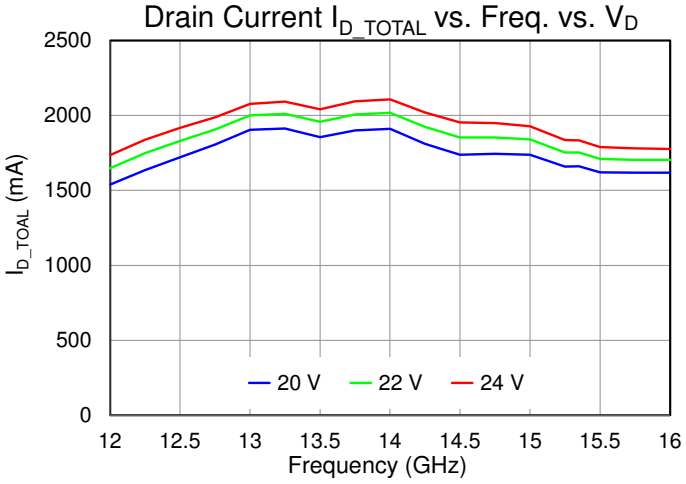

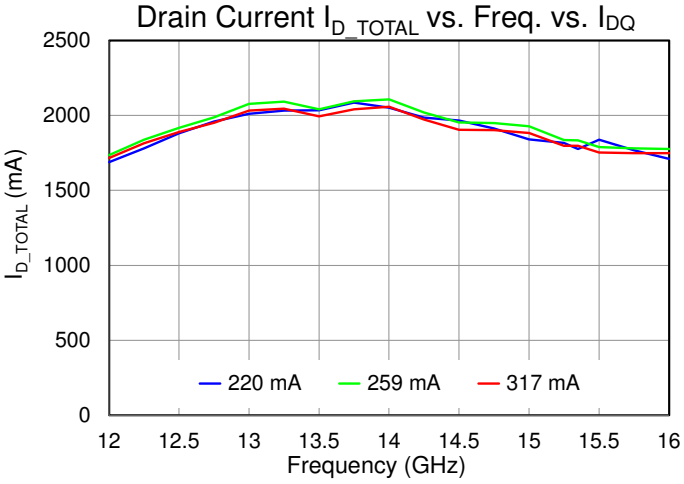

Performance Plots – Large Signal (CW)

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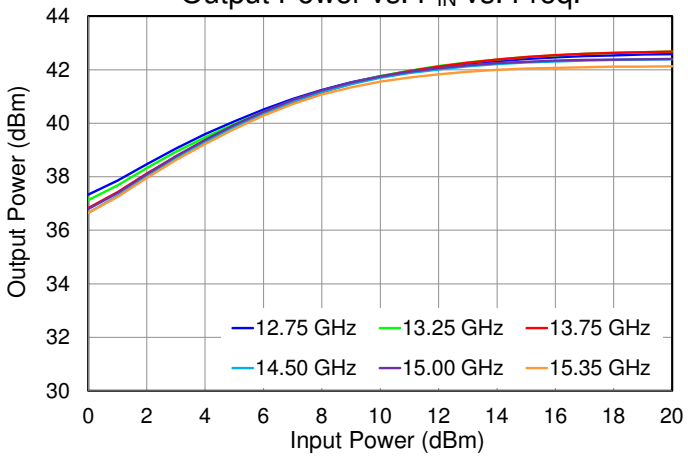
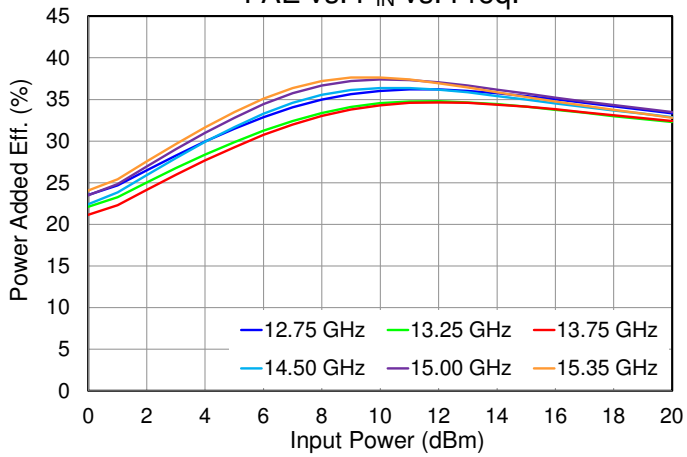
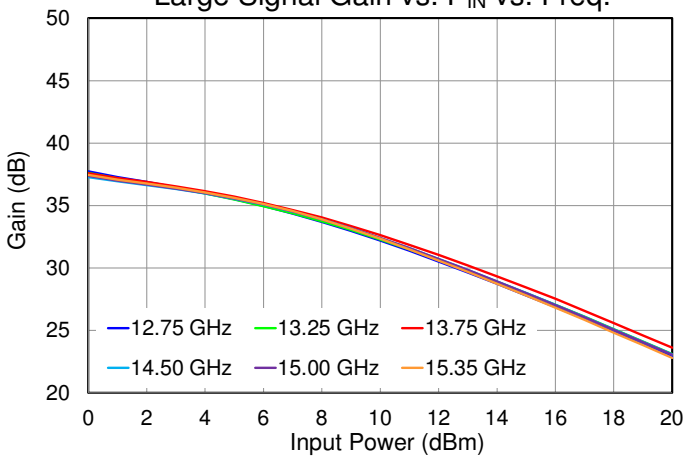
Output Power vs. P_{IN} vs. Freq.



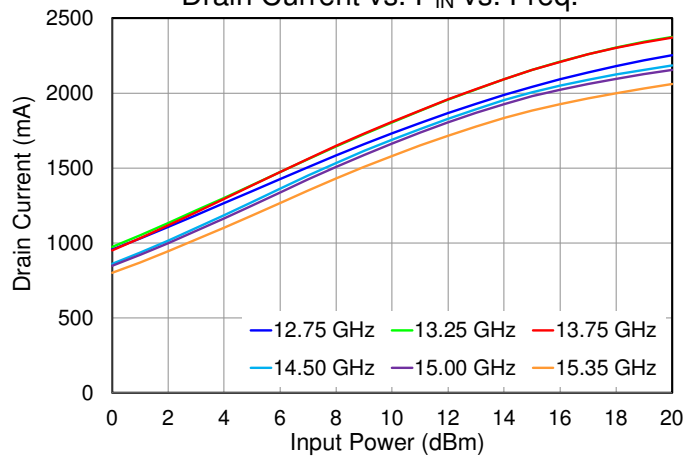
PAE vs. P_{IN} vs. Freq.



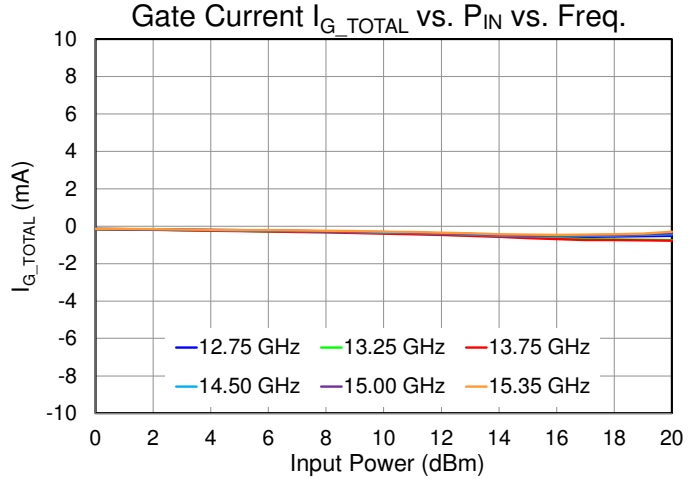
Large Signal Gain vs. P_{IN} vs. Freq.



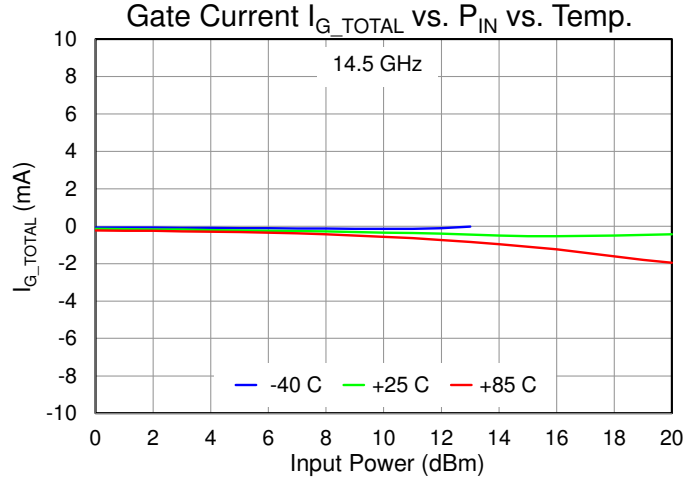
Drain Current vs. P_{IN} vs. Freq.



Gate Current I_{G_TOTAL} vs. P_{IN} vs. Freq.



Gate Current I_{G_TOTAL} vs. P_{IN} vs. Temp.



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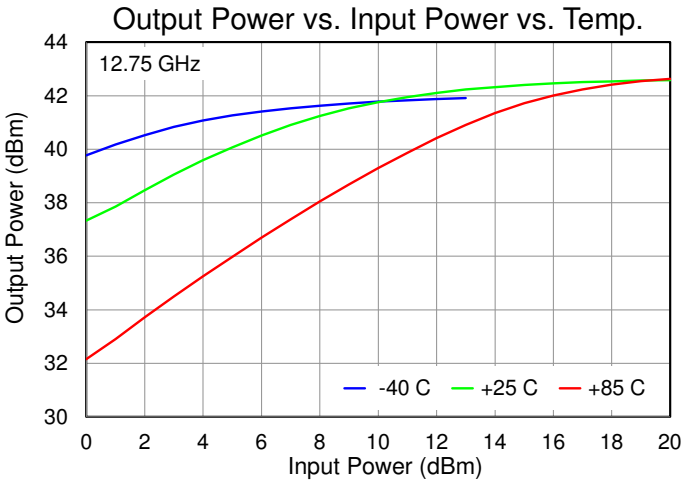

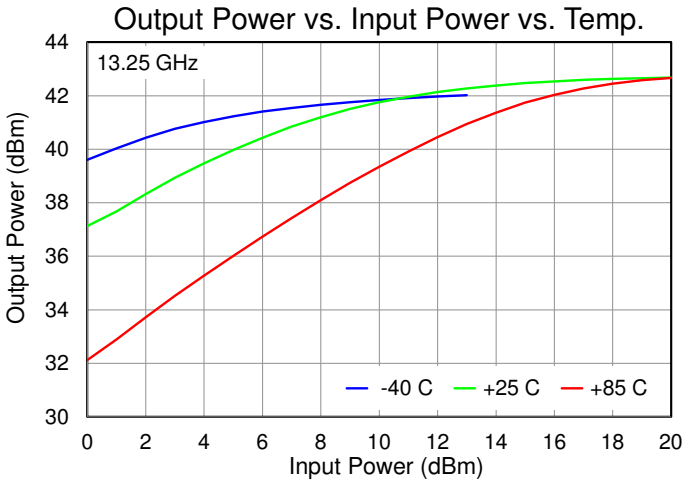

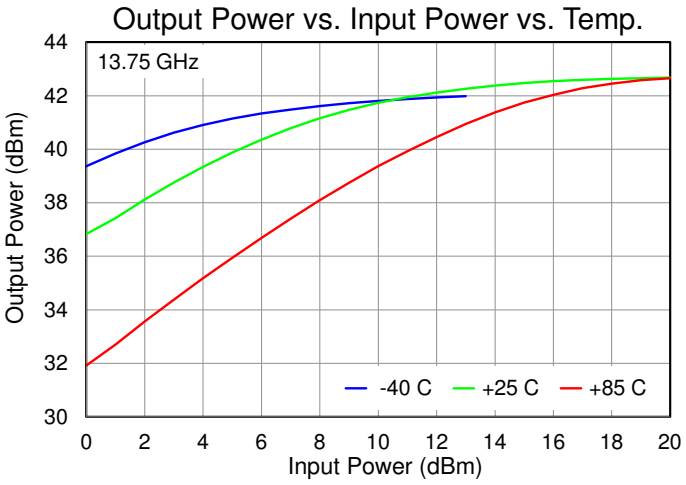

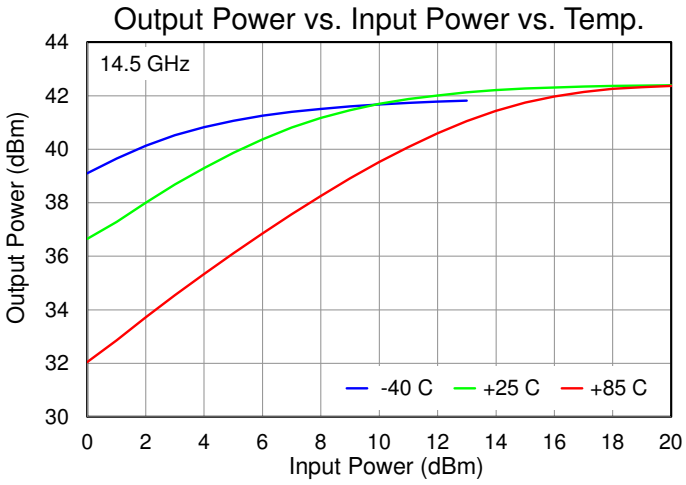

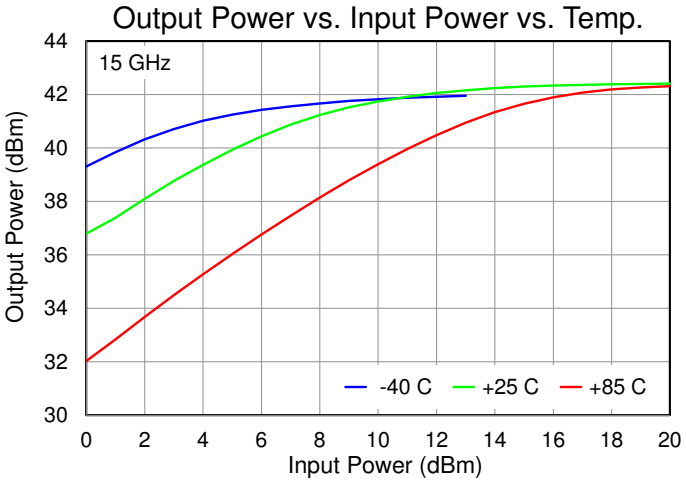

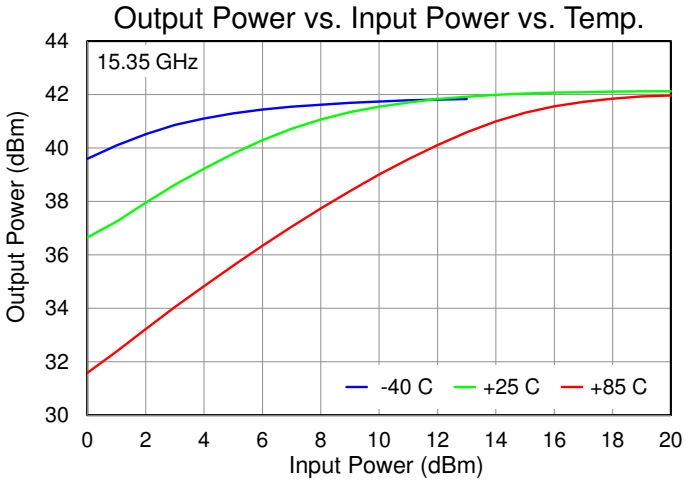

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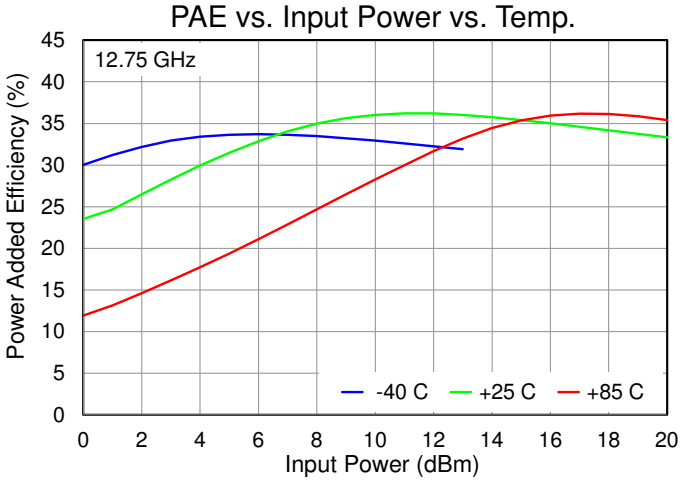

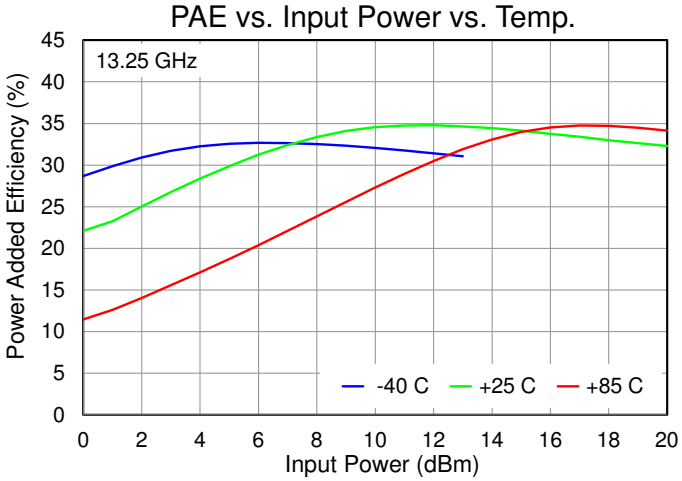

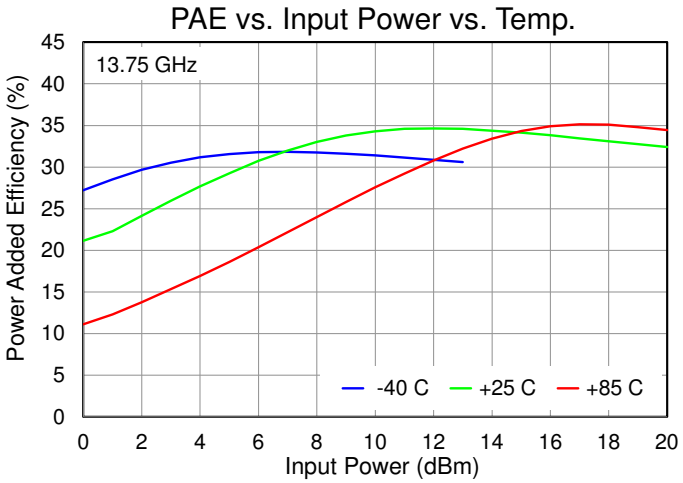

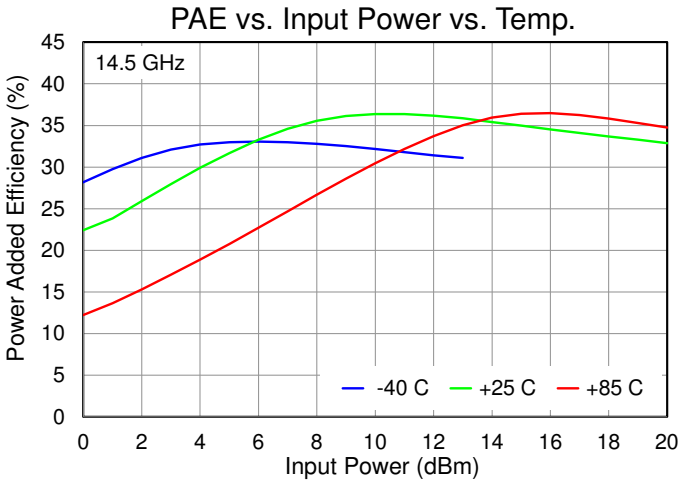

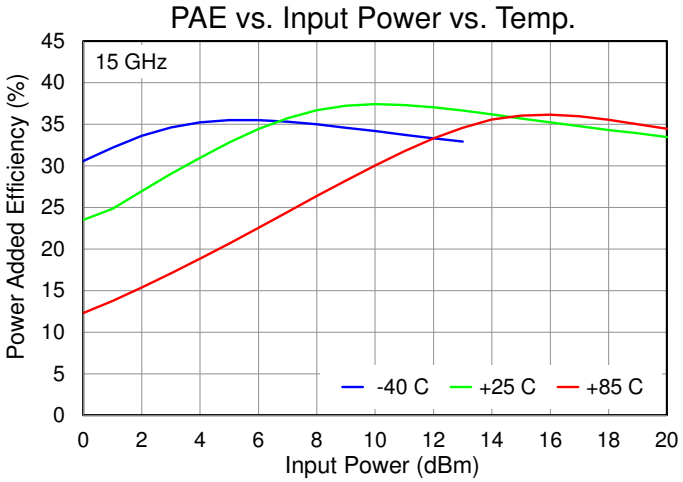

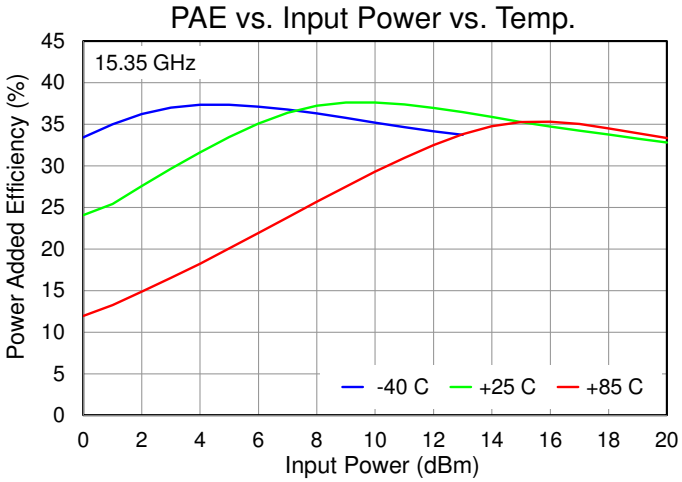

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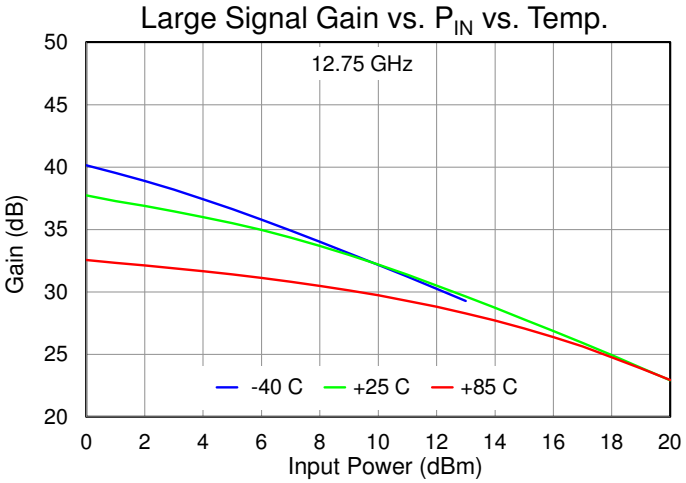

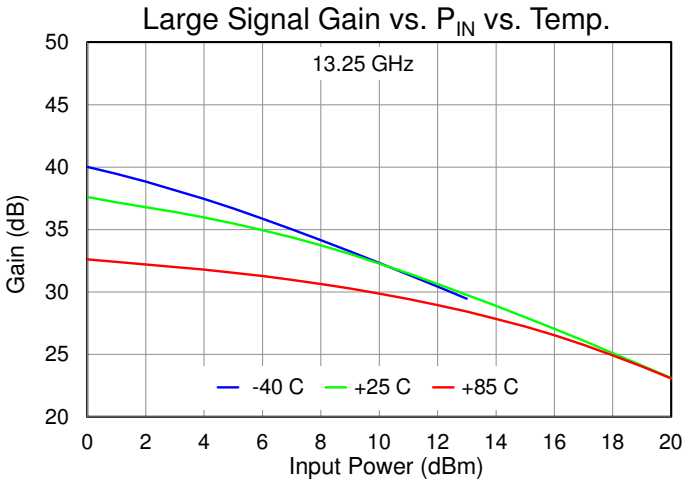

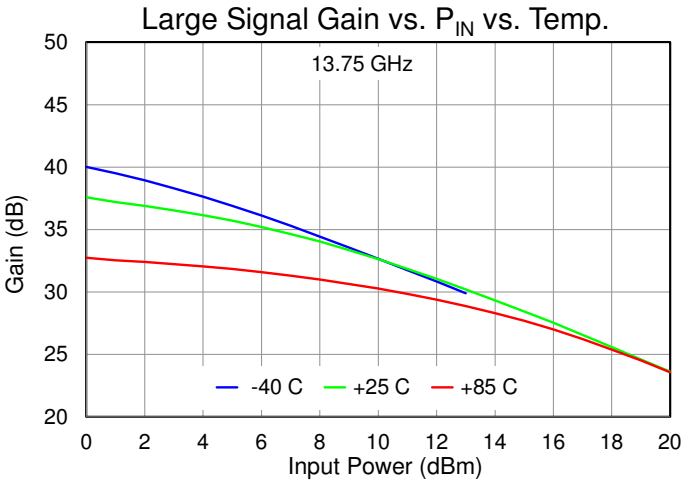

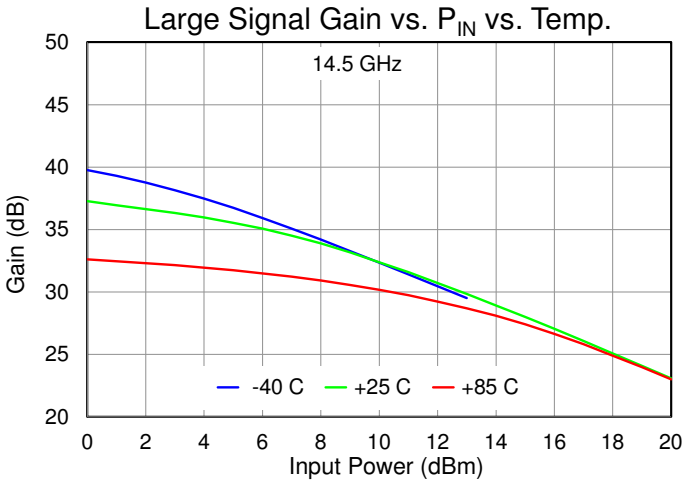

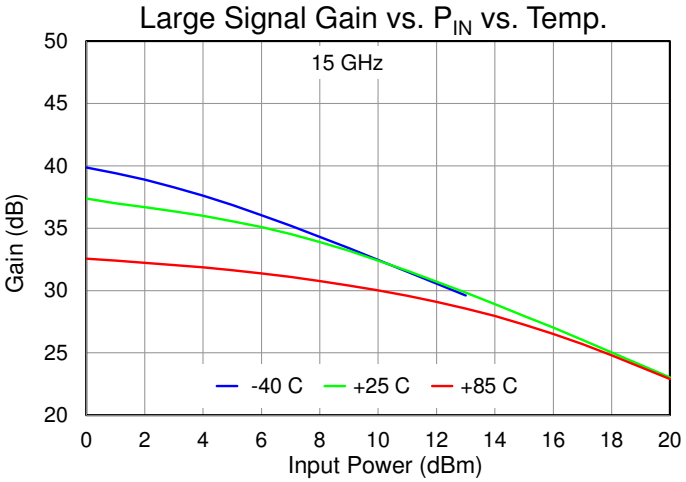

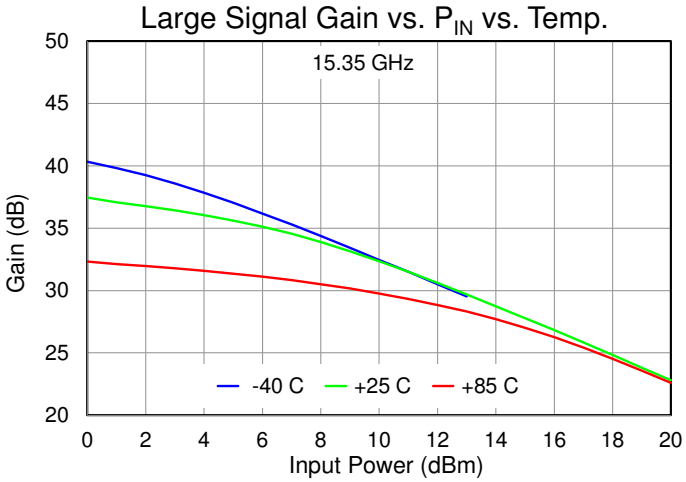

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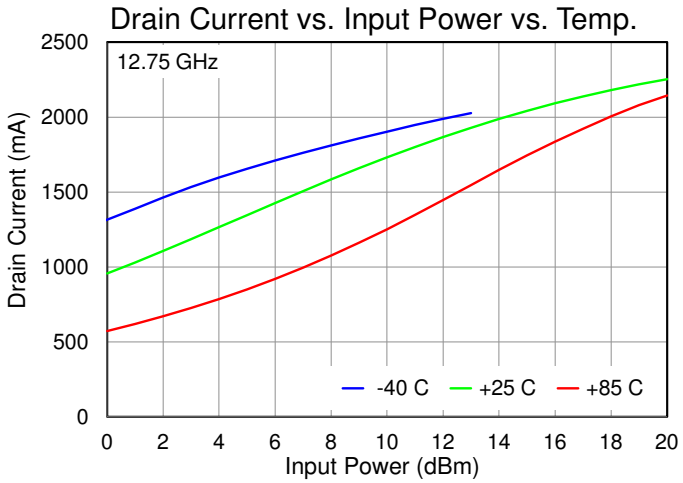

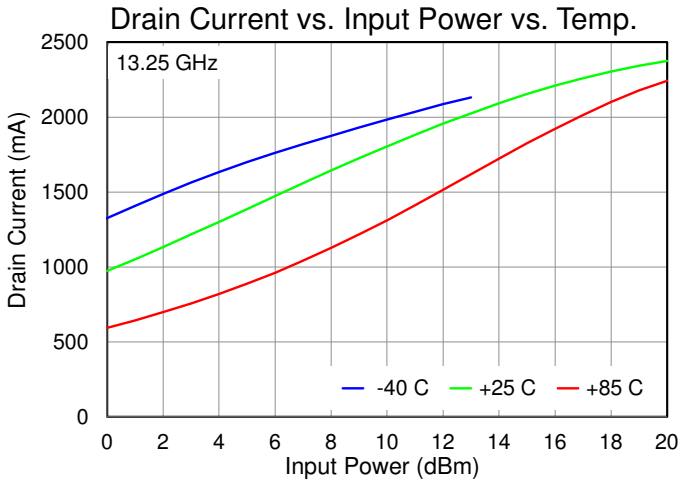

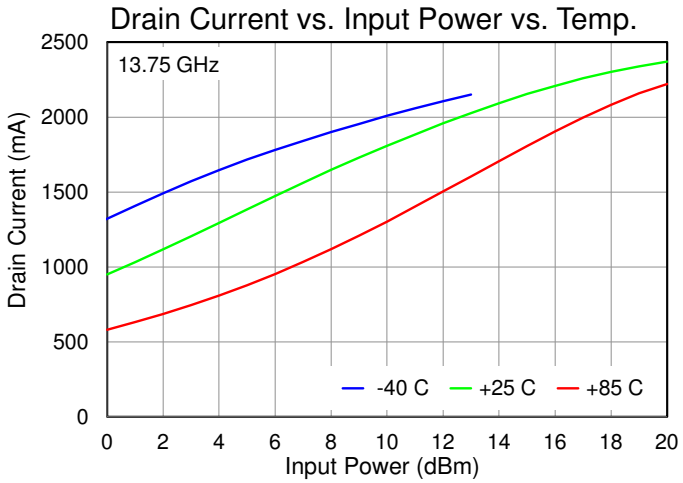

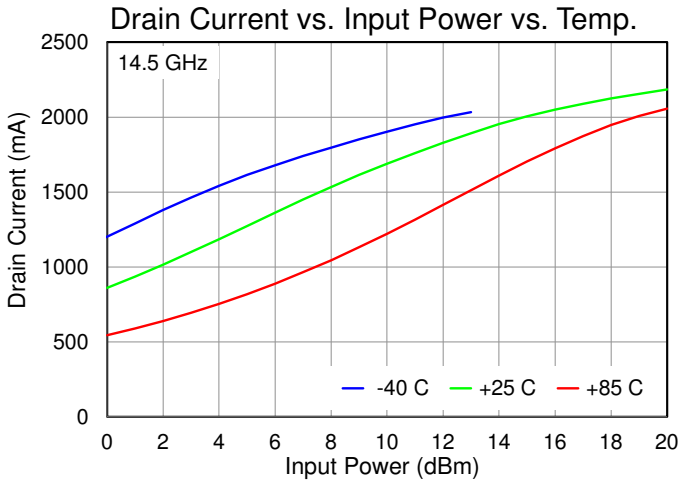

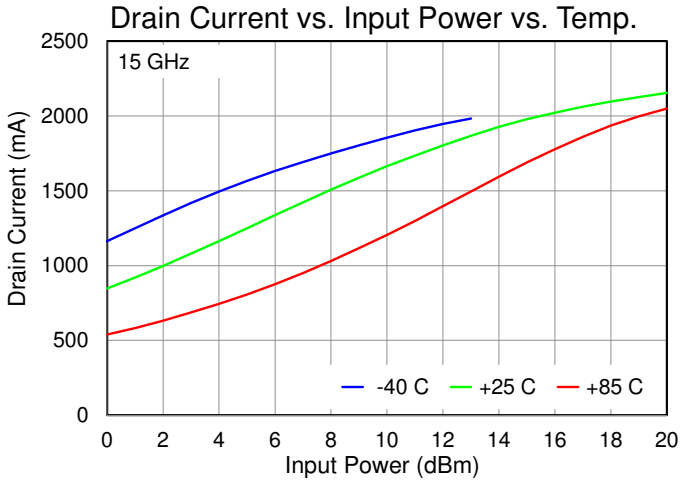

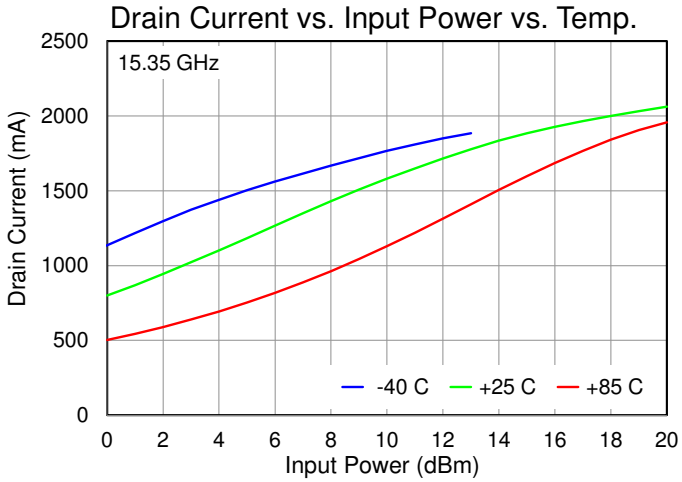

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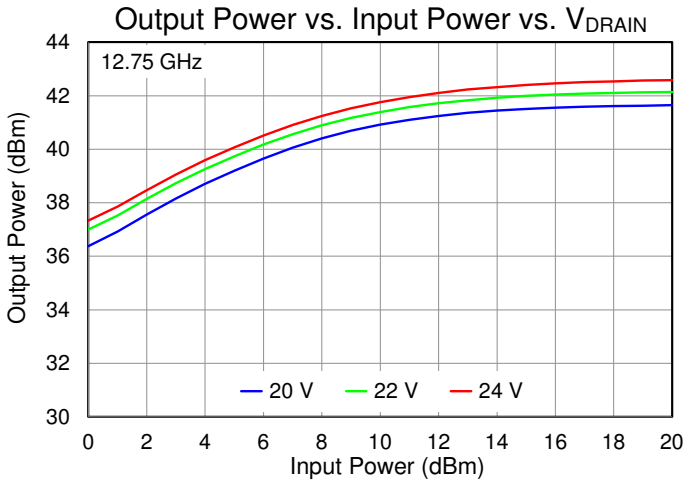
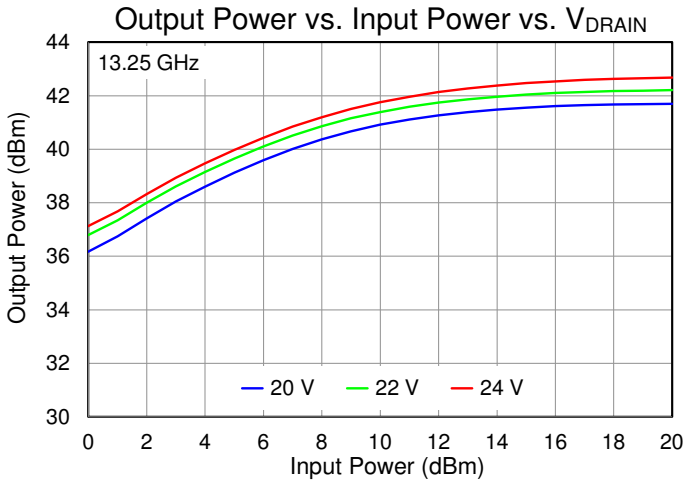
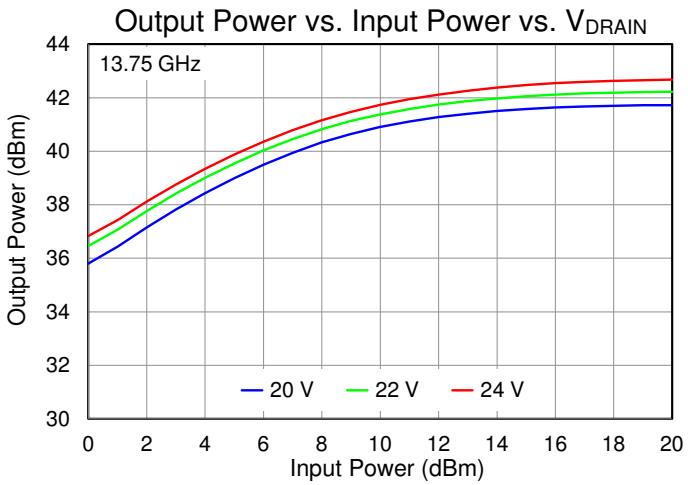
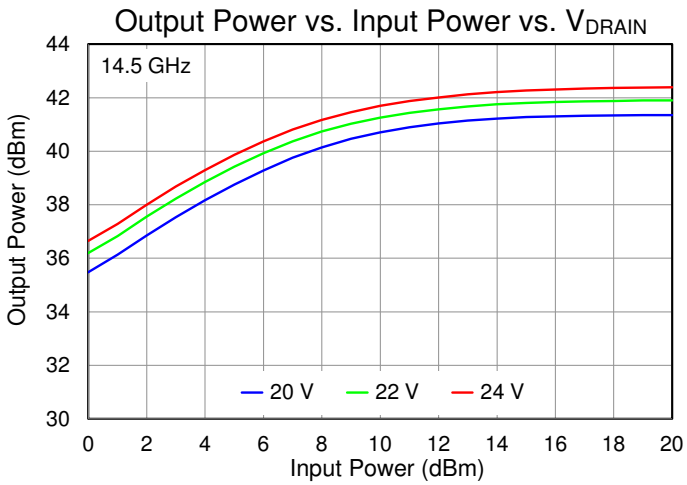
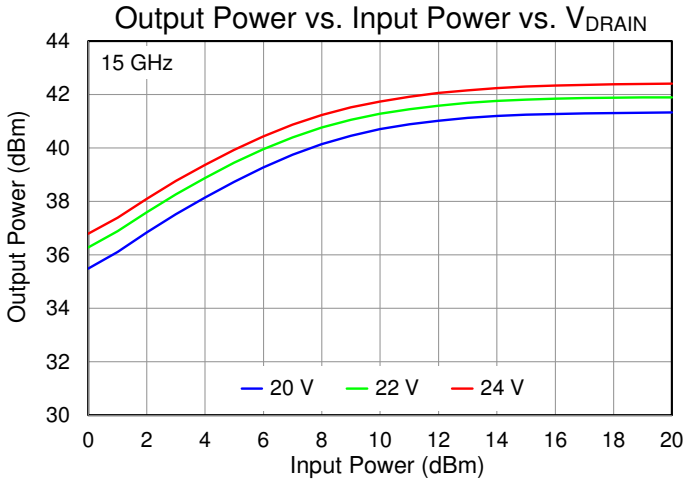
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), P_{IN} = 14 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

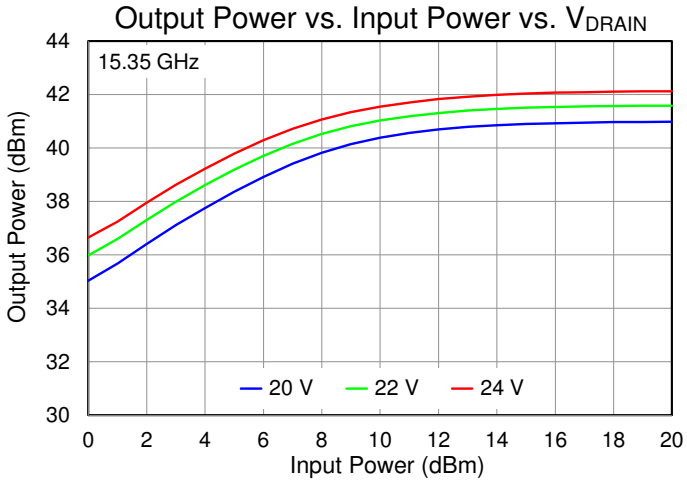






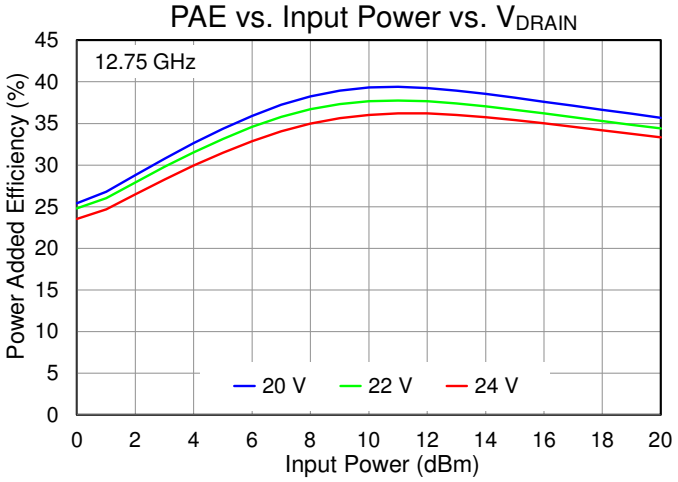


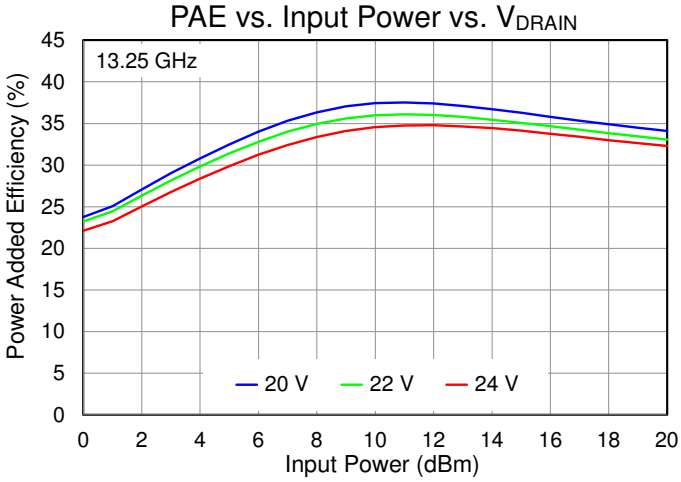


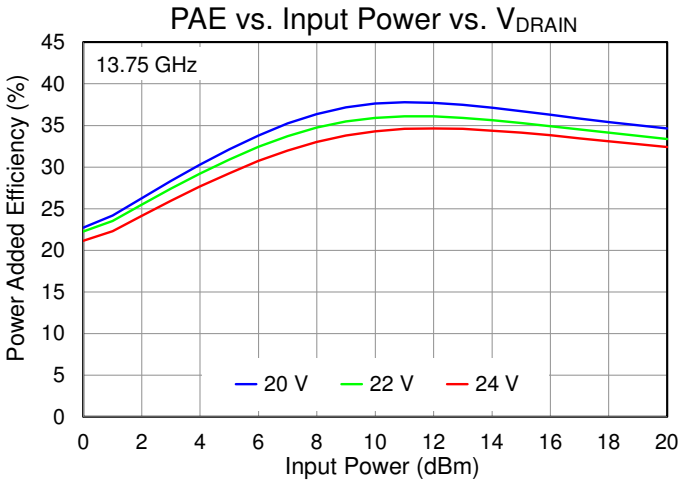


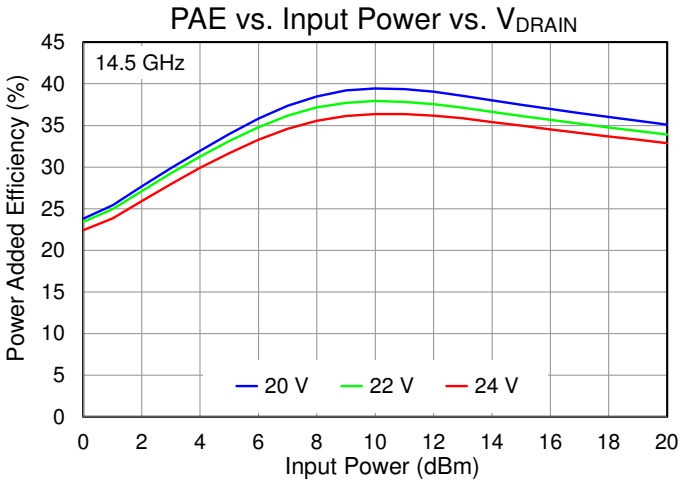
Performance Plots – Large Signal (CW)

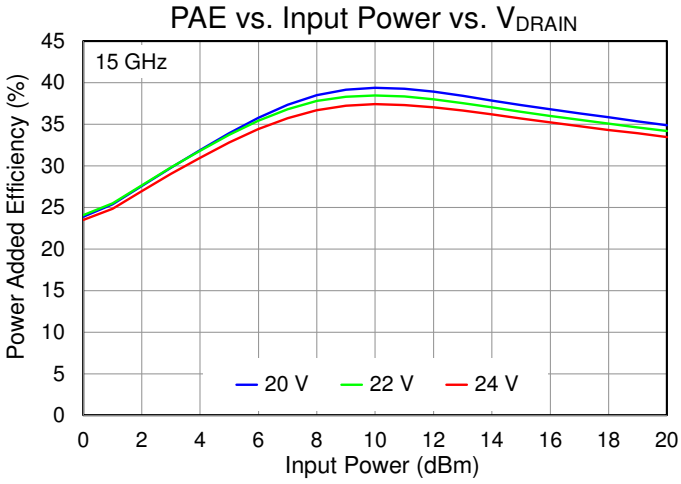
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), P_{IN} = 14 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

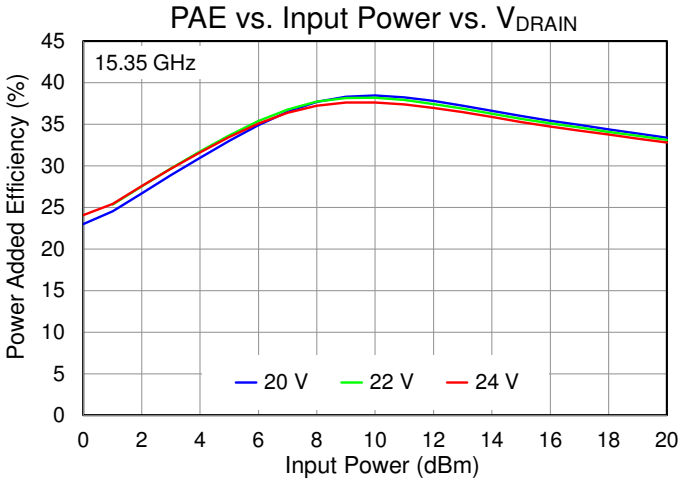






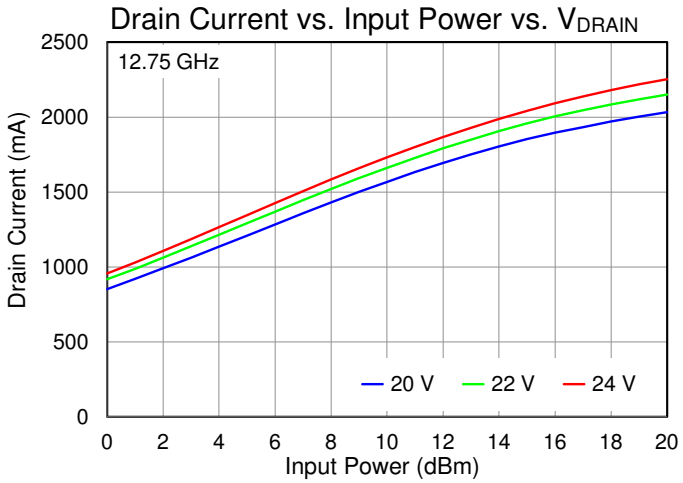


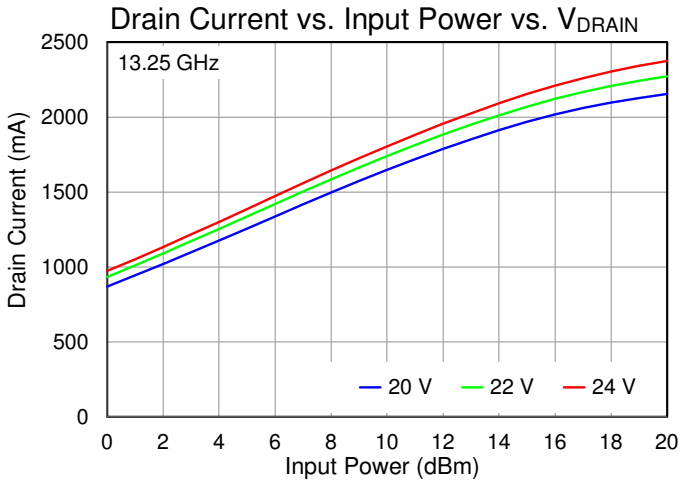


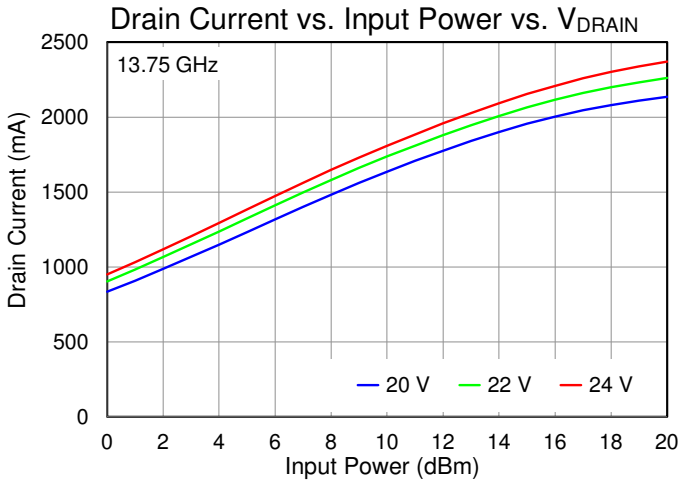


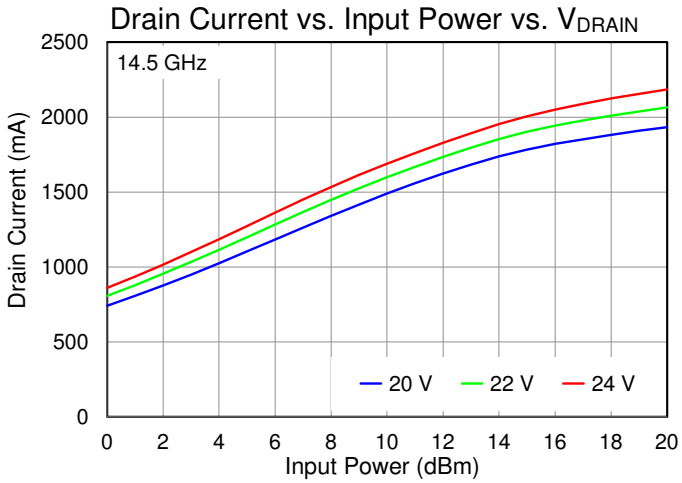
Performance Plots – Large Signal (CW)

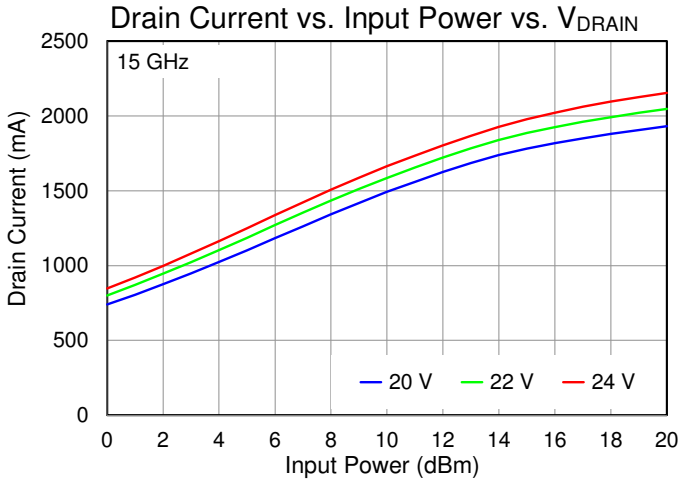
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), P_{IN} = 14 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

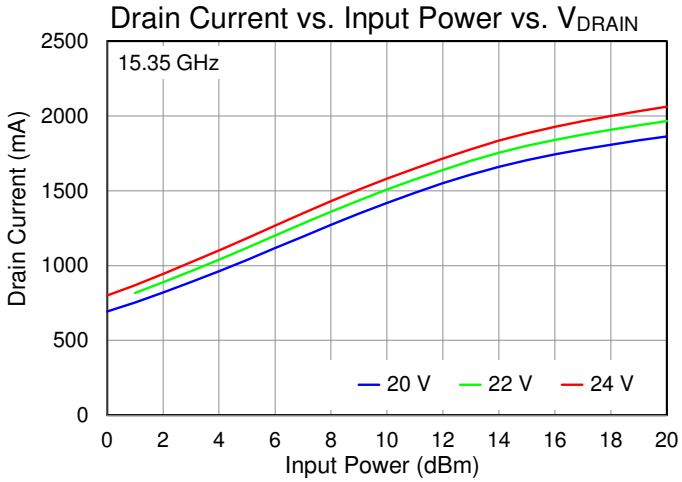






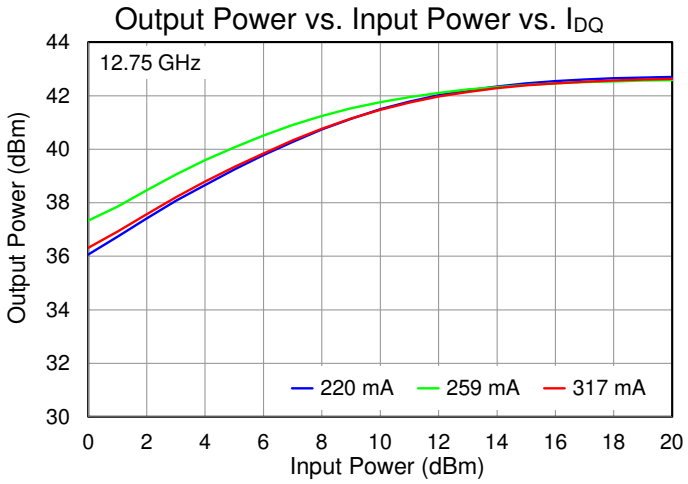


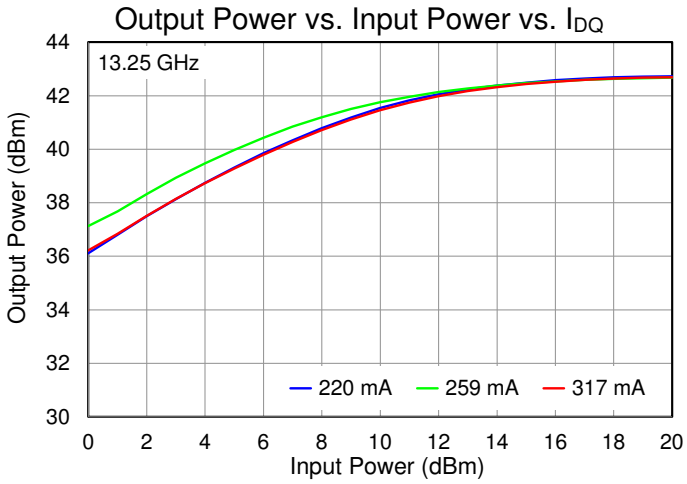


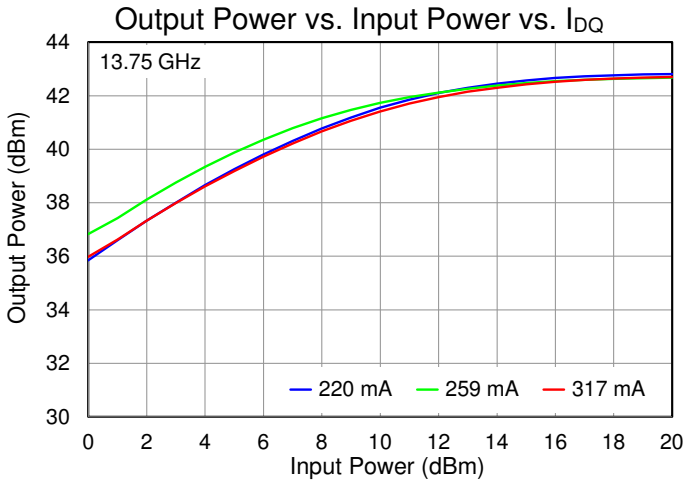


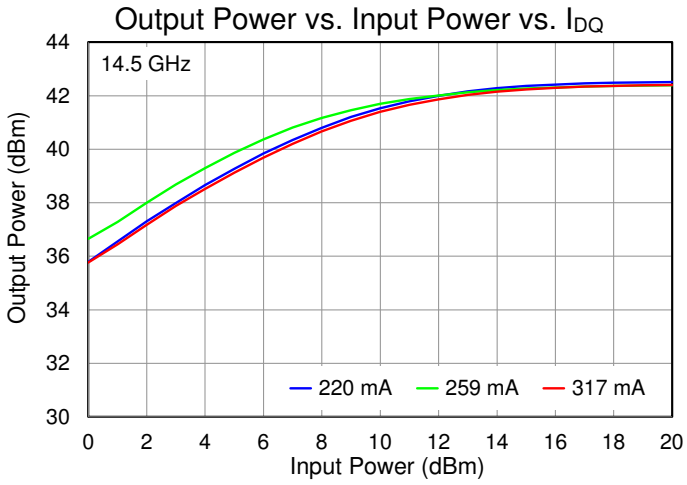
Performance Plots – Large Signal (CW)

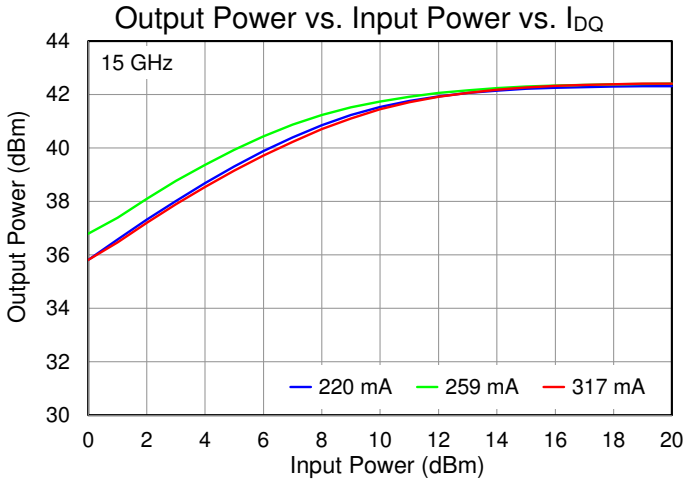
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), P_{IN} = 14 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

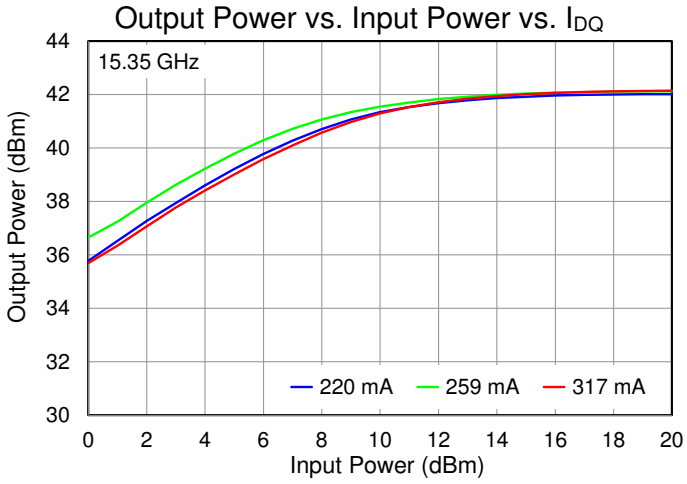






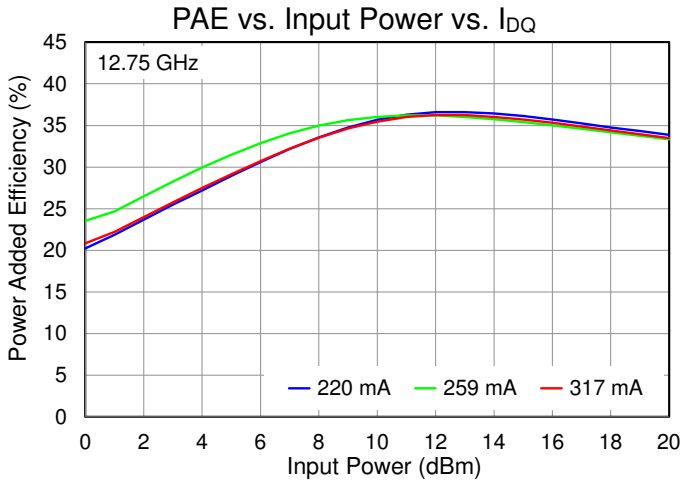


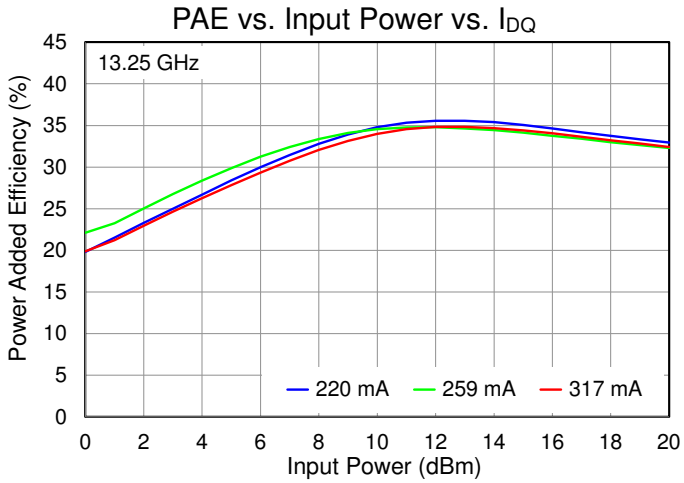


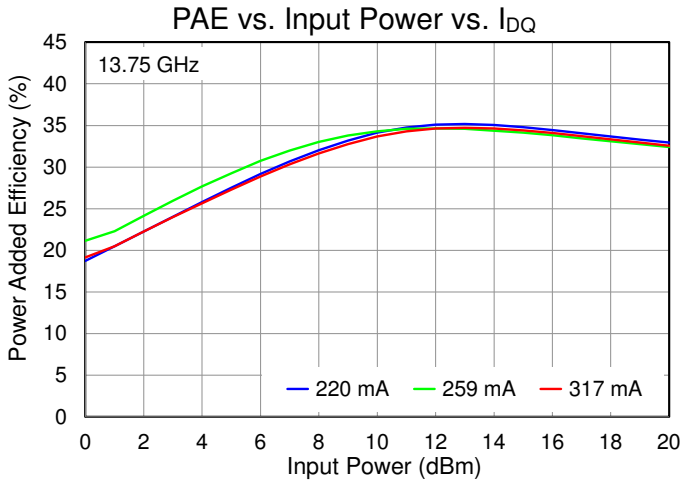


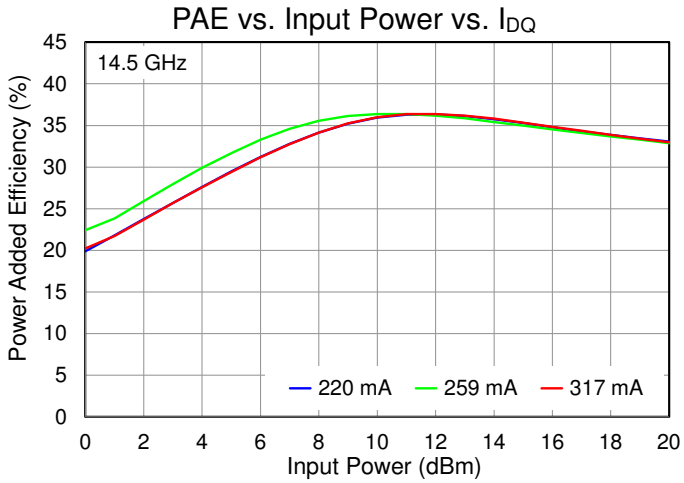
Performance Plots – Large Signal (CW)

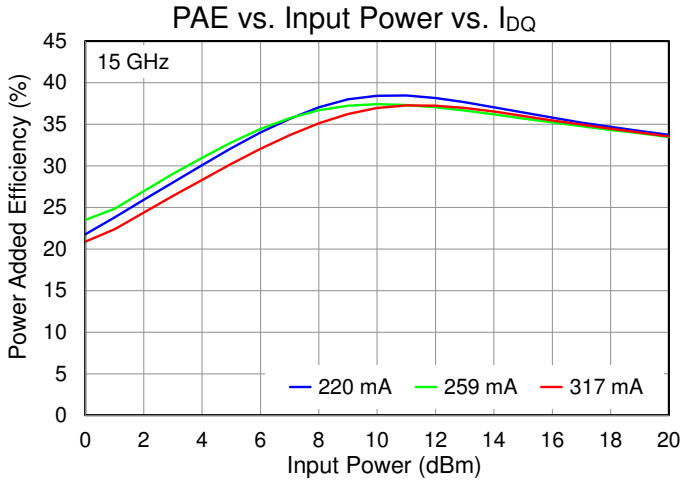
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), P_{IN} = 14 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

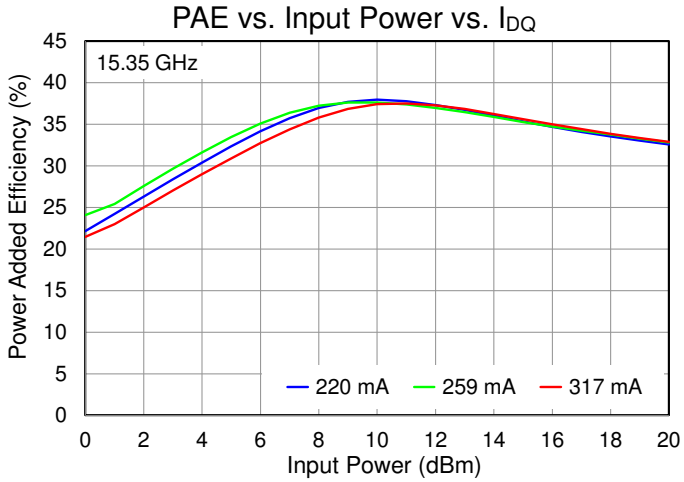






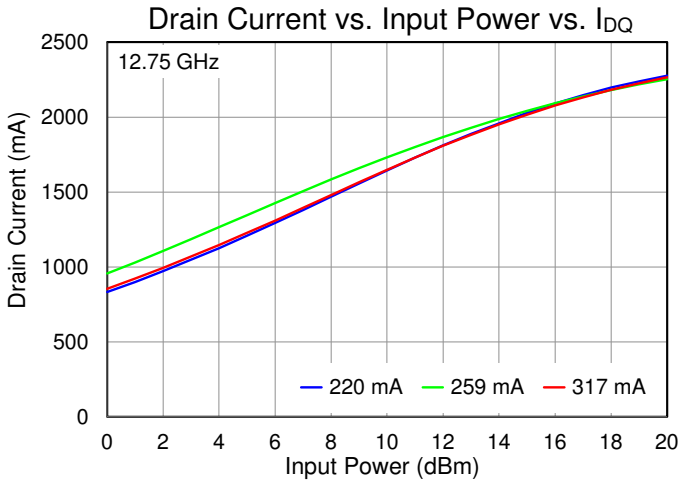


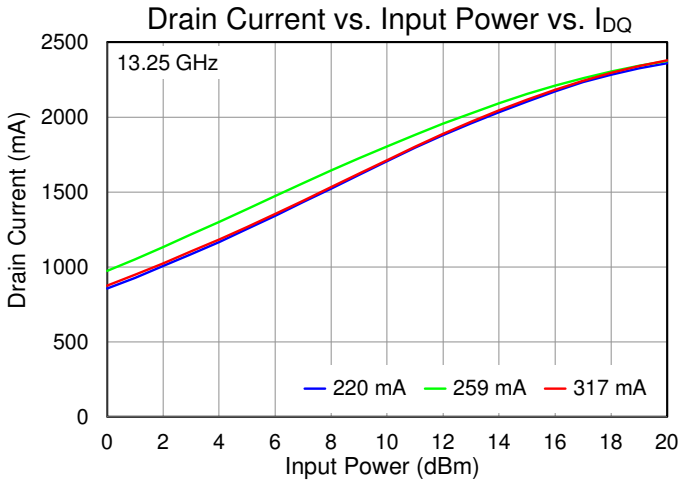


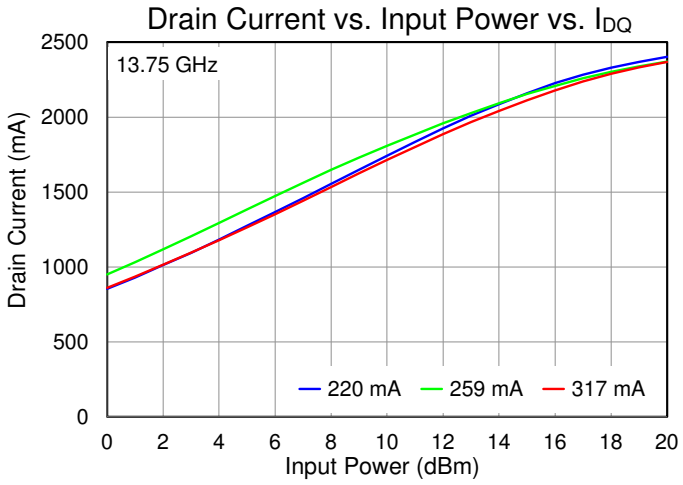


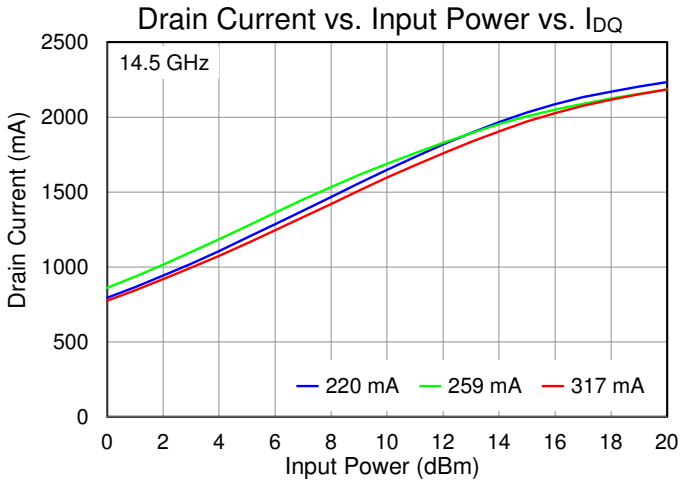
Performance Plots – Large Signal (CW)

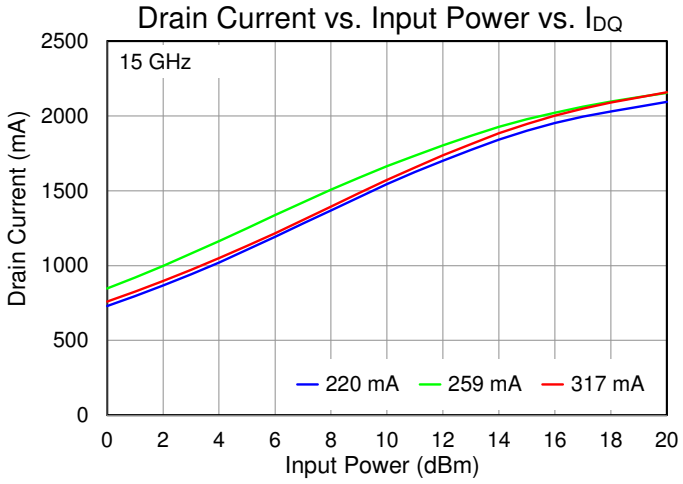
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), P_{IN} = 14 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

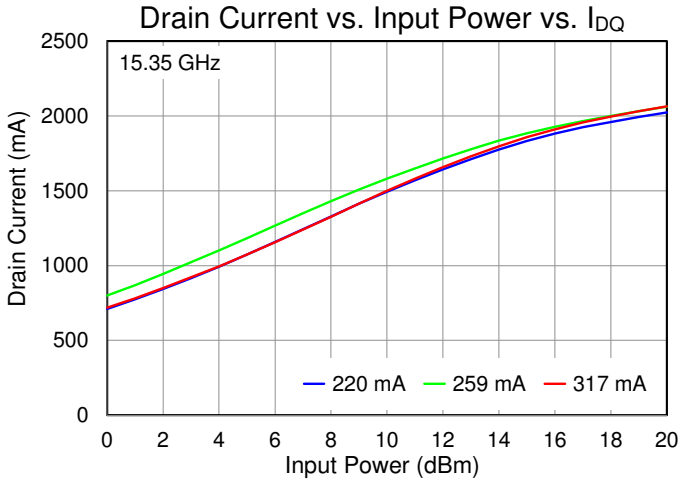






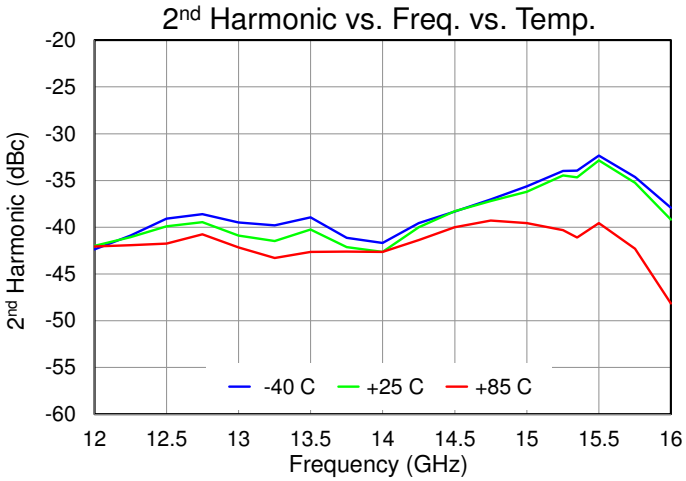


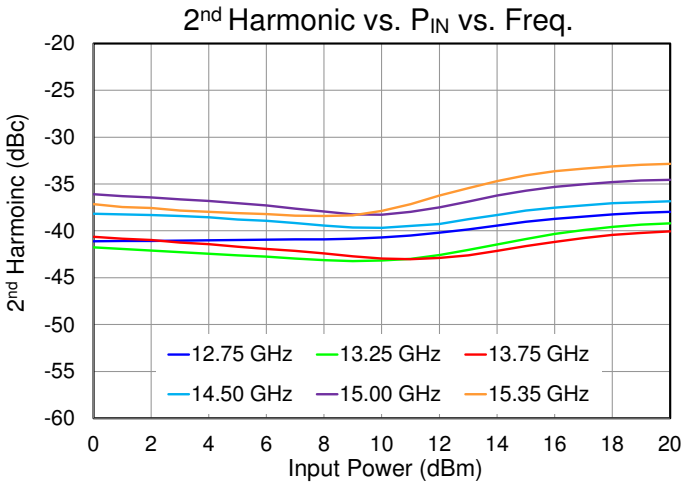


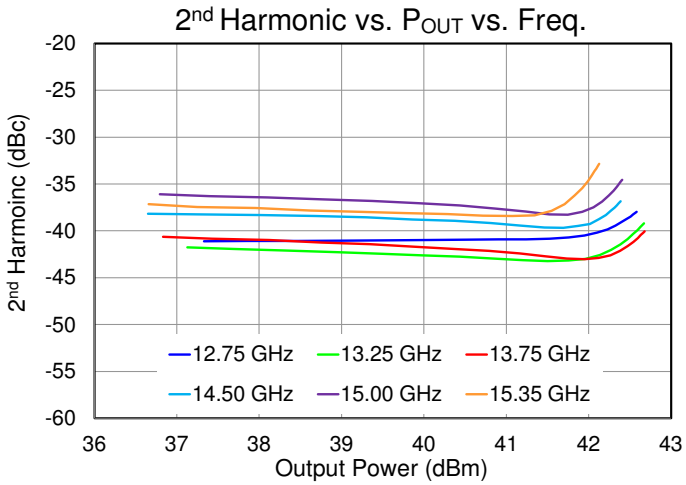


Performance Plots – Harmonics (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

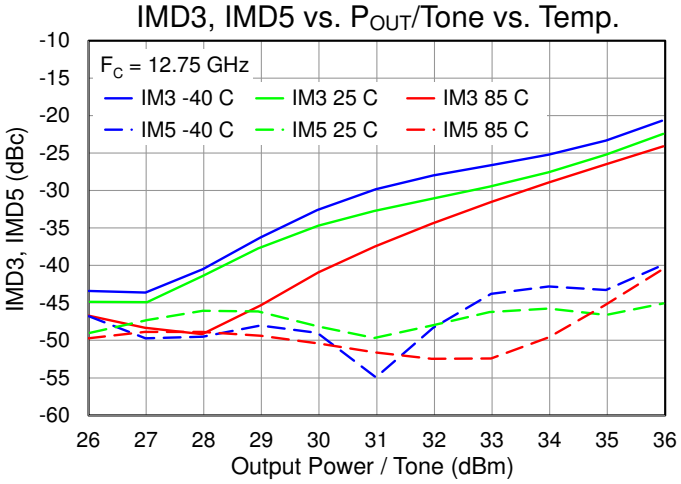


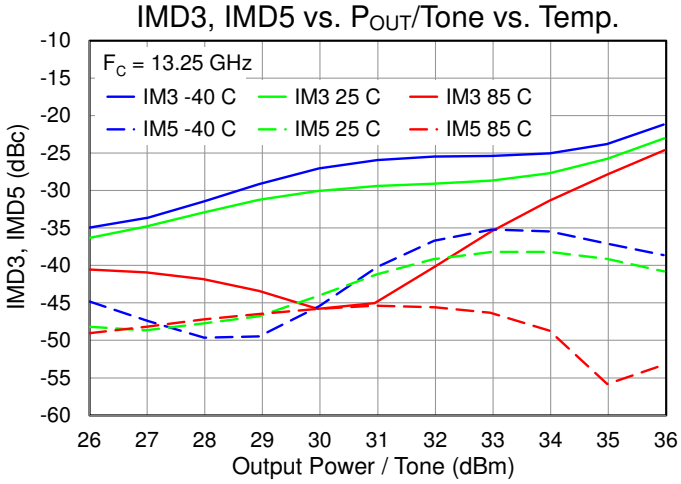


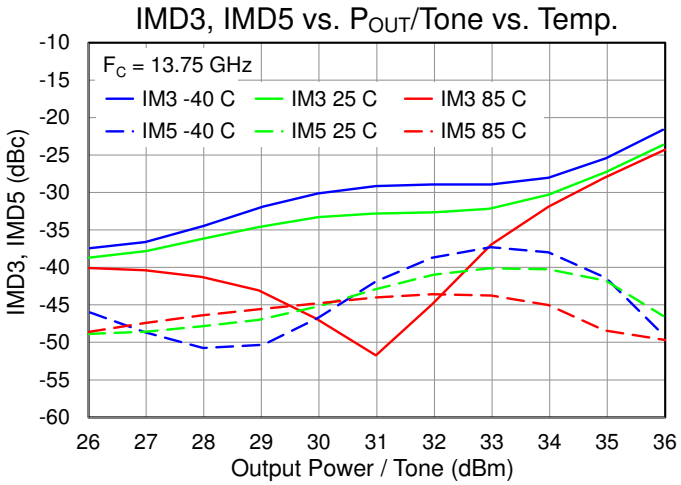


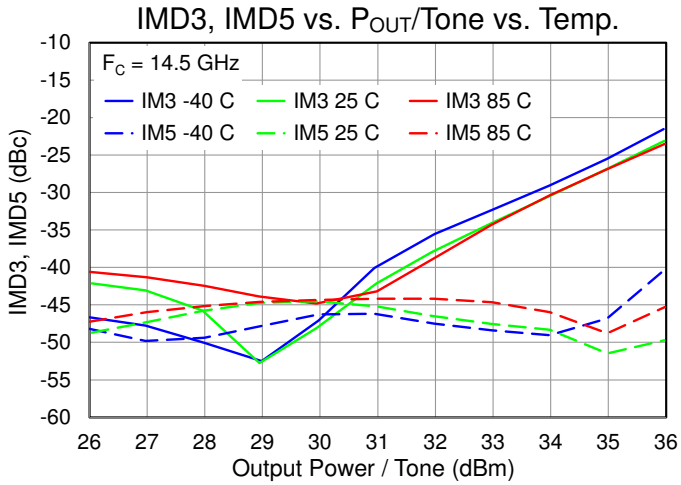
Performance Plots – Linearity (CW)

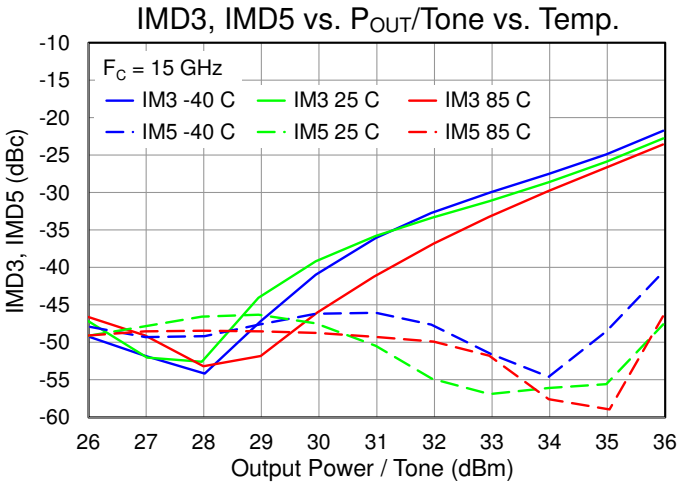
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), Tone Spacing = 20 MHz, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

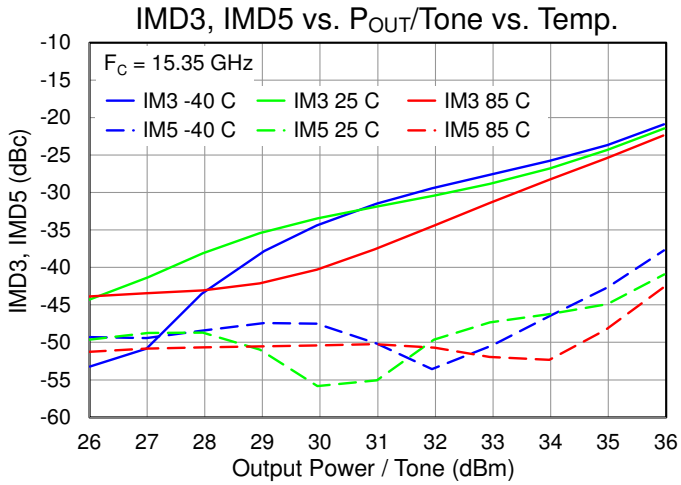






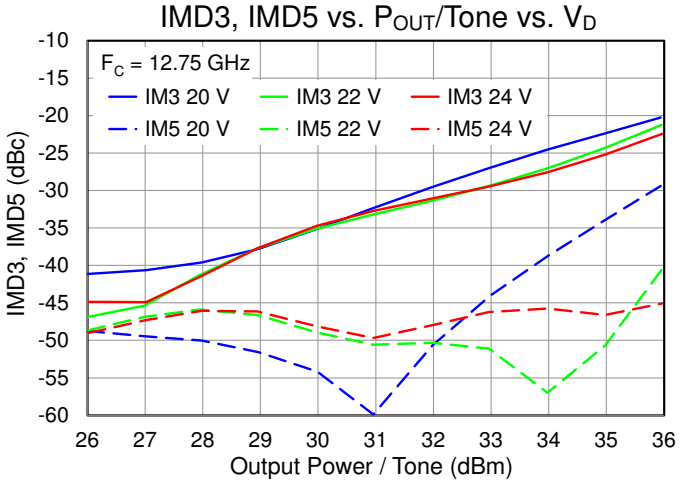


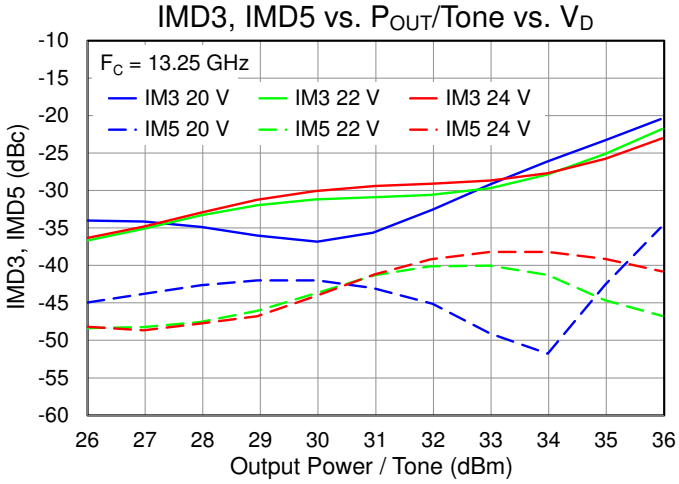


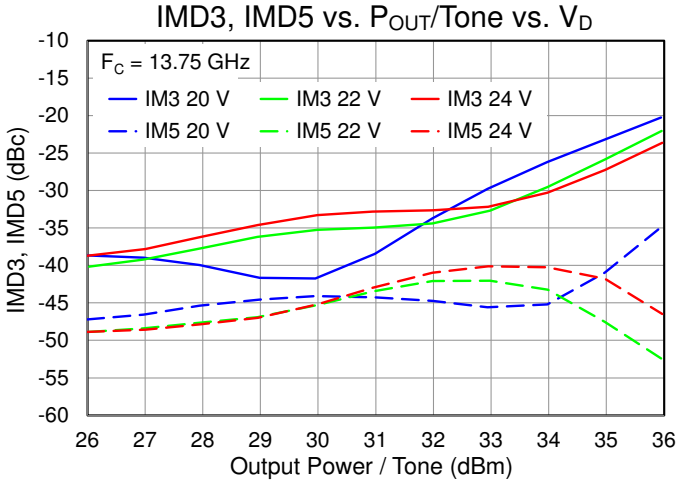


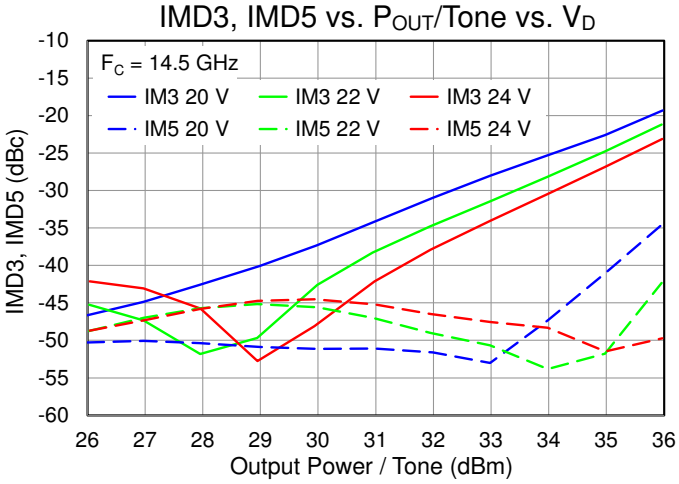
Performance Plots – Linearity (CW)

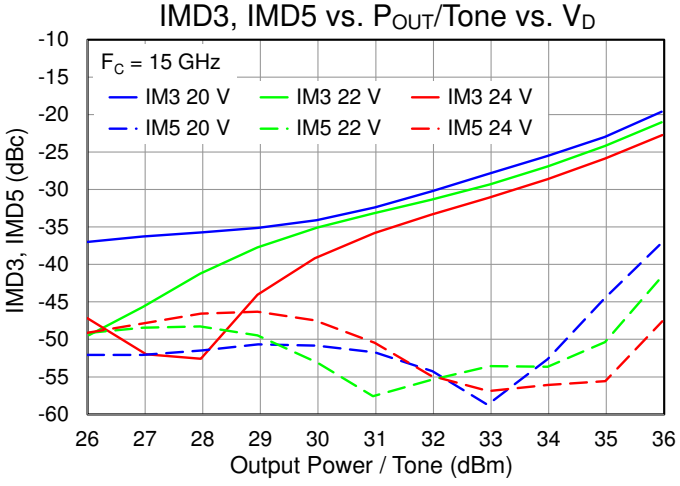
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), Tone Spacing = 20 MHz, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

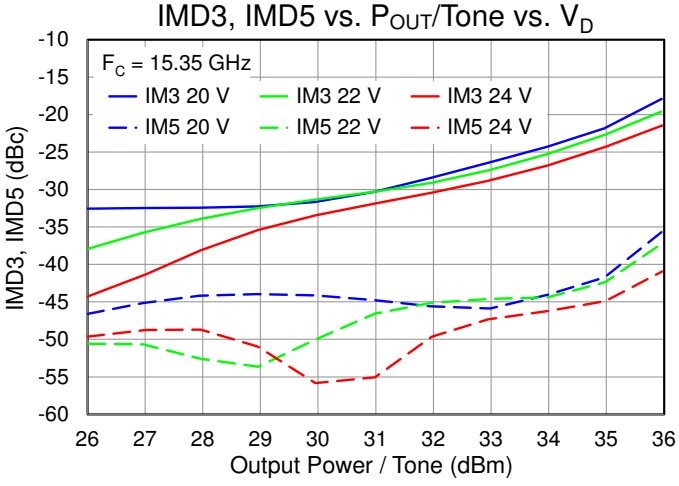








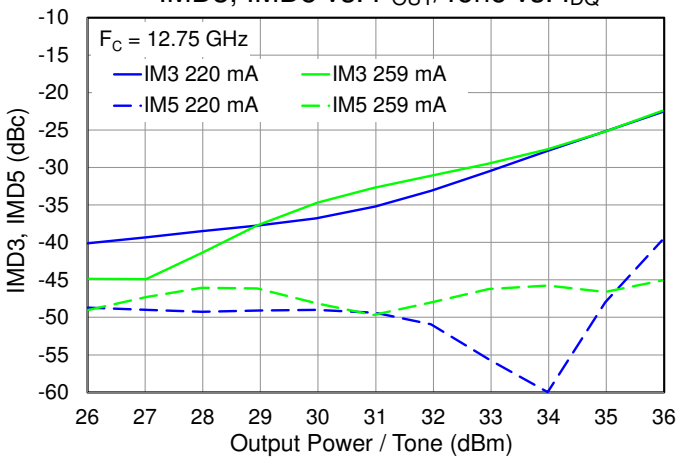




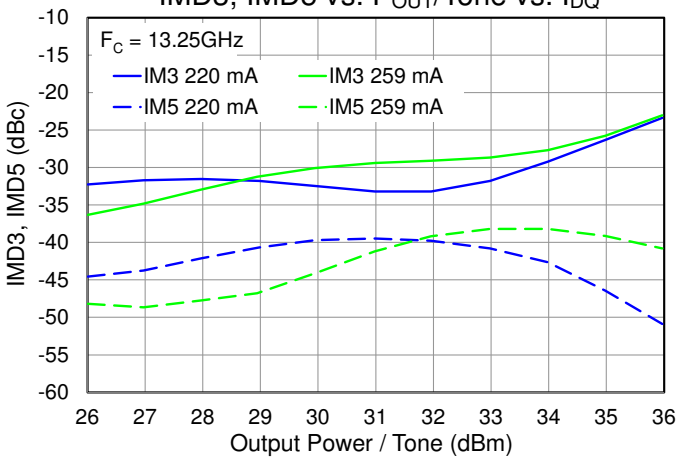
Performance Plots – Linearity (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), Tone Spacing = 20 MHz, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

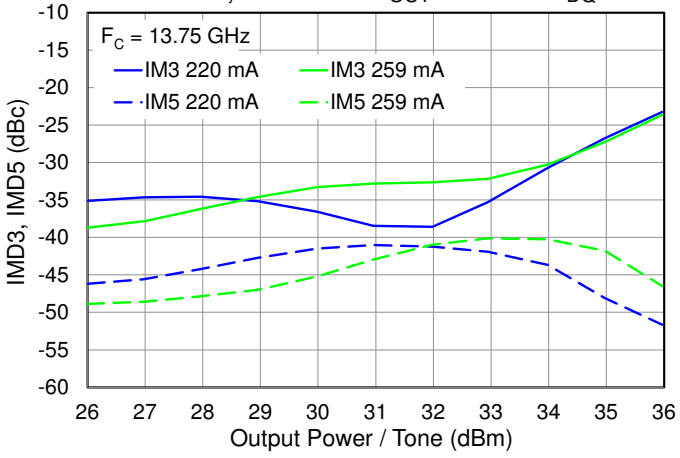
IMD3, IMD5 vs. P_{OUT}/Tone vs. I_{DQ}



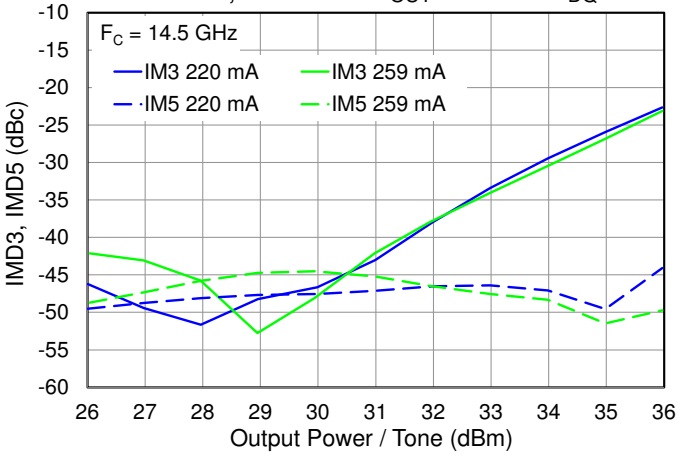
IMD3, IMD5 vs. P_{OUT}/Tone vs. I_{DQ}



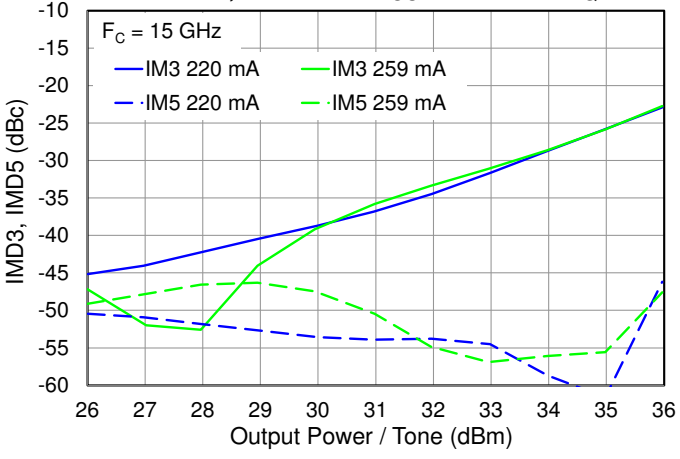
IMD3, IMD5 vs. P_{OUT}/Tone vs. I_{DQ}



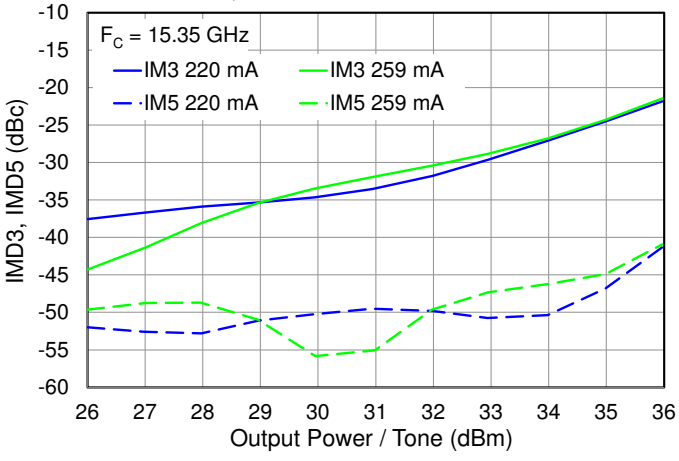
IMD3, IMD5 vs. P_{OUT}/Tone vs. I_{DQ}



IMD3, IMD5 vs. P_{OUT}/Tone vs. I_{DQ}



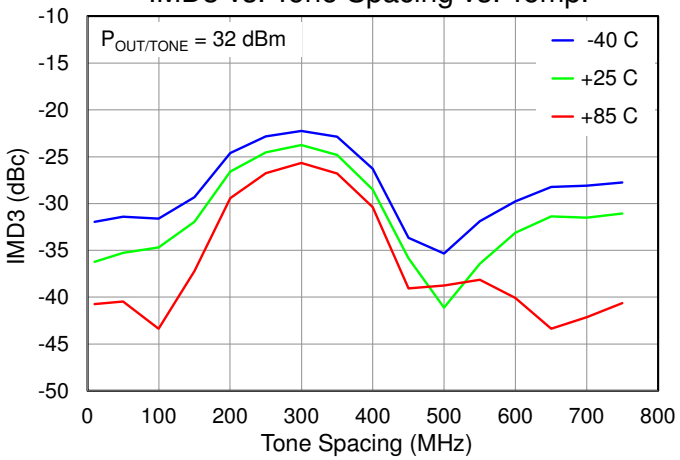
IMD3, IMD5 vs. P_{OUT}/Tone vs. I_{DQ}



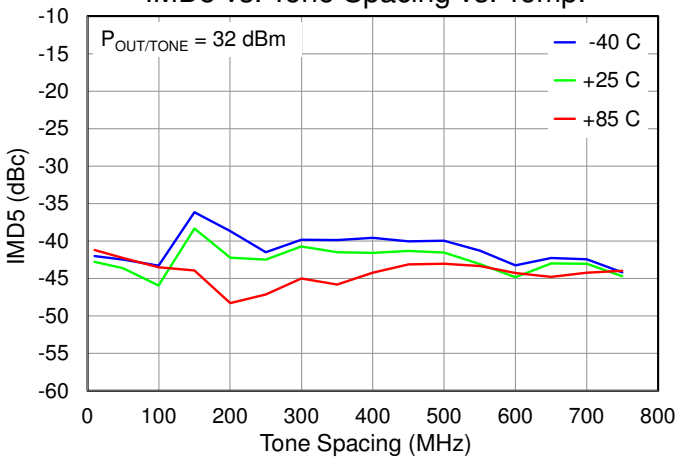
Performance Plots – Linearity (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), F_C = 14.125 GHz, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

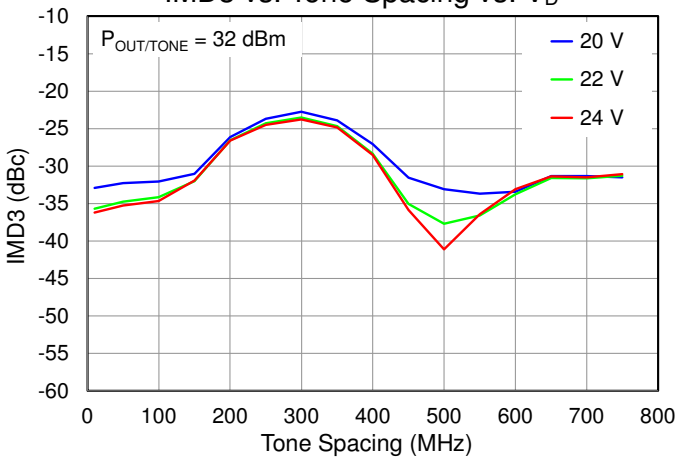
IMD3 vs. Tone Spacing vs. Temp.



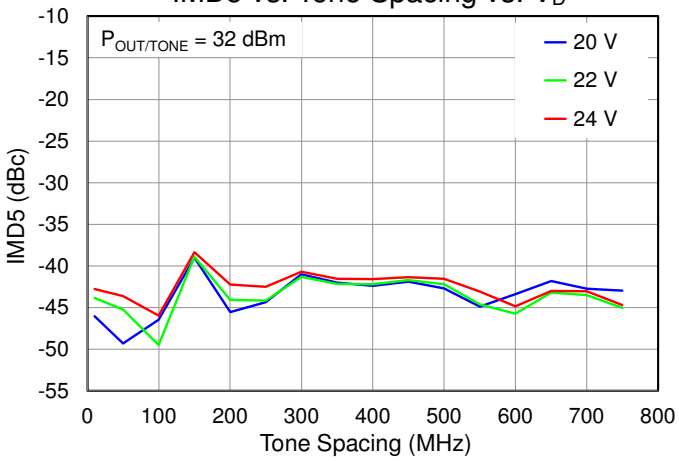
IMD5 vs. Tone Spacing vs. Temp.



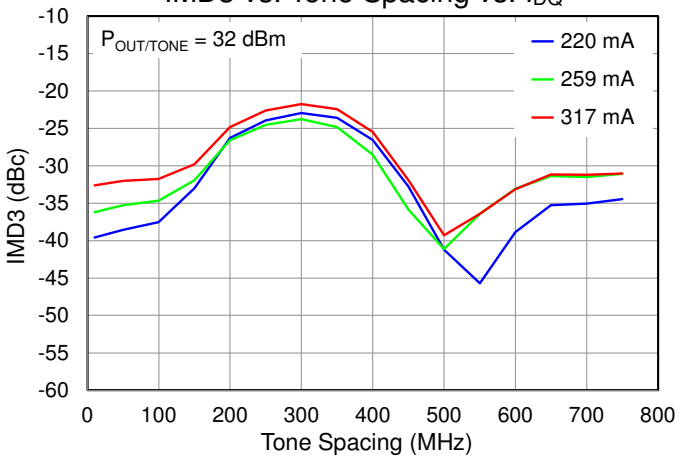
IMD3 vs. Tone Spacing vs. V_D



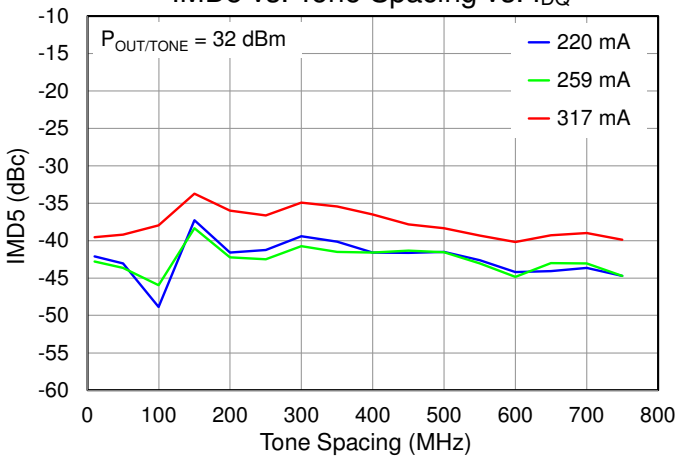
IMD5 vs. Tone Spacing vs. V_D



IMD3 vs. Tone Spacing vs. I_{DQ}



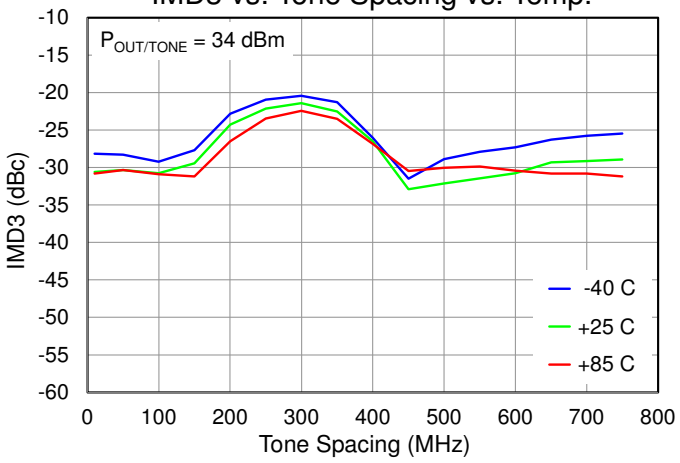
IMD5 vs. Tone Spacing vs. I_{DQ}



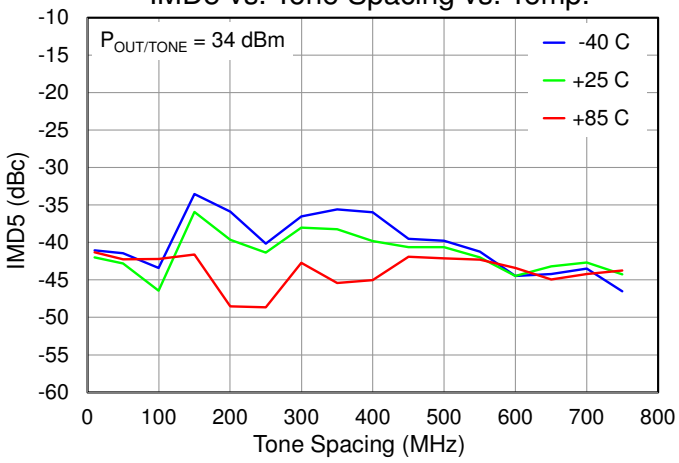
Performance Plots – Linearity (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), F_C = 14.125 GHz, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

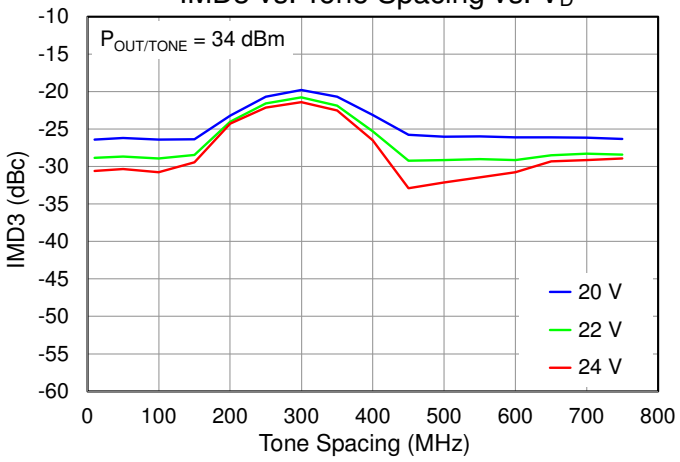
IMD3 vs. Tone Spacing vs. Temp.



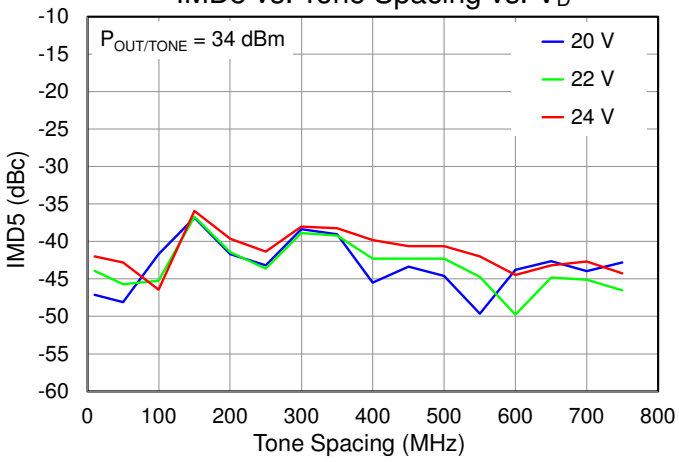
IMD5 vs. Tone Spacing vs. Temp.



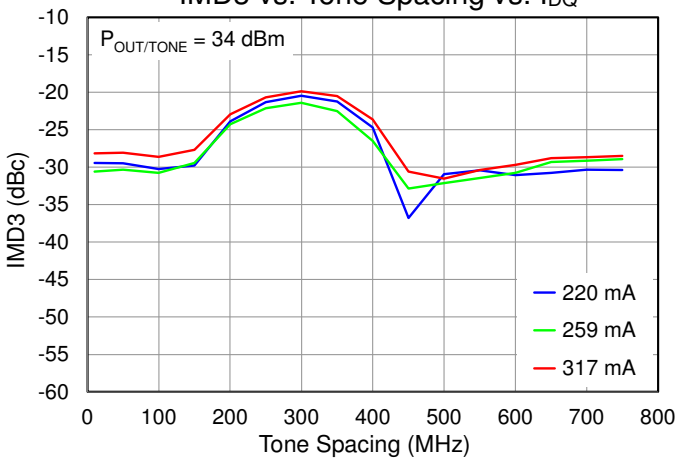
IMD3 vs. Tone Spacing vs. V_D



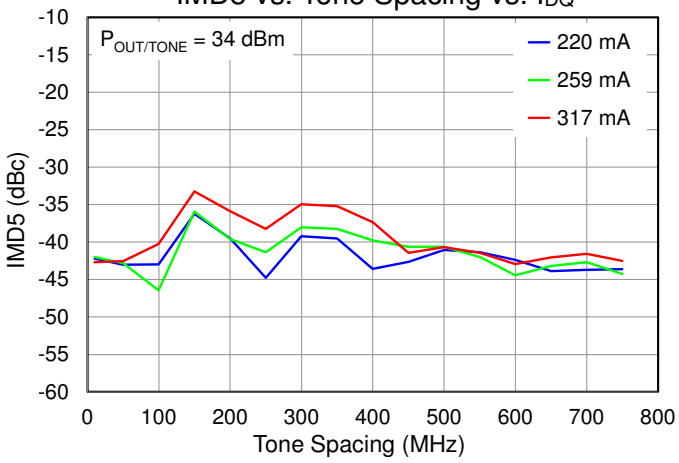
IMD5 vs. Tone Spacing vs. V_D



IMD3 vs. Tone Spacing vs. I_{DQ}



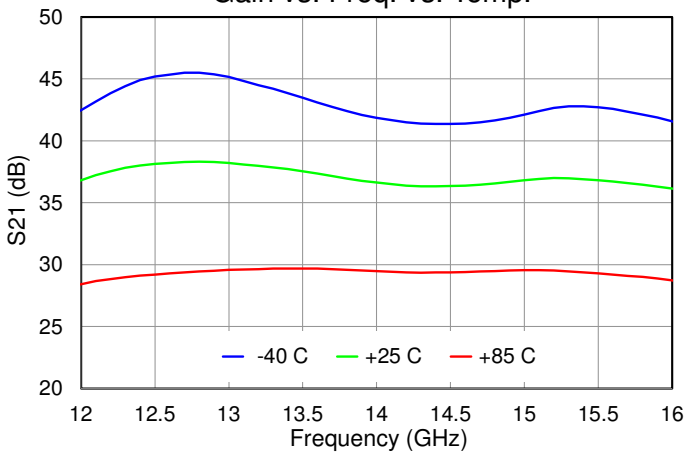
IMD5 vs. Tone Spacing vs. I_{DQ}



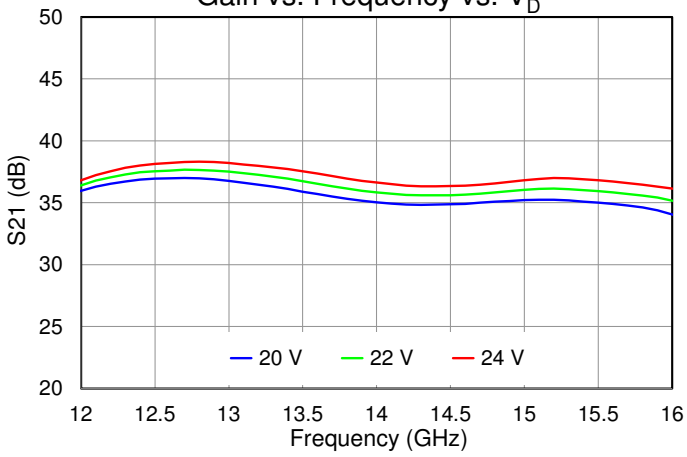
Performance Plots – Small Signal (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), P_{IN} = -30 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).

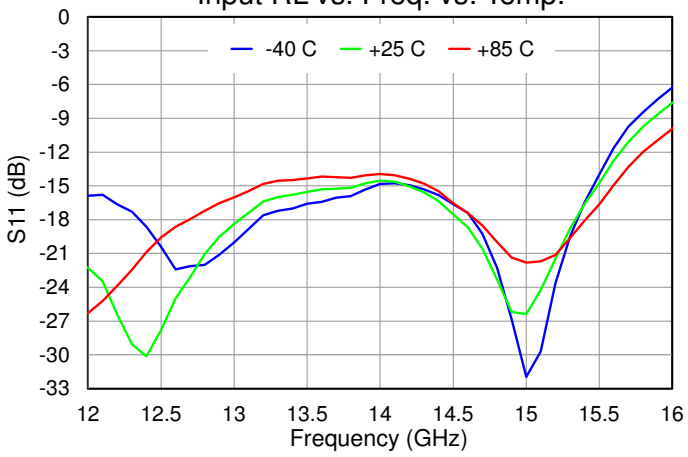
Gain vs. Freq. vs. Temp.



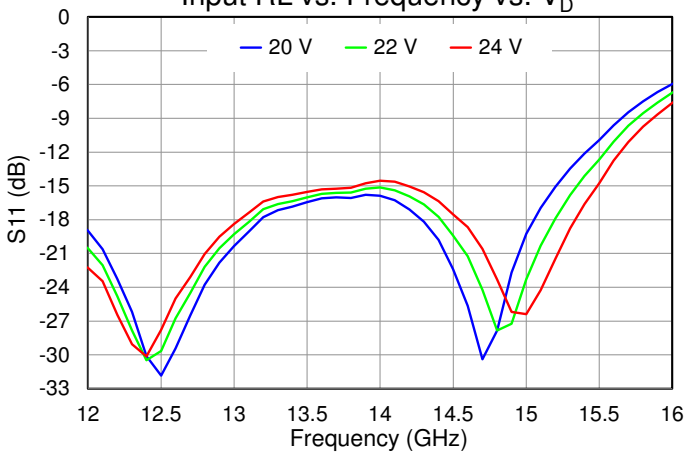
Gain vs. Frequency vs. V_D



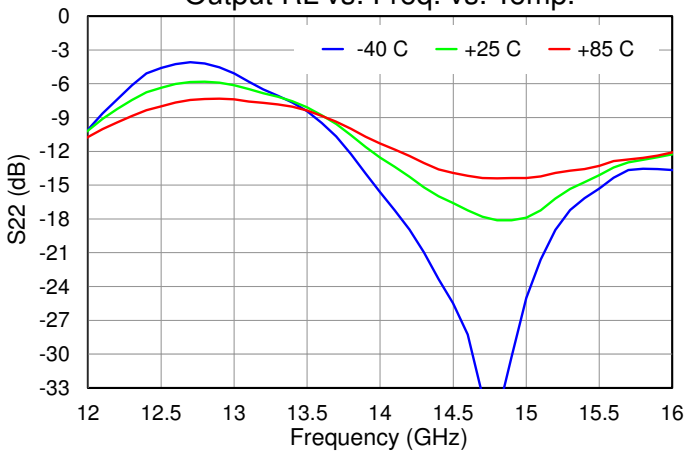
Input RL vs. Freq. vs. Temp.



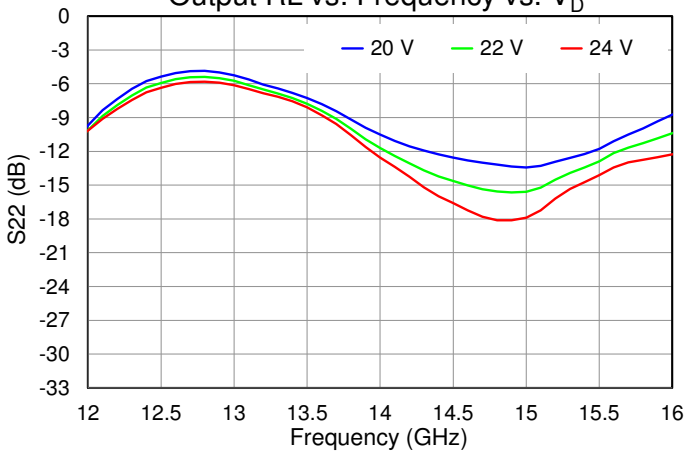
Input RL vs. Frequency vs. V_D



Output RL vs. Freq. vs. Temp.

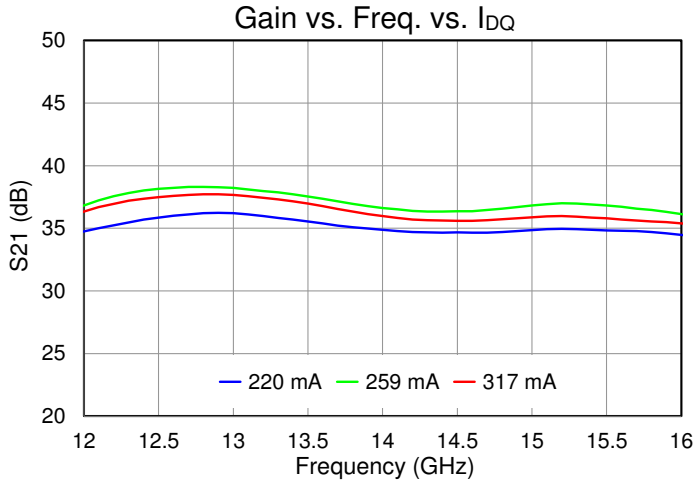


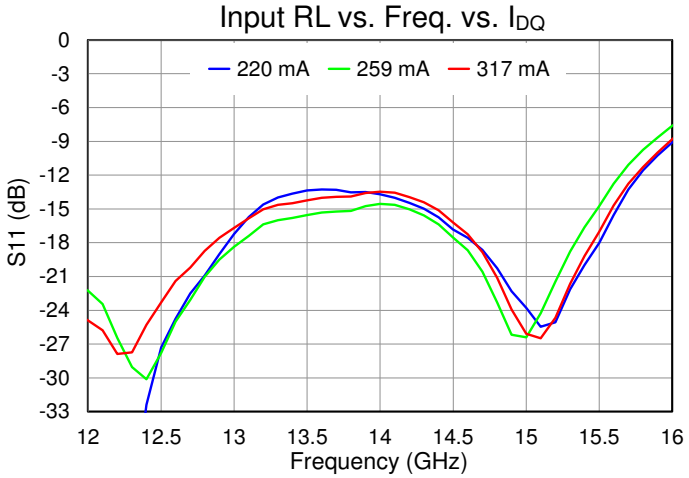
Output RL vs. Frequency vs. V_D

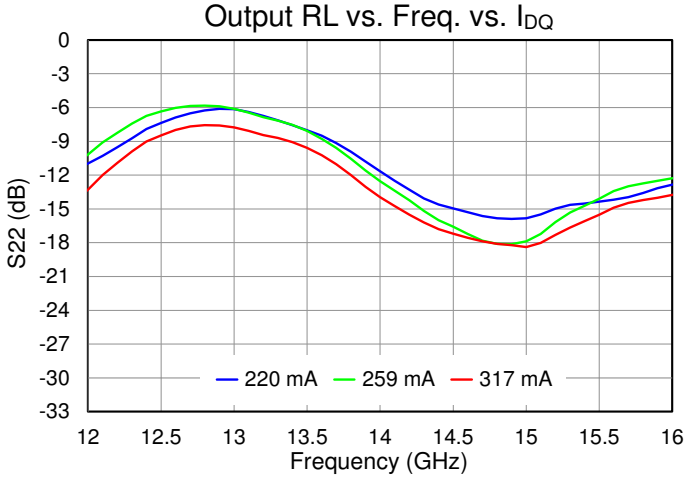


Performance Plots – Small Signal (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), P_{IN} = -30 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0016).







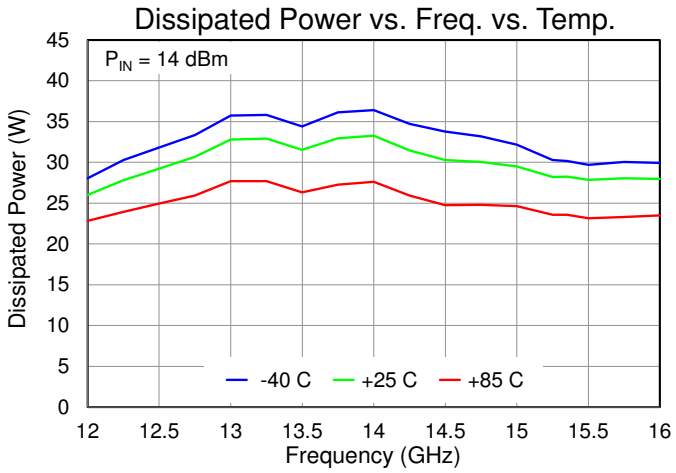
Thermal and Reliability Information

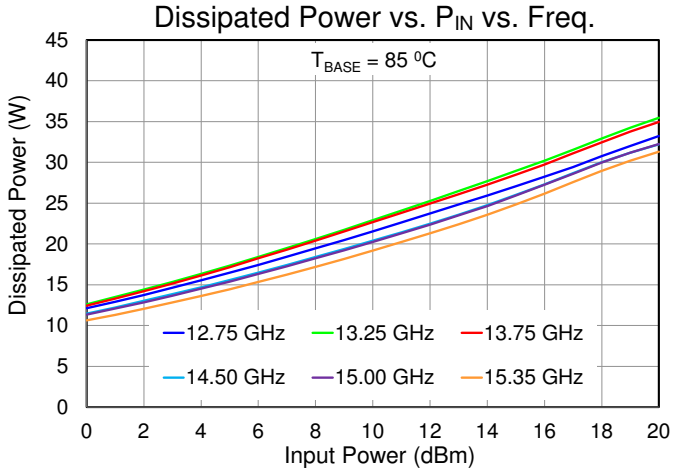
Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} (1)	Quiescent, no RF T_{BASE} = 85 °C, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), P_{DISS} = 6.22 W	2.10	ºC/W
Channel Temperature, T_{CH} (2)		98	°C
Thermal Resistance, θ_{JC} (1)	CW, P_{IN} = 14 dBm (5 W linearity P_{OUT}), T_{BASE} = 85 °C, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), I_{D_DRIVE} = 1720 mA (I_{D12_DRIVE} = 315 mA, I_{D3_DRIVE} = 1405 mA), Freq = 14 GHz, P_{OUT} = 41.3 dBm, P_{DISS} = 27.7 W.	2.22	ºC/W
Channel Temperature, T_{CH} (2)		147	°C

Notes:

1. Thermal resistance determined to T_{BASE} (T_{BASE} is backside of package QPA0016; see p. 29 offset temperature based on Qorvo's EVB design for reference).
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note "GaN Device TCHMAX Theta-JC and Reliability Estimates," located here https://www.qorvo.com/products/d/da006480

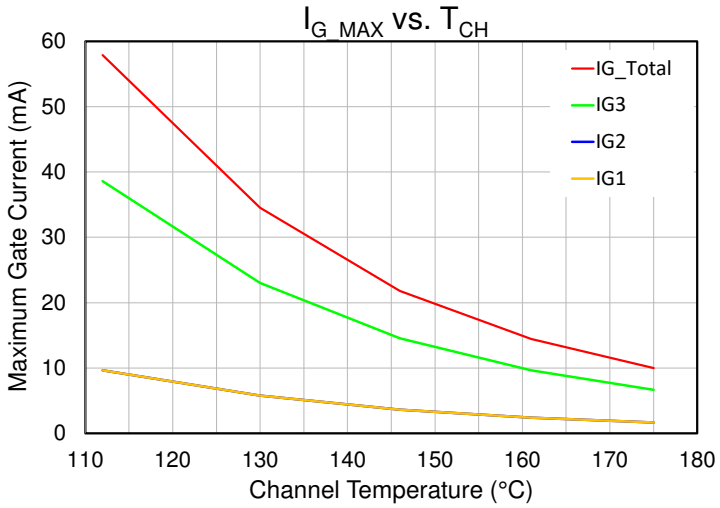
Dissipated Power





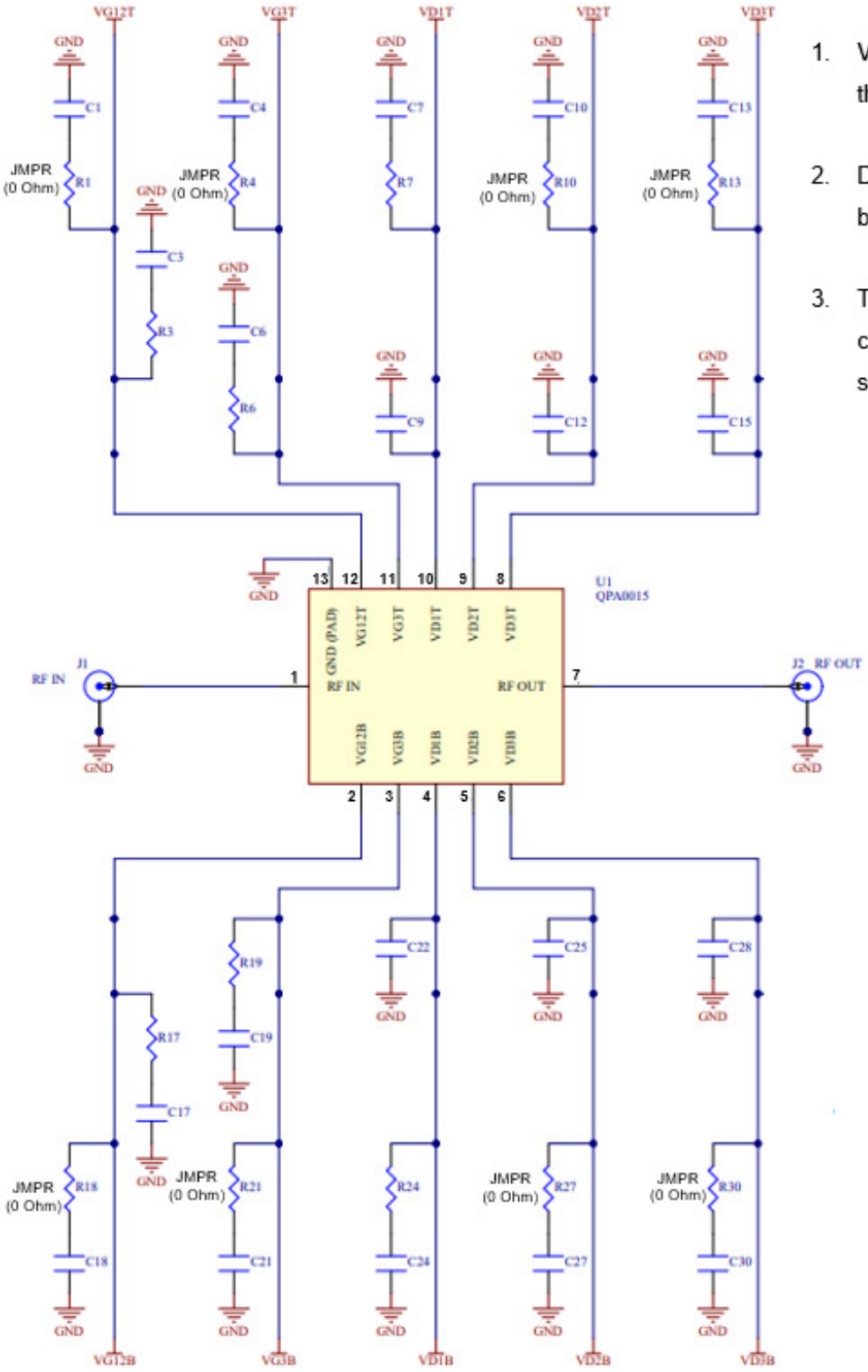
Test conditions, unless otherwise noted.
CW, V_D = 24 V, I_{DQ} = 259 mA (I_{D12} = 131 mA, I_{D3} = 128 mA), T_{BASE} = 85 ºC (T_{BASE} is back side of QPA0016)

Maximum Gate Current



Channel Temperature is an IR scan equivalent

Applications Information



1. V_{D1} and V_{D2} can be tied together at the harness level to form V_{D12}.
2. Drain (V_D's) and Gate (V_G's) can be biased from either or both sides.
3. The external bypassing components are required on both sides (included for non-bias side).

Bill of Materials

Reference Des.	Qty	Value	Description	Part Number
C1, C4, C7, C10, C13, C18, C21, C24, C27, C30	10	10 uF	CAP, 10uF, ±20%, 50V, X5R, 1206	
C3, C6, C9, C12, C15, C17, C19, C22, C25, C28	10	0.01 uF (1)	CAP, 0.01uF, ±10%, 50V, X7R, 0402	
R1, R4, R10, R13, R18, R21, R27, R30	8	0 Ω	RES, 0 Ohm, JMPR, 0402	
R3, R6, R17, R19	4	10 Ω	RES, 10 Ohm, ±1%, 1/16W, 0402	
R7, R24	2	0 Ω	RES, 0 Ohm, 1/10W, 0603	
PCB	1		PCB for QPA0016 (Cu-coined via, see page 28)	Qorvo, Custom
H1, H2	2		DC Header, ST, 2x6, 0.100”, SMD	
J1, J2	2		RF Connector, 2.92mm, F, Pin 0.005, Diel 0.029	Southwest Microwave
H-Block	1		H-Block, Copper C110, 1.248 x 2.246 x 0.275 in	Qorvo, Custom
S1 – S4	4		Screw, Cap, Socket Head, 2-56X1/8”	
Solder Preform			Solder, Preform, 0.400 x 0.320 x 0.002 in	
Solder			Paste, solder, Syntech, Sn63/Pb37	

1. Place as close to QPA0016 as possible (recommended < 12 mils from QPA0016)

Bias-Up Procedure

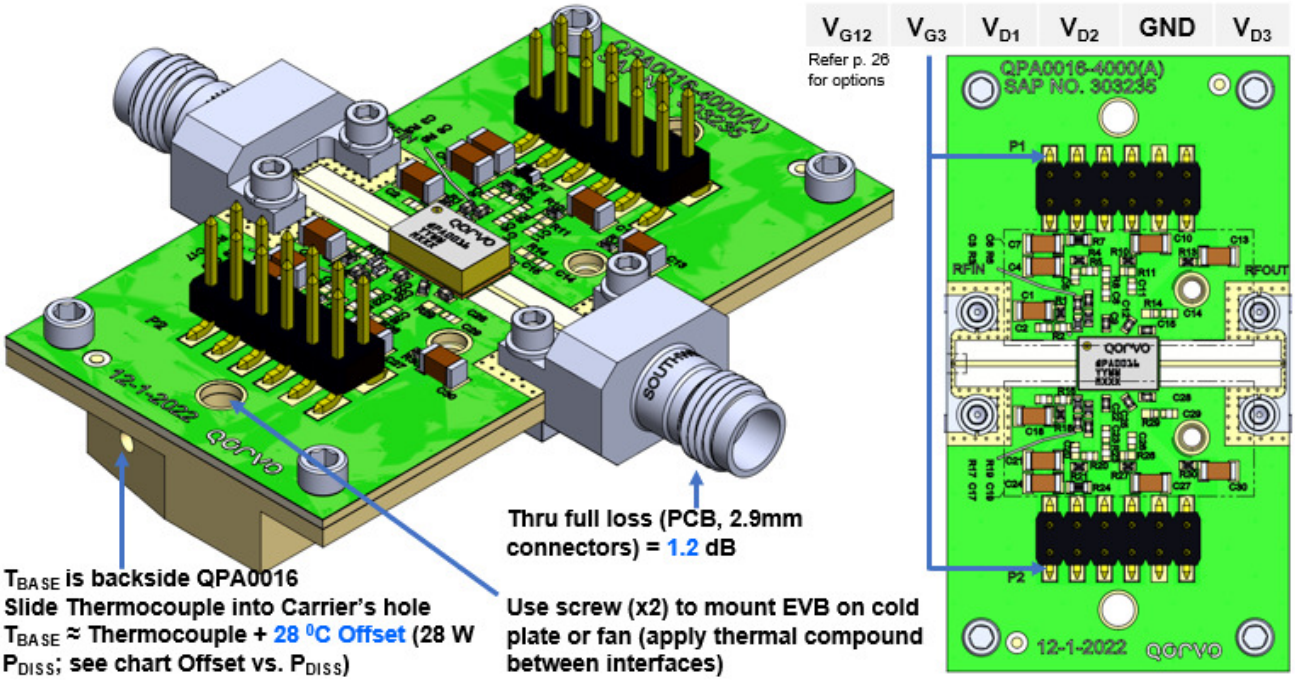
1. Set limit: I_{D12} to 750 mA, I_{D3} to 2000 mA, I_{G12}/I_{G12} to 20 mA each.
2. Set $V_{G12} = V_{G3} = -3.5$ V
3. Set $V_{D12} = V_{D3} = +24$ V. Ensure I_{D12} and I_{D3} ~ 0 mA
4. Adjust V_{G12} more positive until I_{D12} = 131 mA; $V_{G12} \approx$ -2.3 V
   Adjust V_{G3} more positive until I_{D3} = 128 mA; $V_{G3} \approx$ -2.3 V
   $I_{DQ} = I_{D12} + I_{D3}$ = 259 mA; V_G +/- 0.7 V typical range
5. Apply RF signal

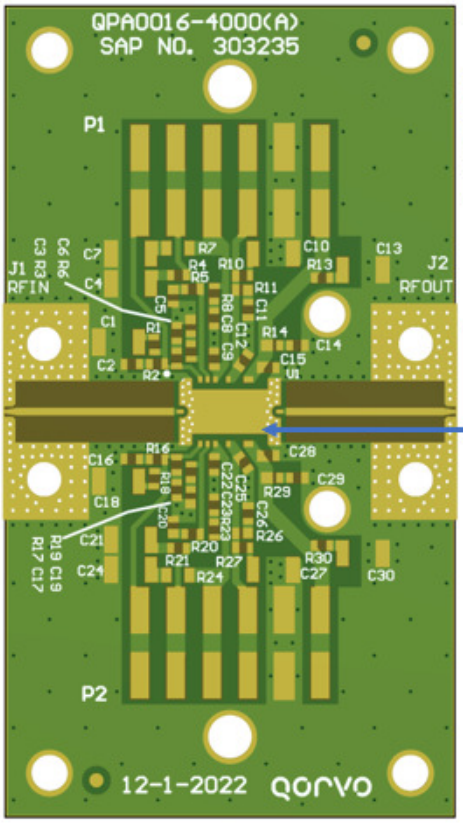
Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to –3.5 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

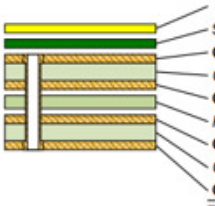
If using three (3) bias supplies for V_D, V_{G12}, V_{G3}: combining all three V_D’s together, adjusting V_{G12} to achieve $I_{DQ} = I_{D12}$, then adjusting V_{G3} to achieve $I_{DQ} = I_{D12} + I_{D3}$

Evaluation Board (EVB) Layout





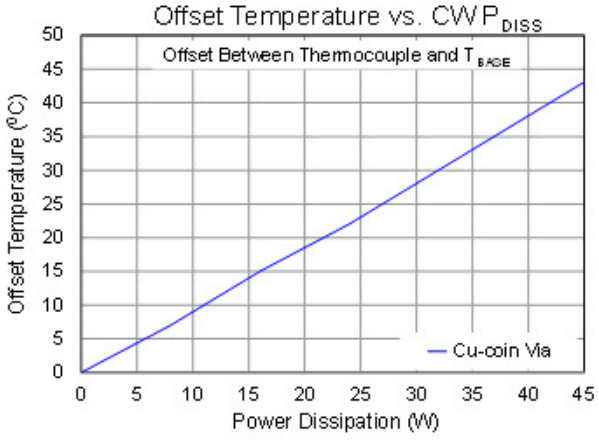
LAYER STACK LEGEND_(COPPER THICKNESS IS ~ FINISHED THICKNESS)



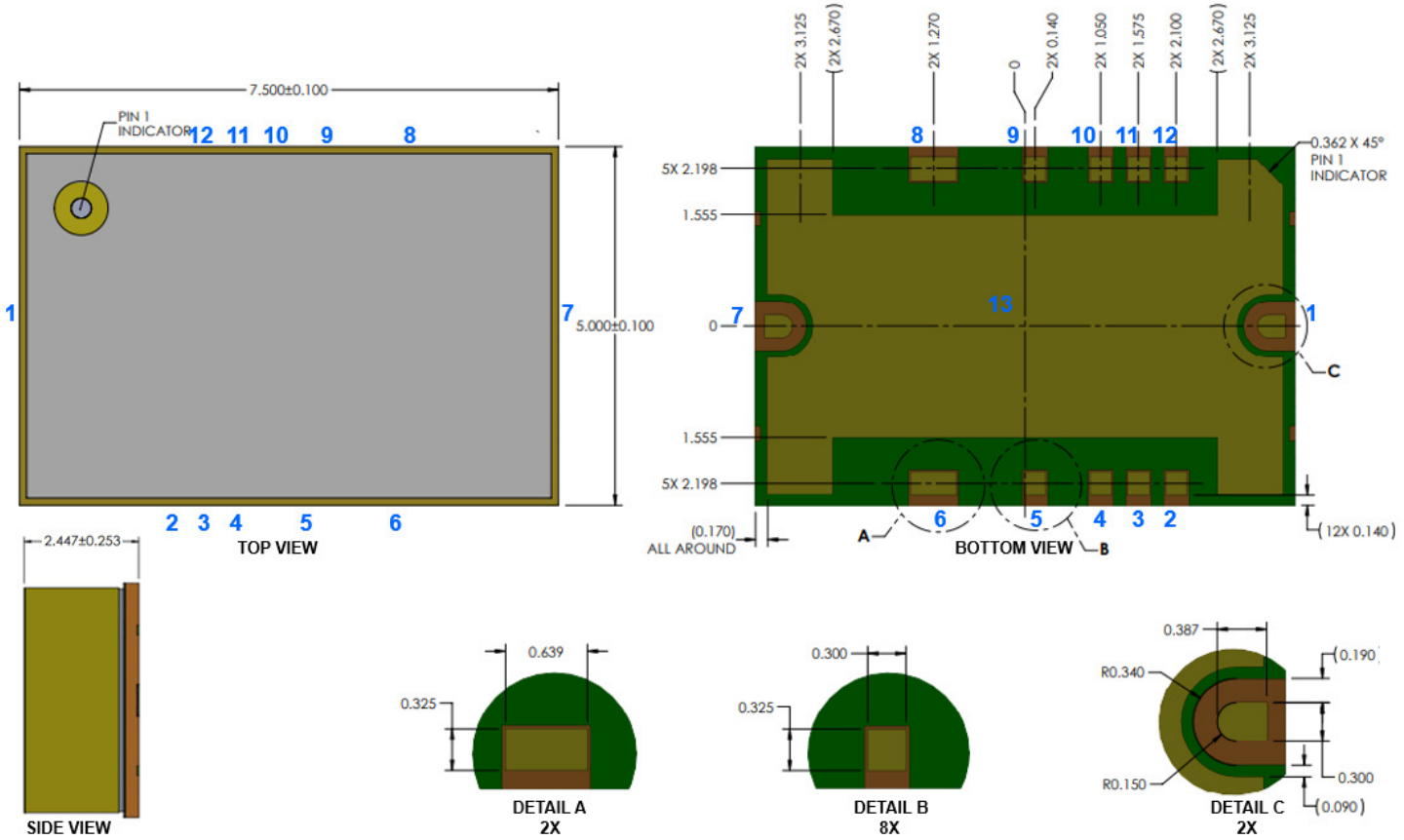
Material	Layer	Thickness	Dielectric Material	Type
	Top Overlay			Legend
Surface Material	Top Solder	0.0010in	Solder Resist	Solder Mask
Copper	**METAL1_TOP**	**0.0020in**		**Signal**
Core		*0.0100in*	*TACONICS RF-35HTC*	*Dielectric*
Copper	**METAL2_MID1**	**0.0006in**		**Signal**
Prepreg		*0.0085in*	*370HR*	*Dielectric*
Copper	**METAL3_MID2**	**0.0006in**		**Signal**
Core		*0.0100in*	*370HR*	*Dielectric*
Copper	**METAL4_BOT**	**0.0020in**		**Signal**

Total thickness: 0.0347in

Cu-coin Via, 0.184 x 0.092 in
Offset Temp. (Thermocouple – T_{BASE}) @ 28 W P_{DISS}:
Cu coined: ~ 28 °C
Cu filled: ~ 38 °C



Mechanical Information



Dimensions (unless otherwise specified): mm.
Tolerances (unless noted): .xx = ± .25; .xxx = ± .100; .xxxx = ± .0254; angles = 0.5^0
Package is air-cavity, non-hermetic, epoxy sealed; lid is FR4; base is laminate; leads are Au plated.

.

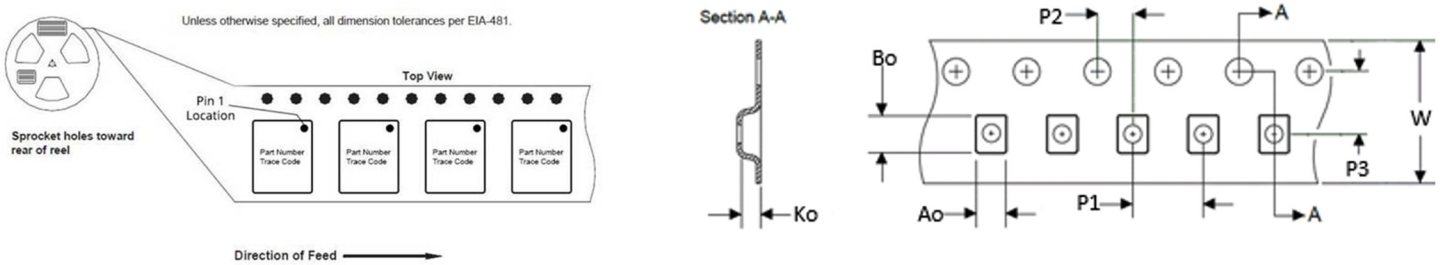
Pin Description

Pin Number	Symbol	Description
1	RF_{IN}	RF Input. Matched to 50 Ω, DC blocked, DC shorted to ground
2, 12	V_{G12}	Gate voltage for stage 1 and 2 (1)
3, 11	V_{G3}	Gate voltage for stage 3 (1)
4, 10	V_{D1}	Drain voltage for stage 1 (1)
5, 9	V_{D2}	Drain voltage for stage 2 (1)
6, 8	V_{D3}	Drain voltage for stage 3 (1)
7	RF_{OUT}	RF Output. Matched to 50 Ω, DC blocked, DC shorted to ground
13	GND	Ground (backside paddle); grounded on PCB; Cu-coined via should be employed to minimize inductance and thermal resistance

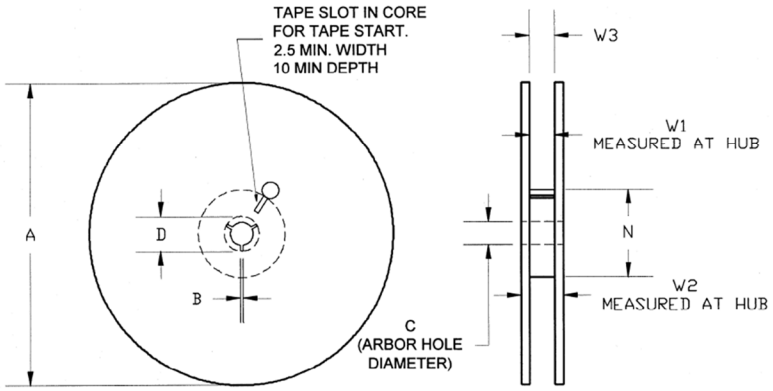
1. External bypassing required; refer to page 27 for recommendation.

Tape & Reel Information

Standard T/R size = 200 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.216	5.5
	Width	B0	0.315	8.0
	Depth	K0	0.112	2.85
	Pitch	P1	0.315	8
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.0
	Cavity to Perforation - Width Direction	P3	0.295	7.50
Cover Tape	Width	C	0.524	13.3
Carrier Tape	Width	W	0.630	16.0



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330
	Thickness	W2	0.882	22.4
	Space Between Flange	W1	.646	16.4
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	.795	20.2

Solderability

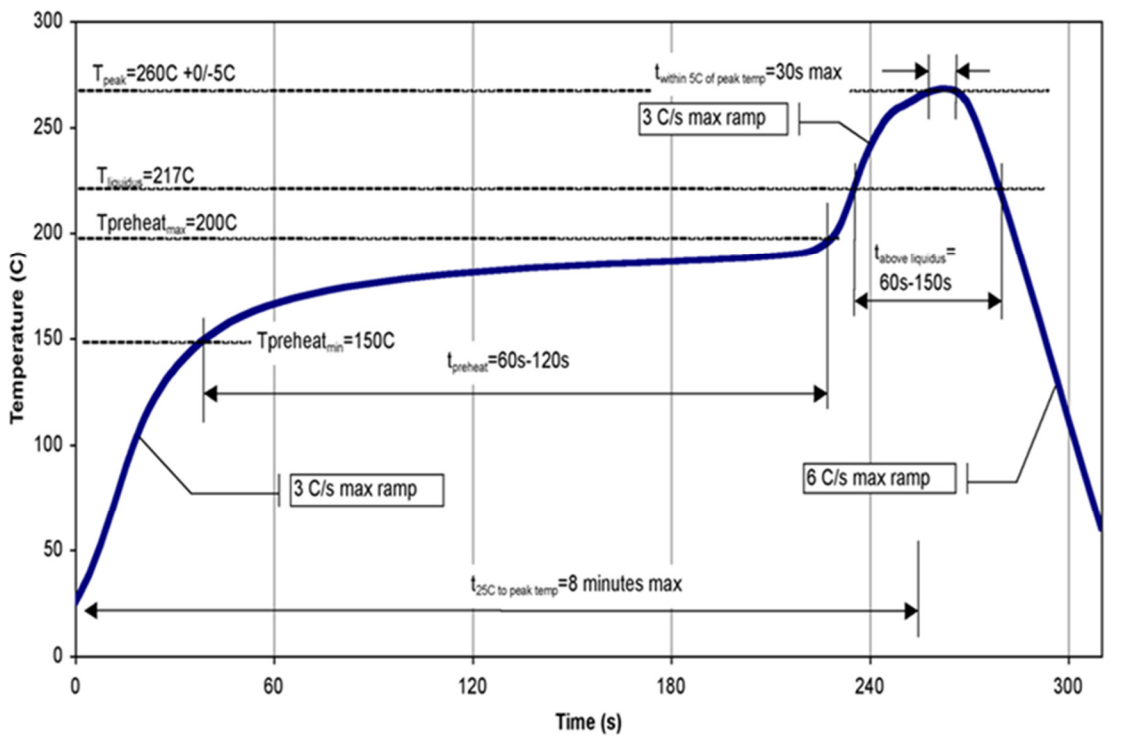
Compatible with the latest version of J-STD-020, lead-free solder, 260 °C peak reflow temperature

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended.

Contact plating: Ni-Au

Solder rework not recommended.

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	C1	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	5A	IPC/JEDEC J-STD-020

Caution!

ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

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